

## Advance Information

# Low Skew CMOS PLL Clock Drivers, 3-State 55, 70, 100, 133 and 160MHz Versions

**MC88915TFN55**  
**MC88915TFN70**  
**MC88915TFN100**  
**MC88915TFN133**  
**MC88915TFN160**

**LOW SKEW CMOS  
PLL CLOCK DRIVER**

The MC88915T Clock Driver utilizes phase-locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations. For a 3.3V version, see the MC88LV915T data sheet.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 7).

Five "Q" outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The  $\overline{Q5}$  output is inverted (180° phase shift) from the "Q" outputs. The 2X\_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X\_Q F<sub>max</sub> specification. The wiring diagrams in Figure 5 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The **FREQ\_SEL** pin provides one bit programmable divide-by in the feedback path of the PLL. It selects between divide-by-1 and divide-by-2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications **FREQ\_SEL** should be held high (+1). If a low frequency reference clock input is used, holding **FREQ\_SEL** low (+2) will allow the VCO to run in its optimal range (>20MHz and >40MHz for the TFN133 version).

In normal phase-locked operation the **PLL\_EN** pin is held high. Pulling the **PLL\_EN** pin low disables the VCO and puts the 88915 in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board-level testing (see detailed description on page 11).

Pulling the **OE/RST** pin low puts the clock outputs 2X\_Q, Q0–Q4,  $\overline{Q5}$  and Q/2 into a high impedance state (3-state). After the **OE/RST** pin goes back high Q0–Q4,  $\overline{Q5}$  and Q/2 will be reset in the low state, with 2X\_Q being the inverse of the selected SYNC input. Assuming **PLL\_EN** is low, the outputs will remain reset until the 88915 sees a SYNC input pulse.

A lock indicator output (LOCK) will go high when the loop is in steady-state phase and frequency lock. The LOCK output will go low if phase-lock is lost or when the **PLL\_EN** pin is low. The LOCK output will go high no later than 10ms after the 88915 sees a SYNC signal and full 5V V<sub>CC</sub>.

## Features

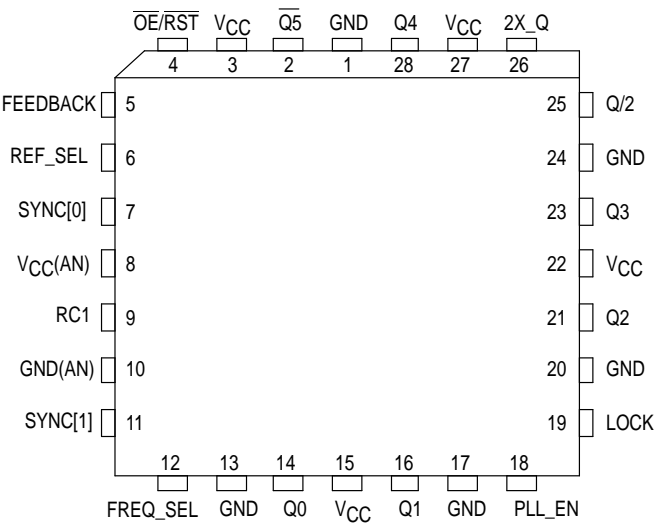
- Five Outputs (Q0–Q4) with Output-Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part-to-part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t<sub>PD</sub> specification, which defines the part-to-part skew)
- Input/Output phase-locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X\_Q F<sub>MAX</sub> spec. (10MHz – 2X\_Q F<sub>MAX</sub> for the TFN133 version)
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a  $\overline{Q}$  (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL-level compatible. ±88mA I<sub>OL</sub>/I<sub>OH</sub> specifications guarantee 50Ω transmission line switching on the incident edge
- Test Mode pin (**PLL\_EN**) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3-state) for board test purposes
- Lock Indicator (LOCK) accuracy indicates a phase-locked state

Yield Surface Modeling and YSM are trademarks of Motorola, Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



Pinout: 28-Lead PLCC (Top View)

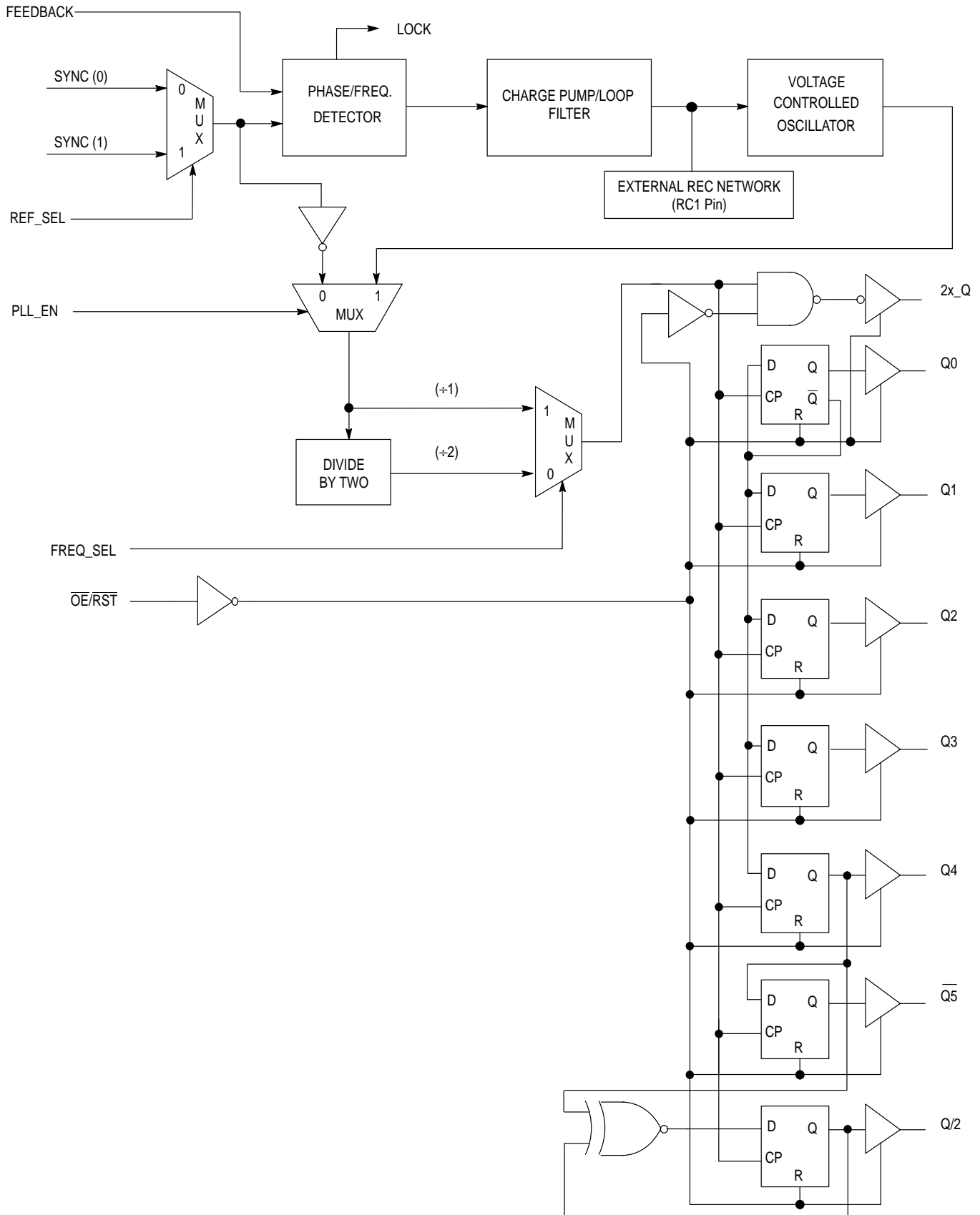


**FN SUFFIX**  
PLASTIC PLCC  
CASE 776-02

PIN SUMMARY

Pin Name	Num	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between sync[0] & Sync[1]
FREQ_SEL	1	Input	Doubles VCO Internal Frequency (low)
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0-4)	5	Output	Clock output (locked to sync)
Q5	1	Output	Inverse of clock output
2x_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Clock output(Q) frequency ÷ 2 (synchronous)
LOCK	1	Output	Indicates phase lock has been achieved (high when locked)
OE/RST	1	Input	Output Enable/Asynchronous reset (active low)
PLL_EN	1	Input	Disables phase-lock for low freq. testing
VCC,GND	11		Power and ground pins (note pins 8, 10 are "analog" supply pins for internal PLL only)

## MC88915T BLOCK DIAGRAM (ALL VERSIONS)



## MC88915TFN55 and MC88915TFN70

### SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum		Maximum	Unit
		TFN70	TFN55		
$t_{RISE/FALL, SYNC}$ Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	—	3.0	ns
$t_{CYCLE, SYNC}$ Inputs	Input Clock Period SYNC Inputs	28.5 <sup>1</sup>	36.0 <sup>1</sup>	200 <sup>2</sup>	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% $\pm$ 25%			

<sup>1</sup>. These  $t_{CYCLE}$  minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.

<sup>2</sup>. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ\_SEL is high or low.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  for 55MHz Version;  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$  for 70MHz Version;  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Target Limit	Unit
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	2.0 2.0	V
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	0.8 0.8	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OH} = -36\text{mA}$ <sup>1</sup>	4.75 5.25	4.01 4.51	V
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OL} = 36\text{mA}$ <sup>1</sup>	4.75 5.25	0.44 0.44	V
$I_{in}$	Maximum Input Leakage Current	$V_I = V_{CC}$ or GND	5.25	$\pm 1.0$	$\mu\text{A}$
$I_{CCT}$	Maximum $I_{CC}$ /Input	$V_I = V_{CC} - 2.1\text{V}$	5.25	2.0 <sup>2</sup>	mA
$I_{OLD}$	Minimum Dynamic Output Current <sup>3</sup>	$V_{OLD} = 1.0\text{V}$ Max	5.25	88	mA
$I_{OHD}$		$V_{OHD} = 3.85\text{V}$ Min	5.25	-88	mA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_I = V_{CC}$ or GND	5.25	1.0	mA
$I_{OZ}$	Maximum 3-State Leakage Current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND	5.25	$\pm 50$ <sup>4</sup>	$\mu\text{A}$

<sup>1</sup>.  $I_{OL}$  and  $I_{OH}$  are 12mA and -12mA respectively for the LOCK output.

<sup>2</sup>. The PLL\_EN input pin is not guaranteed to meet this specification.

<sup>3</sup>. Maximum test duration is 2.0ms, one output loaded at a time.

<sup>4</sup>. Specification value for  $I_{OZ}$  is preliminary, will be finalized upon 'MC' status.

### CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = 5.0\text{V}$
$C_{PD}$	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0\text{V}$
$PD_1$	Power Dissipation @ 50MHz with 50 $\Omega$ Thevenin Termination	23mW/Output 184mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$
$PD_2$	Power Dissipation @ 50MHz with 50 $\Omega$ Parallel Termination to GND	57mW/Output 456mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$

NOTE:  $PD_1$  and  $PD_2$  mW/Output numbers are for a 'Q' output.

**FREQUENCY SPECIFICATIONS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ )

Symbol	Parameter	Guaranteed Minimum		Unit
		TFN70	TFN55	
$f_{max}$ <sup>1</sup>	Maximum Operating Frequency (2X_Q Output)	70	55	MHz
	Maximum Operating Frequency (Q0-Q4, Q5 Output)	35	27.5	MHz

<sup>1</sup>. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 $\Omega$  terminated to  $V_{CC}/2$ .

**MC88915TFN55 and MC88915TFN70** (continued)**AC CHARACTERISTICS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ , Load =  $50\Omega$  Terminated to  $V_{CC}/2$ )

Symbol	Parameter	Min	Max	Unit	Condition
tRISE/FALL Outputs	Rise/Fall Time, All Outputs (Between 0.2V <sub>CC</sub> and 0.8V <sub>CC</sub> )	1.0	2.5	ns	Into a 50Ω Load Terminated to V <sub>CC</sub> /2
tRISE/FALL <sup>1</sup> 2X_Q Output	Rise/Fall Time Into a 20pF Load, With Termination Specified in Note <sup>2</sup>	0.5	1.6	ns	tRISE: 0.8V – 2.0V tFALL: 2.0V – 0.8V
tPULSE WIDTH <sup>1</sup> (Q0–Q4, Q5, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, Q5, Q/2 @ V <sub>CC</sub> /2	0.5tCYCLE – 0.5 <sup>2</sup>	0.5tCYCLE + 0.5 <sup>2</sup>	ns	Into a 50Ω Load Terminated to V <sub>CC</sub> /2
tPULSE WIDTH <sup>1</sup> (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5V	66MHz 0.5tCYCLE – 0.5 <sup>2</sup> 50MHz 0.5tCYCLE – 1.0 40MHz 0.5tCYCLE – 1.5	0.5tCYCLE + 0.5 <sup>2</sup> 0.5tCYCLE + 1.0 0.5tCYCLE + 1.5	ns	Must Use Termination Specified in Note <sup>2</sup>
tPULSE WIDTH <sup>1</sup> (2X_Q Output)	Output Pulse Width: 2X_Q @ V <sub>CC</sub> /2	50–65MHz 0.5tCYCLE – 1.0 <sup>2</sup> 40–49MHz 0.5tCYCLE – 1.5 66–70MHz 0.5tCYCLE – 0.5	0.5tCYCLE + 1.0 <sup>2</sup> 0.5tCYCLE + 1.5 0.5tCYCLE + 0.5	ns	Into a 50Ω Load Terminated to V <sub>CC</sub> /2
tPD <sup>1,3</sup> SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V <sub>CC</sub> )		ns	See Note <sup>4</sup> and Figure 2 for Detailed Explanation
		–1.05	–0.40		
		(With 1MΩ from RC1 to An GND)			
		+1.25	+3.25		
tSKEW <sub>r</sub> <sup>1,4</sup> (Rising) See Note <sup>5</sup>	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V <sub>CC</sub> /2
tSKEW <sub>f</sub> <sup>1,4</sup> (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V <sub>CC</sub> /2
tSKEW <sub>all</sub> <sup>1,4</sup>	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, Q5 Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V <sub>CC</sub> /2
tLOCK <sup>5</sup>	Time Required to Acquire Phase-Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
tPZL <sup>6</sup>	Output Enable Time OE/RST to 2X_Q, Q0–Q4, Q5, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
tPHZ,tPLZ <sup>6</sup>	Output Disable Time OE/RST to 2X_Q, Q0–Q4, Q5, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. These specifications are not tested, they are guaranteed by statistical characterization. See AC specification Note 1.

2.  $T_{CYCLE}$  in this spec is  $1/\text{Frequency}$  at which the particular output is running.

3. The  $T_{PD}$  specification's min/max values may shift closer to zero if a larger pullup resistor is used.

4. Under equally loaded conditions and at a fixed temperature and voltage.

5. With  $V_{CC}$  fully powered-on, and an output properly connected to the FEEDBACK pin.  $t_{LOCK}$  maximum is with  $C1 = 0.1\mu\text{F}$ ,  $t_{LOCK}$  minimum is with  $C1 = 0.01\mu\text{F}$ .

6. The  $t_{PZL}$ ,  $t_{PHZ}$ ,  $t_{PLZ}$  minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

## MC88915TFN100

## SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL, SYNC}$ Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	3.0	ns
$t_{CYCLE}$ , SYNC Inputs	Input Clock Period SYNC Inputs	20.0 <sup>1</sup>	200 <sup>2</sup>	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% $\pm$ 25%		

1. These  $t_{CYCLE}$  minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.

2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if  $FREQ\_SEL$  is high or low.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ 

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Target Limit	Unit
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	2.0 2.0	V
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	0.8 0.8	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OH} = -36\text{mA}$ <sup>1</sup>	4.75 5.25	4.01 4.51	V
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OL} = 36\text{mA}$ <sup>1</sup>	4.75 5.25	0.44 0.44	V
$I_{in}$	Maximum Input Leakage Current	$V_I = V_{CC}$ or GND	5.25	$\pm 1.0$	$\mu\text{A}$
$I_{CCT}$	Maximum $I_{CC}/\text{Input}$	$V_I = V_{CC} - 2.1\text{V}$	5.25	2.0 <sup>2</sup>	mA
$I_{OLD}$	Minimum Dynamic Output Current <sup>3</sup>	$V_{OLD} = 1.0\text{V}$ Max	5.25	88	mA
$I_{OHD}$		$V_{OHD} = 3.85\text{V}$ Min	5.25	-88	mA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_I = V_{CC}$ or GND	5.25	1.0	mA
$I_{OZ}$	Maximum 3-State Leakage Current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND	5.25	$\pm 50$ <sup>4</sup>	$\mu\text{A}$

1.  $I_{OL}$  and  $I_{OH}$  are 12mA and -12mA respectively for the LOCK output.

2. The PLL\_EN input pin is not guaranteed to meet this specification.

3. Maximum test duration is 2.0ms, one output loaded at a time.

4. Specification value for  $I_{OZ}$  is preliminary, will be finalized upon 'MC' status.

## CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = 5.0\text{V}$
$C_{PD}$	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0\text{V}$
$PD_1$	Power Dissipation @ 50MHz with 50 $\Omega$ Thevenin Termination	23mW/Output 184mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$
$PD_2$	Power Dissipation @ 50MHz with 50 $\Omega$ Parallel Termination to GND	57mW/Output 456mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$

NOTE:  $PD_1$  and  $PD_2$  mW/Output numbers are for a 'Q' output.

FREQUENCY SPECIFICATIONS ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ )

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN100	
f <sub>max</sub> <sup>1</sup>	Maximum Operating Frequency (2X_Q Output)	100	MHz
	Maximum Operating Frequency (Q0–Q4, Q <sub>5</sub> Output)	50	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 $\Omega$  terminated to  $V_{CC}/2$ .

**MC88915TFN100** (continued)**AC CHARACTERISTICS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ , Load =  $50\Omega$  Terminated to  $V_{CC}/2$ )

Symbol	Parameter	Min	Max	Unit	Condition
tRISE/FALL Outputs	Rise/Fall Time, All Outputs (Between 0.2V <sub>CC</sub> and 0.8V <sub>CC</sub> )	1.0	2.5	ns	Into a 50Ω Load Terminated to V <sub>CC</sub> /2
tRISE/FALL <sup>1</sup> 2X_Q Output	Rise/Fall Time Into a 20pF Load, With Termination Specified in Note <sup>2</sup>	0.5	1.6	ns	tRISE: 0.8V – 2.0V tFALL: 2.0V – 0.8V
tPULSE WIDTH <sup>1</sup> (Q0–Q4, Q5, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, Q5, Q/2 @ V <sub>CC</sub> /2	0.5tCYCLE – 0.5 <sup>2</sup>	0.5tCYCLE + 0.5 <sup>2</sup>	ns	Into a 50Ω Load Terminated to V <sub>CC</sub> /2
tPULSE WIDTH <sup>1</sup> (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5V	0.5tCYCLE – 0.5 <sup>2</sup>	0.5tCYCLE + 0.5 <sup>2</sup>	ns	Must Use Termination Specified in Note <sup>2</sup>
tPULSE WIDTH <sup>1</sup> (2X_Q Output)	Output Pulse Width: 40–49MHz 50–65MHz 66–100MHz 2X_Q @ V <sub>CC</sub> /2	0.5tCYCLE – 1.5 <sup>2</sup> 0.5tCYCLE – 1.0 0.5tCYCLE – 0.5	0.5tCYCLE + 1.5 <sup>2</sup> 0.5tCYCLE + 1.0 0.5tCYCLE + 0.5	ns	Into a 50Ω Load Terminated to V <sub>CC</sub> /2
tPD <sup>1,3</sup> SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V <sub>CC</sub> )		ns	See Note <sup>4</sup> and Figure 2 for Detailed Explanation
		–1.05	–0.30		
		(With 1MΩ from RC1 to An GND)			
		+1.25	+3.25		
tSKEW <sub>r</sub> <sup>1,4</sup> (Rising) See Note <sup>5</sup>	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V <sub>CC</sub> /2
tSKEW <sub>f</sub> <sup>1,4</sup> (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V <sub>CC</sub> /2
tSKEW <sub>all</sub> <sup>1,4</sup>	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, Q5 Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V <sub>CC</sub> /2
tLOCK <sup>5</sup>	Time Required to Acquire Phase-Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
tPZL <sup>6</sup>	Output Enable Time $\overline{\text{OE}}/\overline{\text{RST}}$ to 2X_Q, Q0–Q4, Q5, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
tPHZ,tPLZ <sup>6</sup>	Output Disable Time $\overline{\text{OE}}/\overline{\text{RST}}$ to 2X_Q, Q0–Q4, Q5, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. These specifications are not tested, they are guaranteed by statistical characterization. See AC specification Note 1.

2.  $T_{CYCLE}$  in this spec is  $1/\text{Frequency}$  at which the particular output is running.

3. The  $T_{PD}$  specification's min/max values may shift closer to zero if a larger pullup resistor is used.

4. Under equally loaded conditions and at a fixed temperature and voltage.

5. With  $V_{CC}$  fully powered-on, and an output properly connected to the FEEDBACK pin.  $t_{LOCK}$  maximum is with  $C1 = 0.1\mu\text{F}$ ,  $t_{LOCK}$  minimum is with  $C1 = 0.01\mu\text{F}$ .

6. The  $t_{PZL}$ ,  $t_{PHZ}$ ,  $t_{PLZ}$  minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

## MC88915TFN133

## SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL, SYNC}$ Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	3.0	ns
$t_{CYCLE, SYNC}$ Inputs	Input Clock Period SYNC Inputs	15.0 <sup>1</sup>	100 <sup>2</sup>	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% $\pm$ 25%		

1. These  $t_{CYCLE}$  minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.

2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if  $FREQ\_SEL$  is high or low.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ 

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Target Limit	Unit
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	2.0 2.0	V
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	0.8 0.8	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OH} = -36\text{mA}$ <sup>1</sup>	4.75 5.25	4.01 4.51	V
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OL} = 36\text{mA}$ <sup>1</sup>	4.75 5.25	0.44 0.44	V
$I_{in}$	Maximum Input Leakage Current	$V_I = V_{CC}$ or GND	5.25	$\pm 1.0$	$\mu\text{A}$
$I_{CCT}$	Maximum $I_{CC}/\text{Input}$	$V_I = V_{CC} - 2.1\text{V}$	5.25	2.0 <sup>2</sup>	mA
$I_{OLD}$	Minimum Dynamic Output Current <sup>3</sup>	$V_{OLD} = 1.0\text{V}$ Max	5.25	88	mA
$I_{OHD}$		$V_{OHD} = 3.85\text{V}$ Min	5.25	-88	mA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_I = V_{CC}$ or GND	5.25	1.0	mA
$I_{OZ}$	Maximum 3-State Leakage Current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND	5.25	$\pm 50$ <sup>4</sup>	$\mu\text{A}$

1.  $I_{OL}$  and  $I_{OH}$  are 12mA and -12mA respectively for the LOCK output.

2. The PLL\_EN input pin is not guaranteed to meet this specification.

3. Maximum test duration is 2.0ms, one output loaded at a time.

4. Specification value for  $I_{OZ}$  is preliminary, will be finalized upon 'MC' status.

## CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = 5.0\text{V}$
$C_{PD}$	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0\text{V}$
$PD_1$	Power Dissipation @ 50MHz with 50 $\Omega$ Thevenin Termination	23mW/Output 184mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$
$PD_2$	Power Dissipation @ 50MHz with 50 $\Omega$ Parallel Termination to GND	57mW/Output 456mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$

NOTE:  $PD_1$  and  $PD_2$  mW/Output numbers are for a 'Q' output.

FREQUENCY SPECIFICATIONS ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ )

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN133	
f <sub>max</sub> <sup>1</sup>	Maximum Operating Frequency (2X_Q Output)	133	MHz
	Maximum Operating Frequency (Q0–Q4, Q <sub>5</sub> Output)	66	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 $\Omega$  terminated to  $V_{CC}/2$ .



**MC88915TFN133** (continued)**AC CHARACTERISTICS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ , Load =  $50\Omega$  Terminated to  $V_{CC}/2$ )

Symbol	Parameter	Min	Max	Unit	Condition
tRISE/FALL Outputs	Rise/Fall Time, All Outputs (Between 0.2V <sub>CC</sub> and 0.8V <sub>CC</sub> )	1.0	2.5	ns	Into a 50Ω Load Terminated to V <sub>CC</sub> /2
tRISE/FALL <sup>1</sup> 2X_Q Output	Rise/Fall Time Into a 20pF Load, With Termination Specified in Note <sup>2</sup>	0.5	1.6	ns	tRISE: 0.8V – 2.0V tFALL: 2.0V – 0.8V
tPULSE WIDTH <sup>1</sup> (Q0–Q4, Q5, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, Q5, Q/2 @ V <sub>CC</sub> /2	0.5tCYCLE – 0.5 <sup>2</sup>	0.5tCYCLE + 0.5 <sup>2</sup>	ns	Into a 50Ω Load Terminated to V <sub>CC</sub> /2
tPULSE WIDTH <sup>1</sup> (2X_Q Output)	Output Pulse Width: 66–133MHz 2X_Q @ 1.5V 40–65MHz	0.5tCYCLE – 0.5 <sup>2</sup> 0.5tCYCLE – 0.9	0.5tCYCLE + 0.5 <sup>2</sup> 0.5tCYCLE + 0.9	ns	Must Use Termination Specified in Note <sup>2</sup>
tPULSE WIDTH <sup>1</sup> (2X_Q Output)	Output Pulse Width: 66–133MHz 2X_Q @ V <sub>CC</sub> /2 40–65MHz	0.5tCYCLE – 0.5 <sup>2</sup> 0.5tCYCLE – 0.9	0.5tCYCLE + 0.5 <sup>2</sup> 0.5tCYCLE + 0.9	ns	Into a 50Ω Load Terminated to V <sub>CC</sub> /2
tPD <sup>1,3</sup> SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V <sub>CC</sub> )		ns	See Note <sup>4</sup> and Figure 2 for Detailed Explanation
		–1.05	–0.25		
		(With 1MΩ from RC1 to An GND)			
		+1.25	+3.25		
tSKEW <sub>r</sub> <sup>1,4</sup> (Rising) See Note <sup>5</sup>	Output-to-Output Skew Between Out- puts Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V <sub>CC</sub> /2
tSKEW <sub>f</sub> <sup>1,4</sup> (Falling)	Output-to-Output Skew Between Out- puts Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V <sub>CC</sub> /2
tSKEW <sub>all</sub> <sup>1,4</sup>	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, Q5 Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V <sub>CC</sub> /2
tLOCK <sup>5</sup>	Time Required to Acquire Phase-Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
tPZL <sup>6</sup>	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, Q5, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
tPHZ,tPLZ <sup>6</sup>	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, Q5, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. These specifications are not tested, they are guaranteed by statistical characterization. See AC specification Note 1.

2.  $T_{CYCLE}$  in this spec is  $1/\text{Frequency}$  at which the particular output is running.3. The  $T_{PD}$  specification's min/max values may shift closer to zero if a larger pullup resistor is used.

4. Under equally loaded conditions and at a fixed temperature and voltage.

5. With  $V_{CC}$  fully powered-on, and an output properly connected to the FEEDBACK pin.  $t_{LOCK}$  maximum is with  $C1 = 0.1\mu\text{F}$ ,  $t_{LOCK}$  minimum is with  $C1 = 0.01\mu\text{F}$ .6. The  $t_{PZL}$ ,  $t_{PHZ}$ ,  $t_{PLZ}$  minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

## MC88915TFN160

### SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL, SYNC}$ Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	3.0	ns
$t_{CYCLE}$ , SYNC Inputs	Input Clock Period SYNC Inputs	25	100	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% $\pm$ 25%		

- These  $t_{CYCLE}$  minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
- Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if  $FREQ\_SEL$  is high or low.

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Target Limit	Unit
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	2.0 2.0	V
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	0.8 0.8	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OH} = -36\text{mA}$ <sup>1</sup>	4.75 5.25	4.01 4.51	V
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OL} = 36\text{mA}$ <sup>1</sup>	4.75 5.25	0.44 0.44	V
$I_{in}$	Maximum Input Leakage Current	$V_I = V_{CC}$ or GND	5.25	$\pm 1.0$	$\mu\text{A}$
$I_{CCT}$	Maximum $I_{CC}/\text{Input}$	$V_I = V_{CC} - 2.1\text{V}$	5.25	2.0 <sup>2</sup>	mA
$I_{OLD}$	Minimum Dynamic Output Current <sup>3</sup>	$V_{OLD} = 1.0\text{V}$ Max	5.25	88	mA
$I_{OHD}$		$V_{OHD} = 3.85\text{V}$ Min	5.25	-88	mA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_I = V_{CC}$ or GND	5.25	1.0	mA
$I_{OZ}$	Maximum 3-State Leakage Current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND	5.25	$\pm 50$ <sup>4</sup>	$\mu\text{A}$

- $I_{OL}$  and  $I_{OH}$  are 12mA and -12mA respectively for the LOCK output.
- The PLL\_EN input pin is not guaranteed to meet this specification.
- Maximum test duration is 2.0ms, one output loaded at a time.
- Specification value for  $I_{OZ}$  is preliminary, will be finalized upon 'MC' status.

### CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = 5.0\text{V}$
$C_{PD}$	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0\text{V}$
$PD_1$	Power Dissipation @ 50MHz with 50 $\Omega$ Thevenin Termination	15mW/Output 120mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$
$PD_2$	Power Dissipation @ 50MHz with 50 $\Omega$ Parallel Termination to GND	57mW/Output 456mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$

NOTE:  $PD_1$  and  $PD_2$  mW/Output numbers are for a 'Q' output.

### FREQUENCY SPECIFICATIONS ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , $V_{CC} = 5.0\text{V} \pm 5\%$ )

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN160	
f <sub>max</sub> <sup>1</sup>	Maximum Operating Frequency (2X_Q Output)	160	MHz
	Maximum Operating Frequency (Q0–Q4, Q <sub>5</sub> Output)	80	MHz

- Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 $\Omega$  terminated to  $V_{CC}/2$ .

**MC88915TFN160** (continued)**AC CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ , Load =  $50\Omega$  Terminated to  $V_{CC}/2$ )

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between $0.2V_{CC}$ and $0.8V_{CC}$ )	1.0	2.5	ns	Into a $50\Omega$ Load Terminated to $V_{CC}/2$
$t_{RISE/FALL}$ $2X\_Q$ Output	Rise/Fall Time	0.5	1.6	ns	$t_{RISE}$ : $0.8\text{V} - 2.0\text{V}$ $t_{FALL}$ : $2.0\text{V} - 0.8\text{V}$
$t_{PULSE\ WIDTH}$ ( $Q0-Q4$ , $Q5$ , $Q/2$ )	Output Pulse Width: $Q0$ , $Q1$ , $Q2$ , $Q3$ , $Q4$ , $Q5$ , $Q/2$ @ $V_{CC}/2$	$0.5t_{CYCLE} - 0.5^2$	$0.5t_{CYCLE} + 0.5^2$	ns	Into a $50\Omega$ Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ ( $2X\_Q$ Output)	Output Pulse Width: $2X\_Q$ @ $V_{CC}$ 80MHz 100MHz 133MHz 160MHz	$0.5t_{CYCLE} - 0.7$ $0.5t_{CYCLE} - 0.5$ $0.5t_{CYCLE} - 0.5$ TBD	$0.5t_{CYCLE} + 0.7$ $0.5t_{CYCLE} + 0.5$ $0.5t_{CYCLE} + 0.5$ TBD	ns	
$t_{PD}^1$ SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins) 133MHz 160MHz	(With $1M\Omega$ from RC1 to An $V_{CC}$ )		ns	See Note 2 and Figure 2 for Detailed Explanation
		-1.05 -0.9	-0.25 -0.10		
$t_{CYCLE}$ ( $2x\_Q$ Output)	Cycle-to-Cycle Variation 133MHz 160MHz	$t_{CYCLE} - 300\text{ps}$ $t_{CYCLE} - 300\text{ps}$	$t_{CYCLE} + 300\text{ps}$ $t_{CYCLE} + 300\text{ps}$		
$t_{SKEW}^3$ (Rising) See Note 4	Output-to-Output Skew Between Out- puts $Q0-Q4$ , $Q/2$ (Rising Edges Only)	—	500	ps	All Outputs Into a Matched $50\Omega$ Load Terminated to $V_{CC}/2$
$t_{SKEW}^3$ (Falling)	Output-to-Output Skew Between Out- puts $Q0-Q4$ (Falling Edges Only)	—	500	ps	All Outputs Into a Matched $50\Omega$ Load Terminated to $V_{CC}/2$
$t_{SKEW}^3$	Output-to-Output Skew $2X\_Q$ , $Q/2$ , $Q0-Q4$ Rising, $Q5$ Falling	—	750	ps	All Outputs Into a Matched $50\Omega$ Load Terminated to $V_{CC}/2$
$t_{LOCK}^4$	Time Required to Acquire Phase-Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
$t_{PZL}^5$	Output Enable Time $\overline{OE}/\overline{RST}$ to $2X\_Q$ , $Q0-Q4$ , $Q5$ , and $Q/2$	3.0	14	ns	Measured With the PLL_EN Pin Low
$t_{PHZ}, t_{PLZ}^5$	Output Disable Time $\overline{OE}/\overline{RST}$ to $2X\_Q$ , $Q0-Q4$ , $Q5$ , and $Q/2$	3.0	14	ns	Measured With the PLL_EN Pin Low

1.  $t_{CYCLE}$  in this spec is 1/Frequency at which the particular output is running.

2. The  $t_{PD}$  specification's min/max values may shift closer to zero if a larger pullup resistor is used.

3. Under equally loaded conditions and at a fixed temperature and voltage.

4. With  $V_{CC}$  fully powered-on, and an output properly connected to the FEEDBACK pin.  $t_{LOCK}$  maximum is with  $C1 = 0.1\mu\text{F}$ ,  $t_{LOCK}$  minimum is with  $C1 = 0.01\mu\text{F}$ .

5. The  $t_{PZL}$ ,  $t_{PHZ}$ ,  $t_{PLZ}$  minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

## Applications Information for All Versions

### General AC Specification Notes

- Several specifications can only be measured when the MC88915TFN55, 70 and 100 are in phase-locked operation. It is not possible to have the part in phase-lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88915TFN55, 70 and 100 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area, to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way all units passing the ATE test will meet or exceed the non-tested specifications limits.
- These two specs ( $t_{RISE/FALL}$  and  $t_{PULSE}$  Width  $2X\_Q$  output) guarantee that the MC88915T meets the 40MHz and 33MHz MC68040 P-Clock input specification (at 80MHz and 66MHz, respectively). For these two specs to be guaranteed by Motorola, the termination scheme shown below in Figure 1 must be used.
- The wiring Diagrams and explanations in Figure 5 demonstrate the input and output frequency relationships for three possible feedback configurations. The allowable SYNC input range for each case is also indicated. There are two allowable SYNC frequency ranges, depending whether  $FREQ\_SEL$  is high or low. Although not shown, it is possible to feed back the  $\overline{Q5}$  output, thus creating a 180° phase shift between the SYNC input and the "Q" outputs. Table 1 below summarizes the allowable SYNC frequency range for each possible configuration.

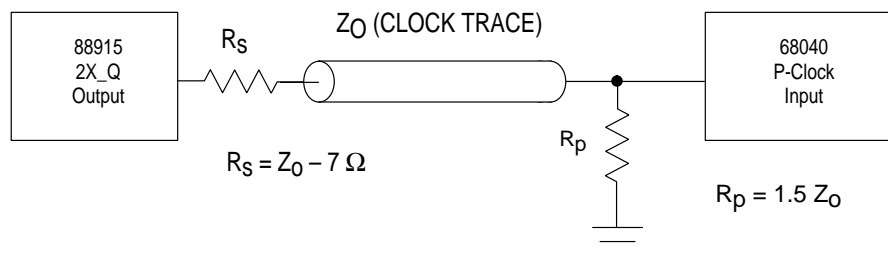


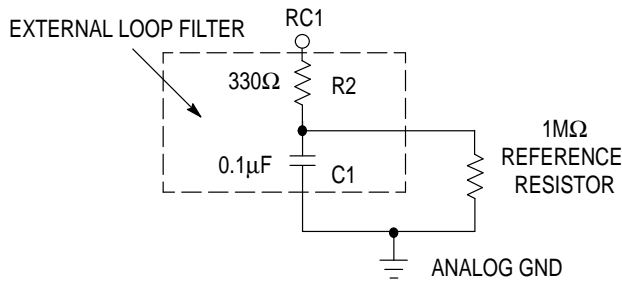
Figure 1. MC68040 P-Clock Input Termination Scheme

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHZ)	Corresponding VCO Frequency Range	Phase Relationships of the "Q" Outputs to Rising SYNC Edge
HIGH	Q/2	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
HIGH	Any "Q" (Q0-Q4)	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°
HIGH	$\overline{Q5}$	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	180°
HIGH	2X_Q	20 to (2X_Q FMAX Spec)	20 to (2X_Q FMAX Spec)	0°
LOW	Q/2	2.5 to (2X_Q FMAX Spec)/8	20 to (2X_Q FMAX Spec)	0°
LOW	Any "Q" (Q0-Q4)	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
LOW	$\overline{Q5}$	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	180°
LOW	2X_Q	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°

Table 1. Allowable SYNC Input Frequency Ranges for Different Feedback Configurations.

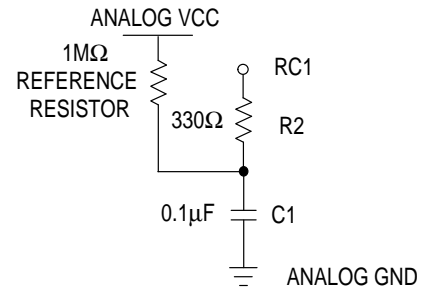
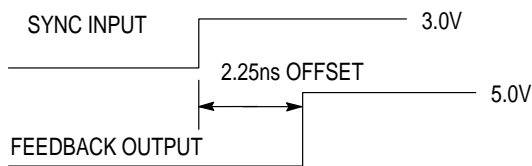
- A 1MΩ resistor tied to either Analog  $V_{CC}$  or Analog GND as shown in Figure 2 is required to ensure no jitter is present on the MC88915T outputs. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The  $t_{PD}$  spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for

the 14 lots described in note 1 while the part was in phase-locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V – 2.0V) with the Q/2 output fed back. The phase measurements were made at 1.5V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to  $V_{CC}$  and 100Ω to ground.



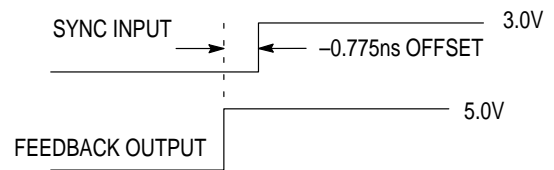
With the 1MΩ resistor tied in this fashion, the  $t_{PD}$  specification measured at the input pins is:

$$t_{PD} = 2.25\text{ns} \pm 1.0\text{ns}$$



With the 1MΩ resistor tied in this fashion, the  $t_{PD}$  specification measured at the input pins is:

$$t_{PD} = -0.775\text{ns} \pm 0.275\text{ns}$$



**Figure 2. Depiction of the Fixed SYNC to Feedback Offset ( $t_{PD}$ ) Which is Present When a 1MΩ Resistor is Tied to VCC or Ground**

5. The  $t_{SKEW_r}$  specification guarantees that the rising edges of outputs Q/2, Q0, Q1, Q2, Q3, and Q4 will always fall within a 500ps window within one part. However, if the relative position of each output within this window is not specified, the 500 ps window must be added to each side of the  $t_{PD}$  specification limits to calculate the total part-to-part skew. For this reason the absolute

distribution of these outputs are provided in table 2. When taking the skew data, Q0 was used as a reference, so all measurements are relative to this output. The information in Table 2 is derived from measurements taken from the 14 process lots described in Note 1, over the temperature and voltage range.

Output	– (ps)	+ (ps)
Q0	0	0
Q1	–72	40
Q2	–44	276
Q3	–40	255
Q4	–274	–34
Q/2	–16	250
2X_Q	–633	–35

**Table 2. Relative Positions of Outputs Q/2, Q0-Q4, 2X\_Q, Within the 500ps  $t_{SKEW_r}$  Spec Window**

## 6. Calculation of Total Output-to-Skew between multiple parts (Part-to-Part skew)

By combining the  $t_{PD}$  specification and the information in Note 5, the worst case output-to-output skew between multiple 88915's connected in parallel can be calculated. This calculation assumes that all parts have a common SYNC input clock with equal delay of that input signal to each part. This skew value is valid at the 88915 output pins only (equally loaded), it does not include PCB trace delays due to varying loads.

With a  $1M\Omega$  resistor tied to analog  $V_{CC}$  as shown in note 4, the  $t_{PD}$  spec. limits between SYNC and the Q/2 output (connected to the FEEDBACK pin) are  $-1.05ns$  and  $-0.5ns$ . To calculate the skew of any given output between two or more parts, the absolute value of the distribution of that output given in table 2 must be subtracted and added to the lower and upper  $t_{PD}$  spec limits respectively. For output Q2,  $[276 - (-44)] = 320ps$  is the absolute value of the distribution. Therefore

$[-1.05ns - 0.32ns] = -1.37ns$  is the lower  $t_{PD}$  limit, and  $[-0.5ns + 0.32ns] = -0.18ns$  is the upper limit. Therefore the worst case skew of output Q2 between any number of parts is  $|(-1.37) - (-0.18)| = 1.19ns$ . Q2 has the worst case skew distribution of any output, so  $1.2ns$  is the absolute worst case output-to-output skew between multiple parts.

7. Note 4 explains that the  $t_{PD}$  specification was measured and is guaranteed for the configuration of the Q/2 output connected to the FEEDBACK pin and the SYNC input running at 10MHz. The fixed offset ( $t_{PD}$ ) as described above has some dependence on the input frequency and at what frequency the VCO is running. The graphs of Figure 3 demonstrate this dependence.

The data presented in Figure 3 is from devices representing process extremes, and the measurements were also taken at the voltage extremes ( $V_{CC} = 5.25V$  and  $4.75V$ ). Therefore the data in Figure 3 is a realistic representation of the variation of  $t_{PD}$ .

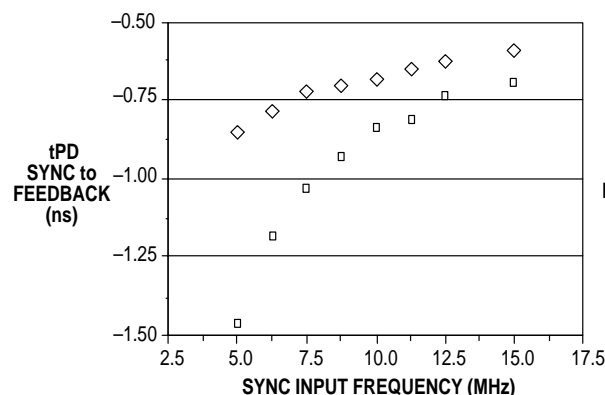


Figure 3a.

$t_{PD}$  versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @  $25^{\circ}C$  (With  $1M\Omega$  Resistor Tied to Analog  $V_{CC}$ )

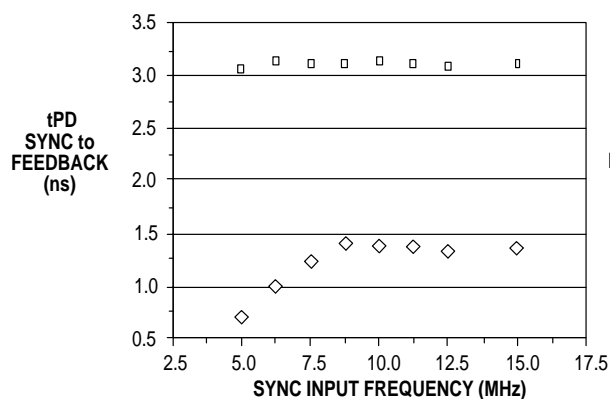


Figure 3c.

$t_{PD}$  versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @  $25^{\circ}C$  (With  $1M\Omega$  Resistor Tied to Analog GND)

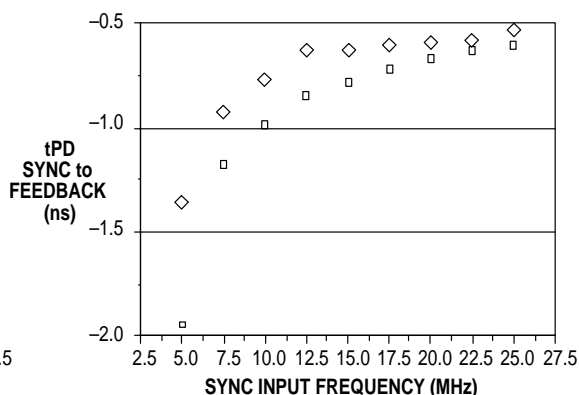


Figure 3b.

$t_{PD}$  versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @  $25^{\circ}C$  (With  $1M\Omega$  Resistor Tied to Analog  $V_{CC}$ )

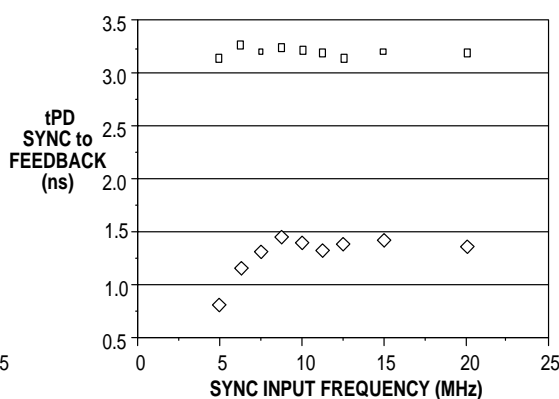
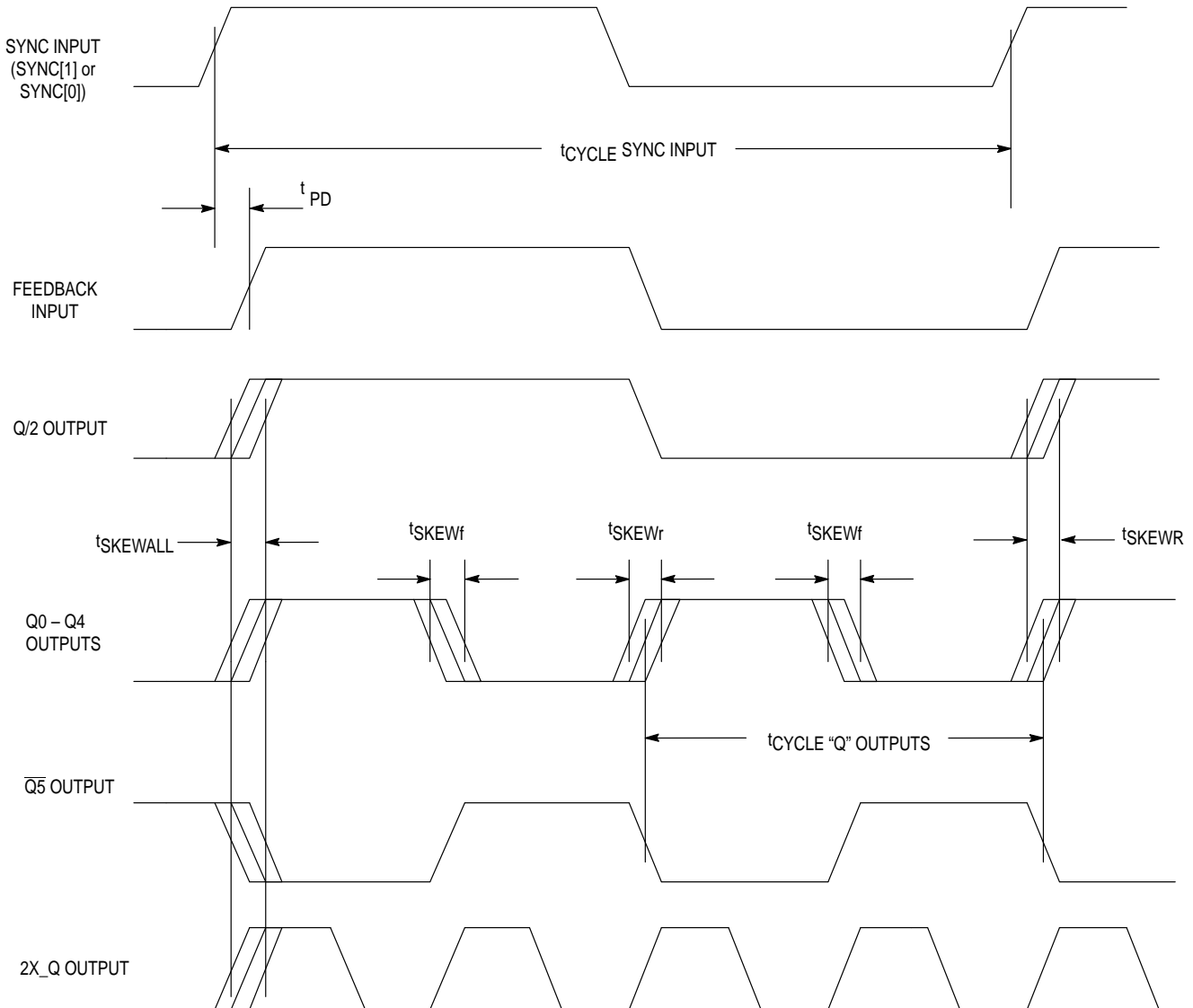


Figure 3d.

$t_{PD}$  versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @  $25^{\circ}C$  (With  $1M\Omega$  Resistor Tied to Analog GND)

8. The lock indicator pin (LOCK) will reliably indicate a phase-locked condition at SYNC input frequencies down to 10MHz. At frequencies below 10MHz, the frequency of correction pulses going into the phase detector from the SYNC and FEEDBACK pins may not be sufficient to allow the lock indicator circuitry to accurately predict a phase-locked condition. The MC88915T is guaranteed

to provide stable phase-locked operation down to the appropriate minimum input frequency given in Table 1, even though the LOCK pin may be LOW at frequencies below 10MHz. The exact minimum frequency where the lock indicator functionality can be guaranteed will be available when the MC88915T reaches 'MC' status.

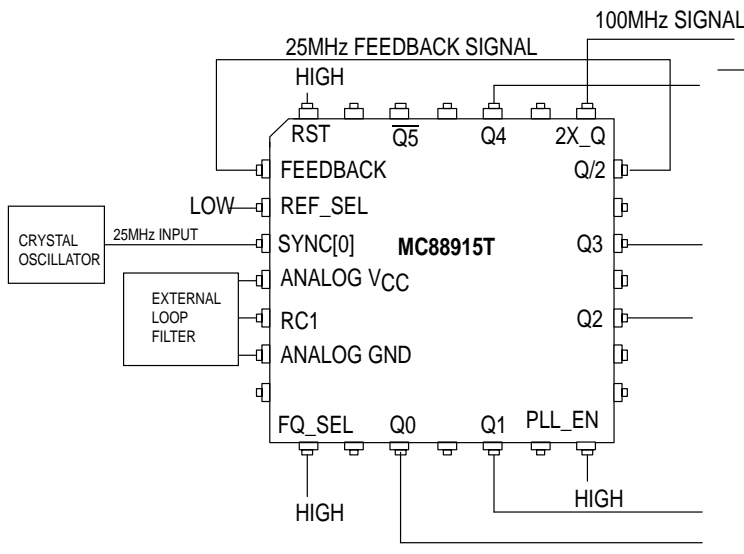


**Figure 4. Output/Input Switching Waveforms and Timing Diagrams**

(These waveforms represent the hook-up configuration of Figure 5a on page 16)

#### Timing Notes:

- The MC88915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
- All skew specs are measured between the  $V_{CC}/2$  crossing point of the appropriate output edges. All skews are specified as 'windows', not as a  $\pm$  deviation around a center point.
- If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X\_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.



### 1:2 Input to "Q" Output Frequency Relationship

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0–Q4, Q5) will always run at 2X the Q/2 frequency, and the 2X\_Q output will run at 4X the Q/2 frequency.

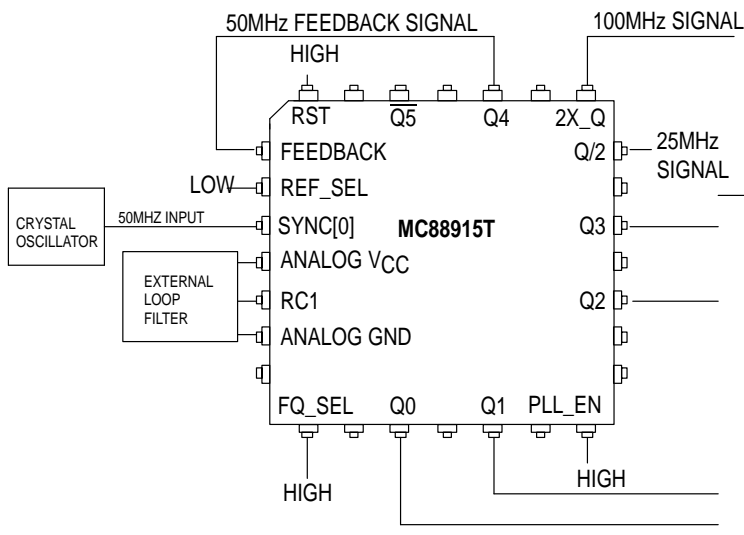
50MHz  
"Q"  
CLOCK  
OUTPUTS

#### Allowable Input Frequency Range:

**5MHz to (2X\_Q FMAX Spec)/4** (for FREQ\_SEL HIGH)  
**2.5MHz to (2X\_Q FMAX Spec)/8** (for FREQ\_SEL LOW)

Note: If the  $\overline{OE}/\overline{RST}$  input is active, a pull-up or pull-down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3-state.

**Figure 5a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back**



### 1:1 Input to "Q" Output Frequency Relationship

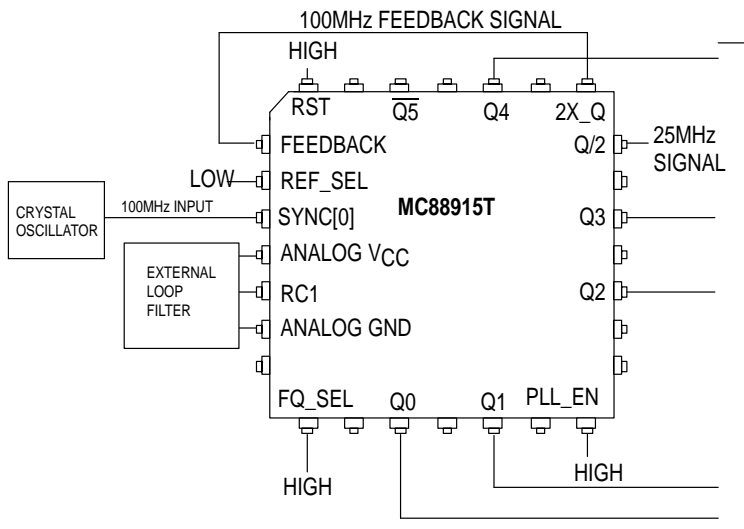
In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the "Q" frequency, and the 2X\_Q output will run at 2X the "Q" frequency.

50MHz  
"Q"  
CLOCK  
OUTPUTS

#### Allowable Input Frequency Range:

**10MHz to (2X\_Q FMAX Spec)/2** (for FREQ\_SEL HIGH)  
**5MHz to (2X\_Q FMAX Spec)/4** (for FREQ\_SEL LOW)

**Figure 5b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back**



### 2:1 Input to "Q" Output Frequency Relationship

In this application, the 2X\_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X\_Q and SYNC, thus the 2X\_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X\_Q frequency, and the "Q" outputs will run at 1/2 the 2X\_Q frequency.

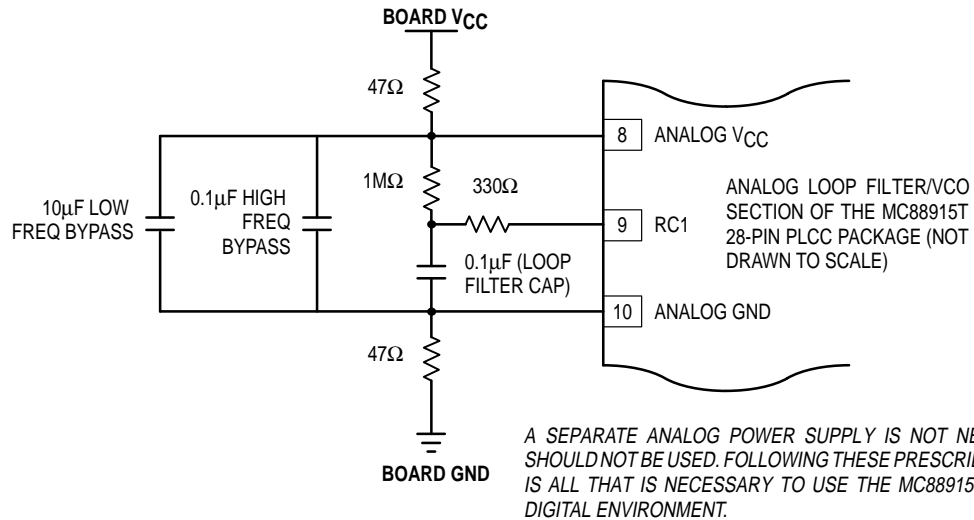
50MHz  
"Q"  
CLOCK  
OUTPUTS

#### Allowable Input Frequency Range:

**20MHz to (2X\_Q FMAX Spec)** (for FREQ\_SEL HIGH)  
**10MHz to (2X\_Q FMAX Spec)/2** (for FREQ\_SEL LOW)

**Figure 5c. Wiring Diagram and Frequency Relationships with 2X\_Q Output Feed Back**





**Figure 6. Recommended Loop Filter and Analog Isolation Scheme for the MC88915T**

### Notes Concerning Loop Filter and Board Layout Issues

1. Figure 6 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88915T's sensitivity to voltage transients from the system digital V<sub>CC</sub> supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V<sub>CC</sub> supply will cause no more than a 100pS phase deviation on the 88915T outputs. A 250mV step deviation on V<sub>CC</sub> using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V<sub>CC</sub> step should cause no more than a 100pS phase deviation.

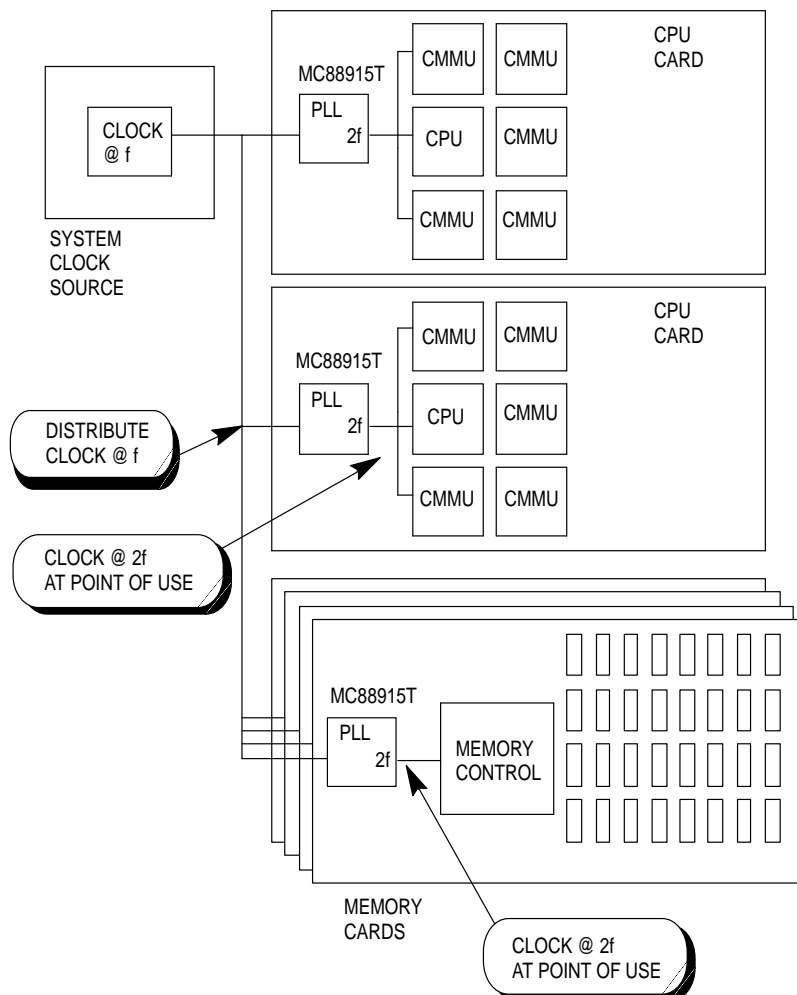
If good bypass techniques are used on a board design near components which may cause digital V<sub>CC</sub> and ground noise, the above described V<sub>CC</sub> step deviations should not occur at the 88915T's digital V<sub>CC</sub> supply. The

purpose of the bypass filtering scheme shown in Figure 6 is to give the 88915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1MΩ and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead-band. If the VCO (2X\_Q output) is running above 40MHz, the 1MΩ resistor provides the correct amount of current injection into the charge pump (2–3μA). For the TFN55, 70 or 100, if the VCO is running below 40MHz, a 1.5MΩ reference resistor should be used (instead of 1MΩ).

2. In addition to the bypass capacitors used in the analog filter of Figure 6, there should be a 0.1μF bypass capacitor between each of the other (digital) four V<sub>CC</sub> pins and the board ground plane. This will reduce output switching noise caused by the 88915T outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88915T package as possible.



**Figure 7. Representation of a Potential Multi-Processing Application Utilizing the MC88915T for Frequency Multiplication and Low Board-to-Board Skew**

### MC88915T System Level Testing Functionality

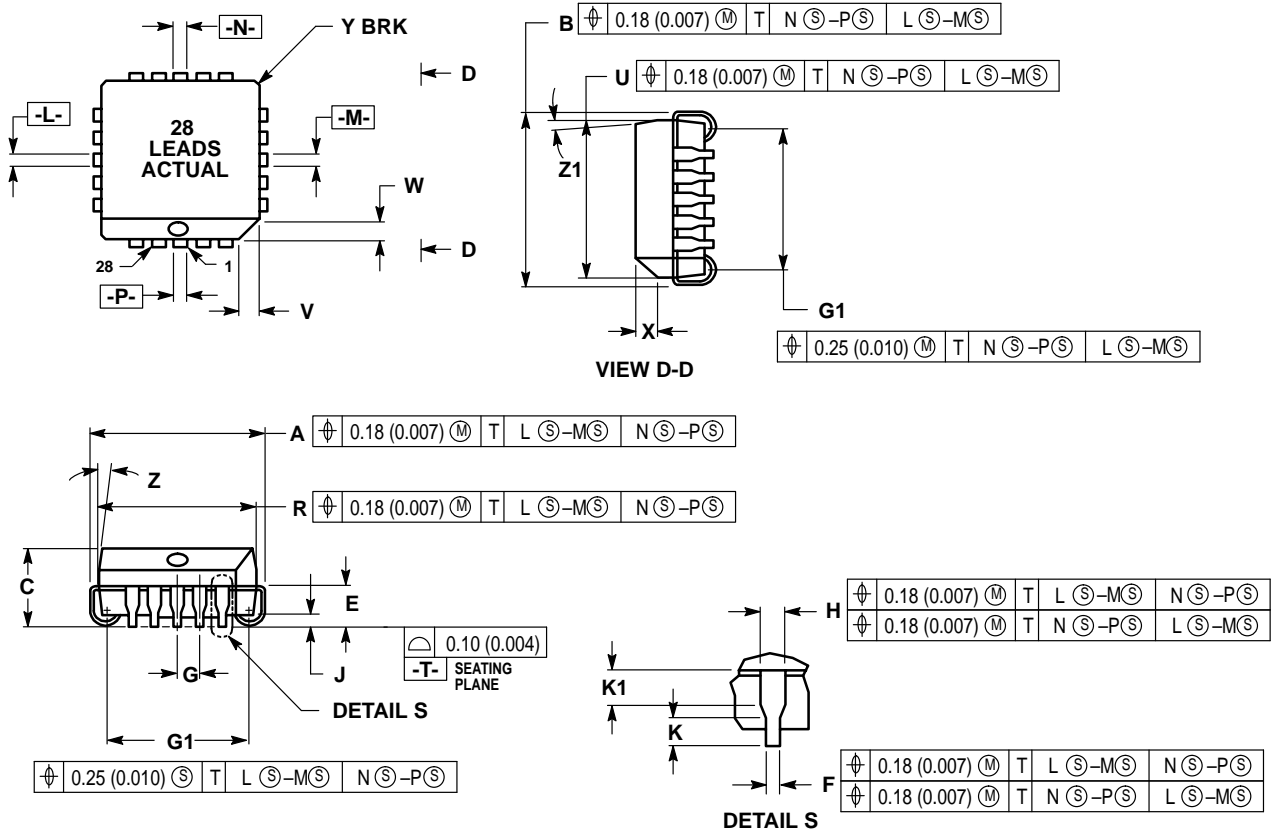
3-state functionality has been added to the 100MHz version of the MC88915T to ease system board testing. Bringing the  $\overline{OE}/RST$  pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL\_EN pin is low, the Q0–Q4, Q5, and the Q/2 outputs will remain reset in the low state after the  $\overline{OE}/RST$  until a falling SYNC edge is seen. The 2X\_Q output will be the inverse of the SYNC signal in this mode. If the 3-state functionality will be used, a pull-up or pull-down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the feedback output goes into high impedance.

With the PLL\_EN pin low the selected SYNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3-state during normal PLL operation, the loop will be broken and phase-lock will be lost. It will take a maximum of 10mS (tLOCK spec) to regain phase-lock after the  $\overline{OE}/RST$  pin goes back high.


## OUTLINE DIMENSIONS

FN SUFFIX  
PLASTIC PACKAGE  
CASE 776-02  
ISSUE D



## NOTES:

1. DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. 776-01 IS OBSOLETE, NEW STANDARD 776-02.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**Literature Distribution Centers:**

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.

ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

