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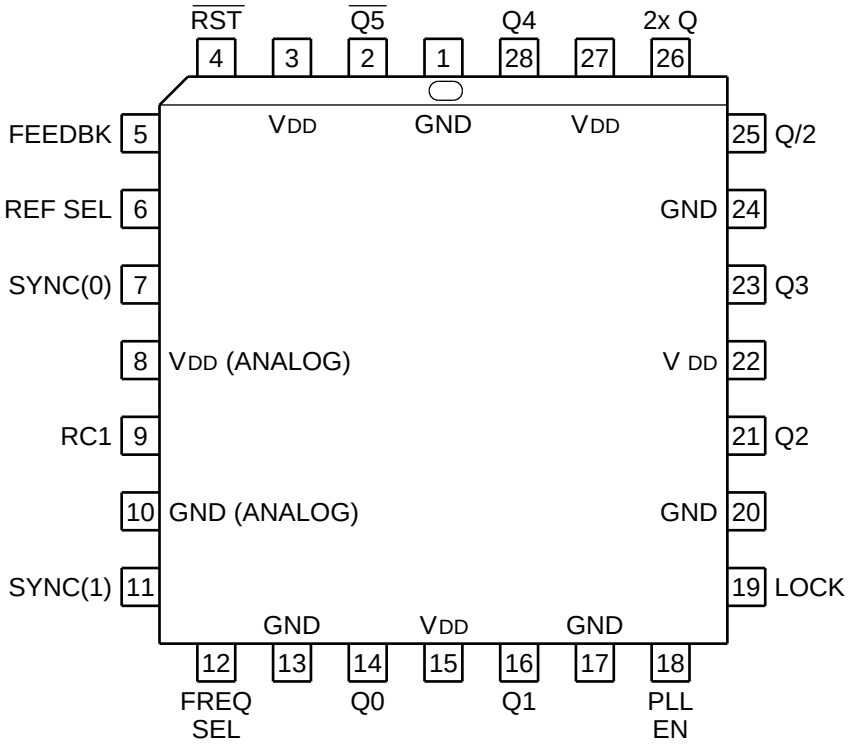
IL08

C-MOS LOW SKEW PLL CLOCK DRIVER

- TOP VIEW -

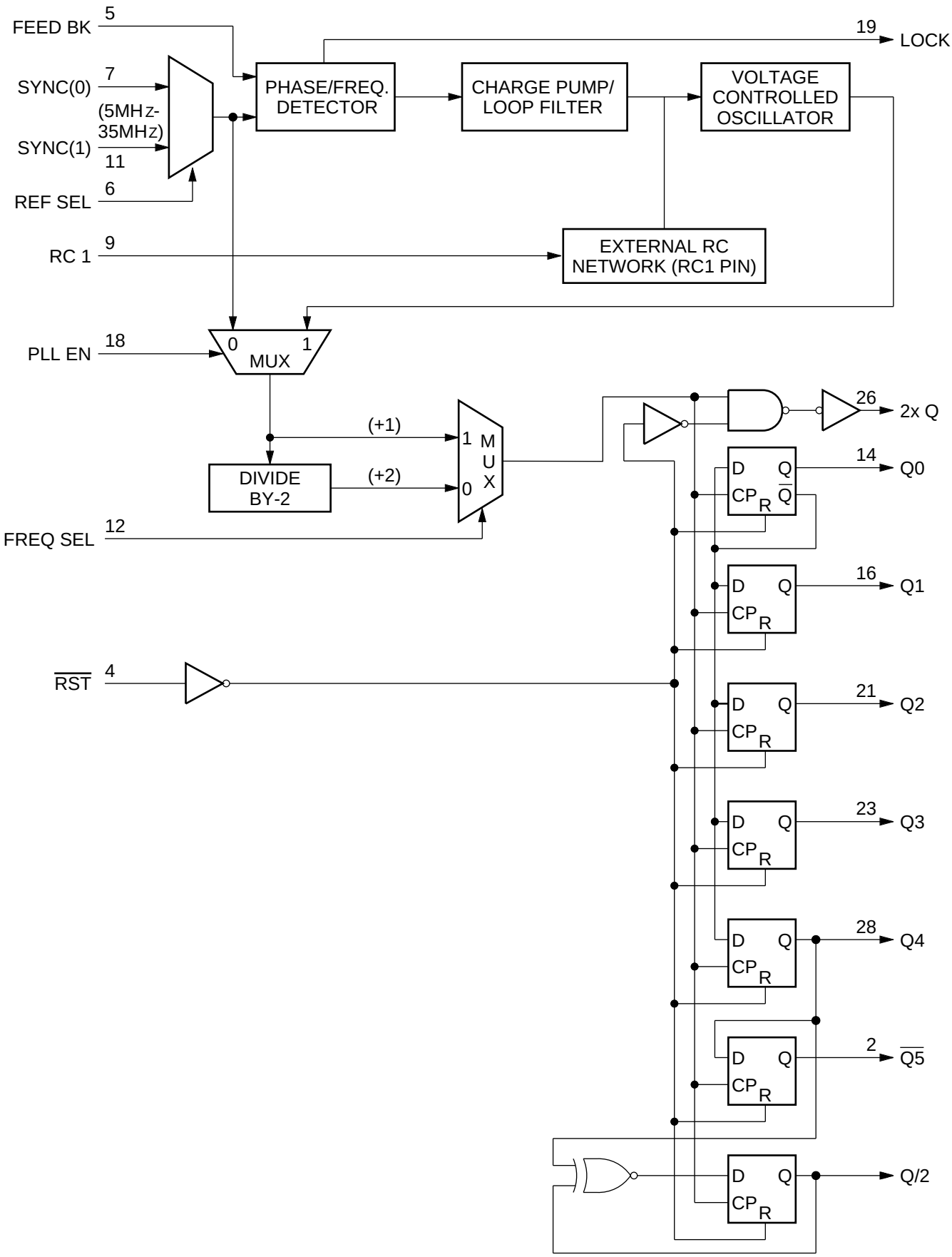


INPUT

FEEDBK	; FEEDBACK TO PHASE DETECTOR FROM Q
FREQ SEL	; SELECTS Q OUTPUT FREQUENCY (MUST MATCH SYNC)
PLL EN	; DISABLES PHASE-LOCK FOR LOW FREQUENCY TESTING
RC1	; INPUT FOR EXTERNAL RC NETWORK
REF SEL	; CHOOSES REFERENCE BETWEEN SYNC (0) & SYNC (1)
$\overline{\text{RST}}$	; ASYNCHRONOUS RESET (ACTIVE LOW)
SYNC (0),(1)	; REFERENCE CLOCK INPUT

OUTPUT

Q /2	; CLOCK OUTPUT (Q) FREQUENCY +2 (SYNCHRONOUS)
2x Q	; 2x CLOCK OUTPUT (Q) FREQUENCY (SYNCHRONOUS)
LOCK	; INDICATES PHASE LOCK HAS BEEN ACHIEVED
Q (0-4)	; CLOCK OUTPUT (LOCKED TO SYNC)
$\overline{\text{Q5}}$	; INVERSE OF CLOCK OUTPUT (LOCKED TO SYNC)


FEED BK
5
19
LOCK
SYNC(0)
7
(5MHz-
35MHz)
SYNC(1)
11
REF SEL
6
PHASE/FREQ.
DETECTOR
CHARGE PUMP/
LOOP FILTER
VOLTAGE
CONTROLLED
OSCILLATOR
RC 1
9
EXTERNAL RC
NETWORK (RC1 PIN)
PLL EN
18
0
MUX
1
(+1)
(+2)
DIVIDE
BY-2
1
M
U
X
0
FREQ SEL
12
26
2x Q
14
Q0
16
Q1
RST
4
21
Q2
23
Q3
28
Q4
2
Q5
Q/2
D
Q
CP
R