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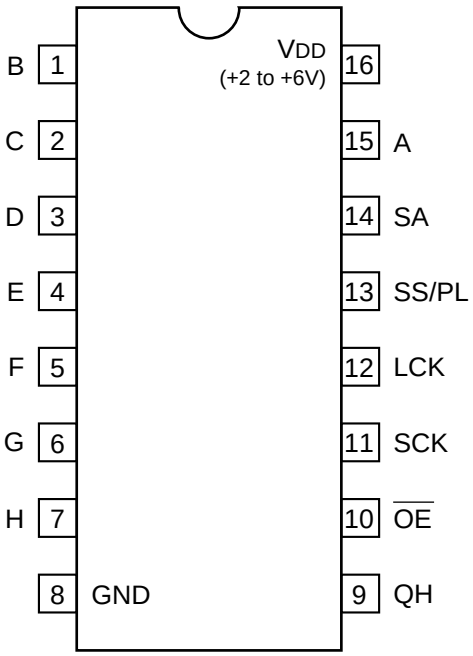
C-MOS 8-BIT SERIAL OR PARALLEL INPUT/SERIAL OUTPUT SHIFT REGISTER WITH 3-STATE OUTPUT

—TOP VIEW—

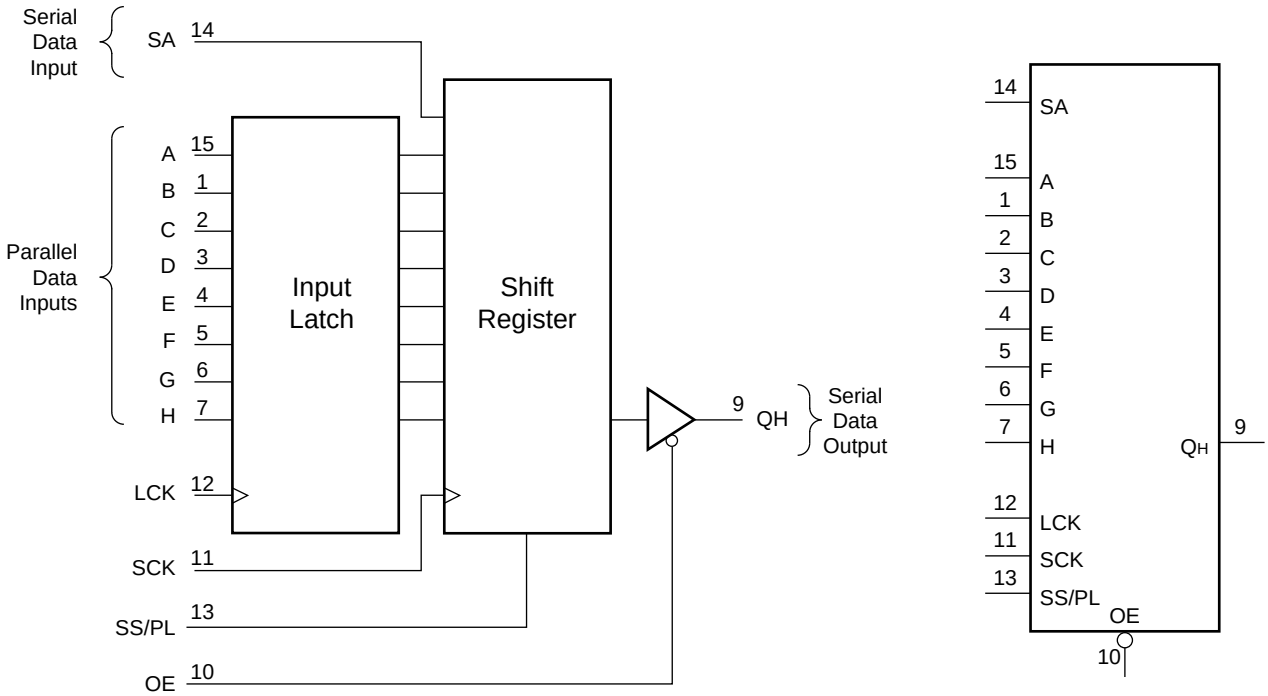


A-H ; PARALLEL DATA INPUTS
LCK ; LATCH CLOCK INPUT
$\overline{OE}$; OUTPUT ENABLE INPUT
QH ; SERIAL DATA OUTPUT
SA ; SERIAL DATA INPUT
SCK ; SHIFT CLOCK INPUT
SS/PL ; SERIAL SHIFT/PARALLEL LOAD

FUNCTION TABLE

INPUTS						OUTPUT QH	RESULTING FUNCTION
OUTPUT ENABLE	SERIAL SHIFT PARALLEL LOAD	LATCH CLOCK	SHIFT CLOCK	SA	A-H		
H	X	X	X	X	X	Z	QH is in the high impedance state.
L	H	⎍	L, H, ⎎	X	a-h	no change	Parallel data is stored in the input latch. The state of the shift register is unaffected.
L	L	⎍	X	X	a-h	h	Parallel data is stored in the input latch and loaded into the shift register.
L	L	L, H, ⎎	L, H, ⎎	X	X	h_L*	Parallel data is stored in the input latch and loaded into the shift register.
L L	H H	X X	⎍ ⎍	L H	X X	Q_{GN} Q_{GN}	A low logic level is shifted into the shift register. A high logic level is shifted into the shift register.
L	H	⎍	⎍	L, H	L, H	Q_{GN}	Serial data is shifted into the shift register and parallel data is stored in the input latch.

* h_L = the data stored in stage H of the input latch
X = don't care
Q_{GN} = Data shifted from stage G
a-h = Data at inputs A-H, respectively
Z = High Impedance State


Serial
Data
Input
SA
14
Parallel
Data
Inputs
A
15
B
1
C
2
D
3
E
4
F
5
G
6
H
7
Input
Latch
Shift
Register
9
QH
Serial
Data
Output
LCK
12
SCK
11
SS/PL
13
OE
10
14
SA
15
A
1
B
2
C
3
D
4
E
5
F
6
G
7
H
9
QH
12
LCK
11
SCK
13
SS/PL
OE
10