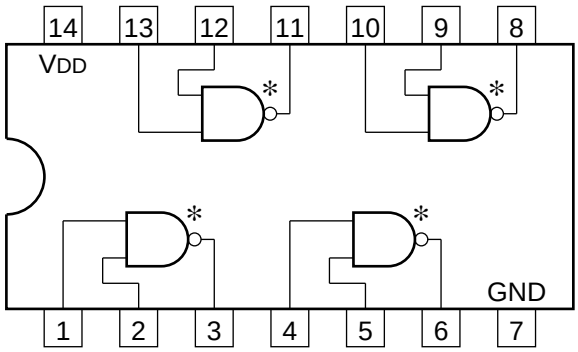
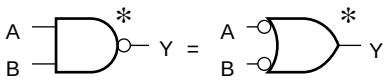
C-MOS QUAD 2-INPUT POSITIVE-NAND GATE WITH OPEN-DRAIN

—TOP VIEW—





$Y = \overline{A \bullet B} = \overline{A} + \overline{B}$

A	B	Y
0	0	HI-Z
0	1	HI-Z
1	0	HI-Z
1	1	0

0 : LOW LEVEL
1 : HIGH LEVEL
HI-Z : HIGH IMPEDANCE