MOTOROLA

MC74F657A,B

OCTAL BIDIRECTIONAL TRANSCEIVER WITH 8-BIT PARITY GENERATOR CHECKER (3-STATE OUTPUTS)

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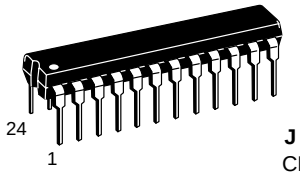
FAST™ SCHOTTKY TTL

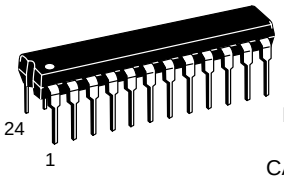
The MC74F657A and MC74F657B are Octal Bidirectional Transceivers with an 8-bit parity Generator/Checker and 3-state outputs.

The A and B options are faster versions of the F657 and contain eight non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker. These devices are intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA at the A ports and 64 mA at the B ports. The Transmit/Receiver ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports.

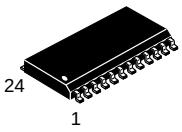
- High-Impedance NPN Base Input for Reduced Loading (20 μA in HIGH and LOW States)
- Ideal in Applications Where High Output Drive and Light Bus Loading are Required (I_{IL} is 20 μA versus Fast std of 600 μA)
- Combines F245 and F280A Functions in One Package
- 3-State Outputs
- B Outputs, PARITY, $\overline{ERROR}$, Sink 64 mA and Source 15 mA
- 15 mA Source Current
- Input Diodes for Termination Effects
- Glitchless Outputs During Power Up and Power Down
- High Impedance Outputs During Power Off
- ESD Protection > 4000 Volts



J SUFFIX
CERAMIC
CASE 758-01



N SUFFIX
PLASTIC
CASE 724-03

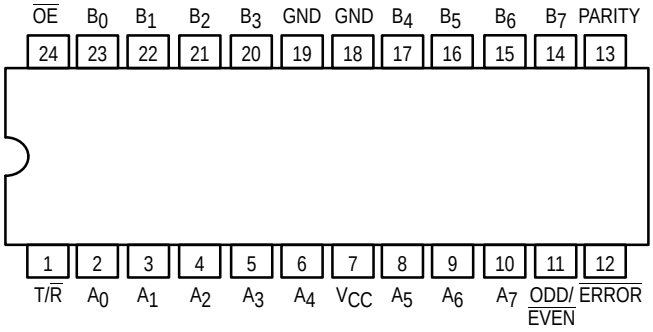


DW SUFFIX
SOIC
CASE 751E-03

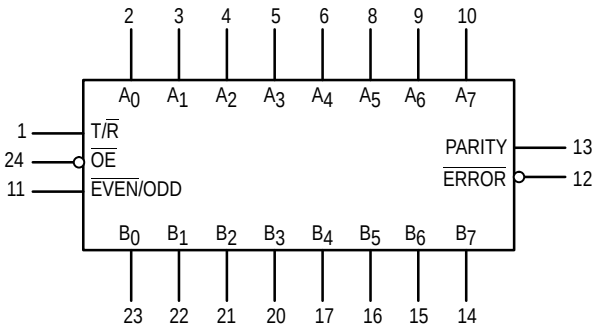
ORDERING INFORMATION

MC74FXXXAJ/BJ	Ceramic
MC74FXXXAN/BN	Plastic
MC74FXXXADW/BDW	SOIC

PIN ASSIGNMENT



LOGIC SYMBOL



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			–3.0/–15	mA
I_{OL}	Output Current — Low	74			24/64	mA

FUNCTION TABLE

Number of Inputs That are High	Inputs			Input/Output	Outputs	
	OE	T/$\overline{R}$	$\overline{Even}$/Odd	Parity	Error	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive

Number of Inputs That are High	Inputs			Input/Output	Outputs	
	OE	T/$\overline{R}$	$\overline{Even}$/Odd	Parity	Error	Outputs Mode
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't Care	H	X	X	Z	Z	Z

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = HIGH impedance state.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter			Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage			2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage					0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–0.73	–1.2	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	All Outputs	74	2.4			V	I_{OH} = –3.0 mA	V_{CC} = 4.5 V
				2.7	3.4				V_{CC} = 4.75 V
		B0–B7 PARITY, $\overline{ERROR}$	74	2.0			V	I_{OH} = –15 mA	V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	A0–A7	74		0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
		B0–B7 PARITY, $\overline{ERROR}$	74		0.4	0.55	V	I_{OL} = 64 mA	
I_{IH}	Input HIGH Current	T/$\overline{R}$, $\overline{OE}$, $\overline{EVEN}$/ODD				100	µA	V_{CC} = 0 V, V_{IN} = 7.0 V	
		A0–A7				2.0	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V	
		B0–B7, PARITY				1.0		V_{CC} = 5.5 V, V_{IN} = 5.5 V	
		$\overline{EVEN}$/ODD				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		T/$\overline{R}$, $\overline{OE}$				40			
I_{IL}	Input LOW Current	$\overline{EVEN}$/ODD				–20	µA	V_{CC} = MAX, V_{IN} = 0.5 V	
		T/$\overline{R}$, $\overline{OE}$				–40			
I_{IH} + I_{OZH}	Off-State Current HIGH Level Voltage Applied	A0–A7 B0–B7 PARITY				70	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{IL} + I_{OZL}	Off-State Current LOW Level Voltage Applied					–70		V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OZH}	Off-State Output Current, High-Level Voltage Applied	$\overline{ERROR}$				50	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied					–50		V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)	A_n Outputs		–60		–150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
		PARITY, B_n Outputs, $\overline{ERROR}$		–100		–225			
I_{CC}	Total Supply Current	I_{CCH}			90	135	mA	V_{CC} = MAX	
		I_{CCL}			106	150			
		I_{CCZ}			98	145			

NOTES:
1. For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at one time, nor for more than 1 second.

F657A
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			74F $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0$ V $\pm$ 10% $C_L = 50$ pF		Unit
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	2.0 2.0		7.0 7.0	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to PARITY	6.0 6.5		13 13	5.5 6.5	14 14	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{EVEN}$/ODD to PARITY, $\overline{ERROR}$	4.5 4.5		10.5 10.5	4.5 4.5	11 11.5	ns
t_{PLH} t_{PHL}	Propagation Delay B_n to $\overline{ERROR}$	7.0 7.0		18 18	6.5 6.5	19 19	ns
t_{PLH} t_{PHL}	Propagation Delay PARITY to $\overline{ERROR}$	8.0 7.0		14 14	7.0 7.0	15 15	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH or LOW Level	3.0 4.0		8.0 9.0	3.0 4.0	9.0 10	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH or LOW Level	2.0 2.0		7.5 6.0	2.0 2.0	8.0 6.5	ns

F657B
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			74F $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0$ V $\pm$ 10% $C_L = 50$ pF		Unit
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	2.0 2.0		6.0 6.0	2.0 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to PARITY	4.5 4.5		11.5 11.5	4.5 4.5	13 13	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{EVEN}$/ODD to PARITY, $\overline{ERROR}$	2.0 2.0		7.5 7.5	2.0 2.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay B_n to $\overline{ERROR}$	4.0 4.0		15 15	3.5 3.5	16 16	ns
t_{PLH} t_{PHL}	Propagation Delay PARITY to $\overline{ERROR}$	5.0 5.0		11 11	4.0 4.0	12 12	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH or LOW Level	2.0 2.0		7.0 7.0	2.0 2.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH or LOW Level	2.0 2.0		6.0 6.0	2.0 2.0	6.5 6.5	ns

LOGIC DIAGRAM