MOTOROLA

MC74F195

4-BIT PARALLEL ACCESS SHIFT REGISTER

The functional characteristics of the MC74F195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting, and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

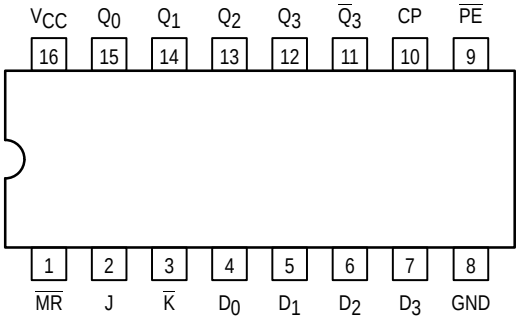
The MC74F195 operates in two primary modes, shift right (Q_0-Q_1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted 1 bit in the direction Q_0-Q_1-Q_2-Q_3 following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the J$\overline{K}$ type input is made for special applications, and by tying the two pins together the simple D-type input is made for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0-D_3) is transferred to the respective Q_0-Q_3 outputs. Shift left operation (Q_3-Q_2) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The MC74F195 utilizes edge-triggering; therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the setup and hold time requirements.

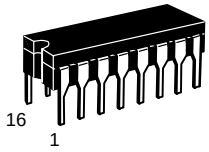
A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

- Shift Right and Parallel Load Capability
- J-$\overline{K}$ (D-Type) Inputs to First Stage
- Complement Output from Last Stage
- Asynchronous Master Reset

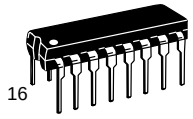
CONNECTION DIAGRAM DIP



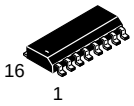
4-BIT PARALLEL ACCESS SHIFT REGISTER
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

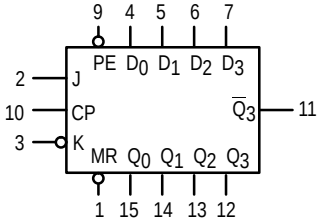


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL

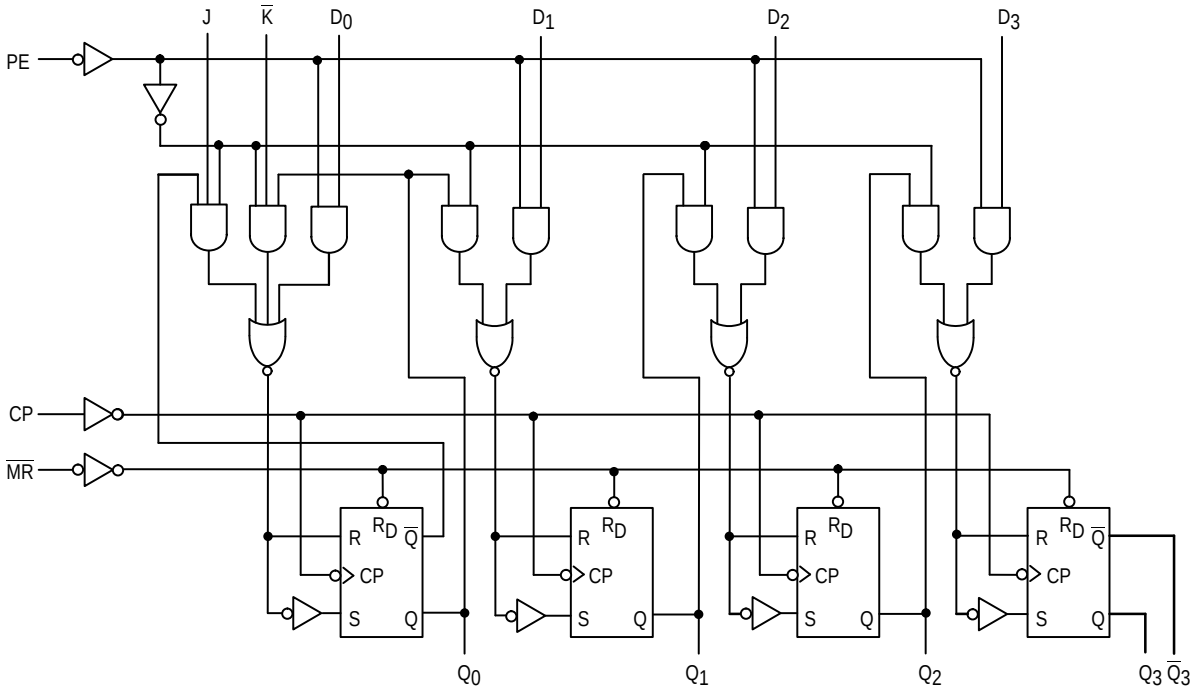


V_{CC} = PIN 16
GND = PIN 8

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			–1.0	mA
I_{OL}	Output Current — Low	74			20	mA

LOGIC DIAGRAM



FUNCTION TABLE

Operating Modes	Inputs						Outputs				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	I_{IN} = –18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	74	2.5			V	I_{OH} = –1.0 mA	V_{CC} = 4.5 V
		74	2.7			V		V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = 4.5 V
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				–0.6	mA	V_{CC} = MAX	
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current				38	mA	V_{CC} = MAX	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F T_A = + 25°C, V_{CC} = + 5.0 V, C_L = 50 pF Min	54/74F Max	74F T_A = 0°C to + 70°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF Min	74F Max	Unit
f_{max}		105		90		MHz
t_{PLH}	Propagation Delay	2.5	7.0	2.5	8.0	ns
t_{PHL}	CP to Q/$\overline{Q}$	2.5	8.0	2.5	9.0	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q	3.0	10	3.0	11	ns
t_{PLH}	Propagation Delay, $\overline{MR}$ to $\overline{Q}$	3.0	10.5	3.0	11	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F T_A = + 25°C V_{CC} = + 5.0 V C_L = 50 pF		74F T_A = 0°C to + 70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		Unit
		Min	Max	Min	Max	
t_s (H)	Setup Time, HIGH or LOW J, K, D to CP	4.0		4.0		ns
t_s (L)		4.0		4.0		
t_h (H)	Hold Time, HIGH or LOW J, K, D to CP	0		1.0		ns
t_h (L)		0		1.0		
t_s (H)	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0		9.0		ns
t_s (L)		8.0		9.0		
t_h (H)	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0		0		ns
t_h (L)		0		0		
t_w (H)	CP Pulse Width, HIGH	5.0		5.5		ns
t_w (L)	$\overline{MR}$ Pulse Width, LOW	5.0		5.0		ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	7.0		8.0		ns