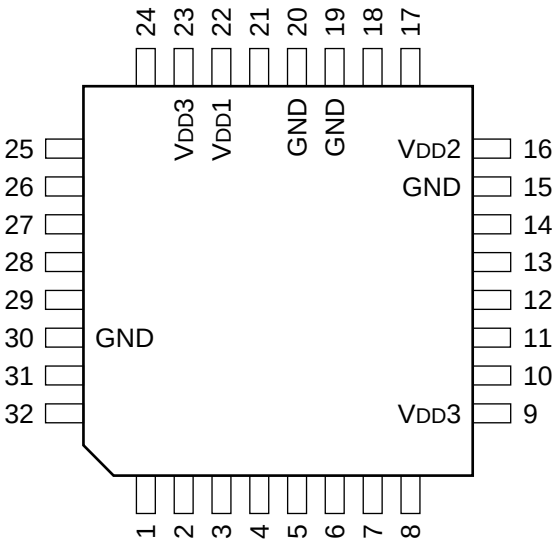
C-MOS 8-BIT MICRO CONTROLLER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	AD0/SCLK	9	—	$V_{DD}3$	17	I	$\overline{SYNC}$	25	I/O	PLLTD
2	I/O	AD1/SDATA	10	I	SDI/AS	18	I	VDATA	26	I	TEST
3	I/O	AD2/SWIN	11	I/O	SDO/$\overline{RW}$	19	—	GND	27	I	PAR/$\overline{SER}$
4	I/O	AD3	12	I	$\overline{SCK}$/E	20	—	GND	28	I	$\overline{RESET}$
5	I/O	AD4	13	I	$\overline{CS}$	21	I	XFC	29	O	BUSY
6	I/O	AD5	14	I	CSA	22	—	$V_{DD}1$	30	—	GND
7	I/O	AD6	15	—	GND	23	—	$V_{DD}3$	31	I	OSC1
8	I/O	AD7	16	—	$V_{DD}2$	24	I/O	PLLTA	32	O	OSC2

INPUT

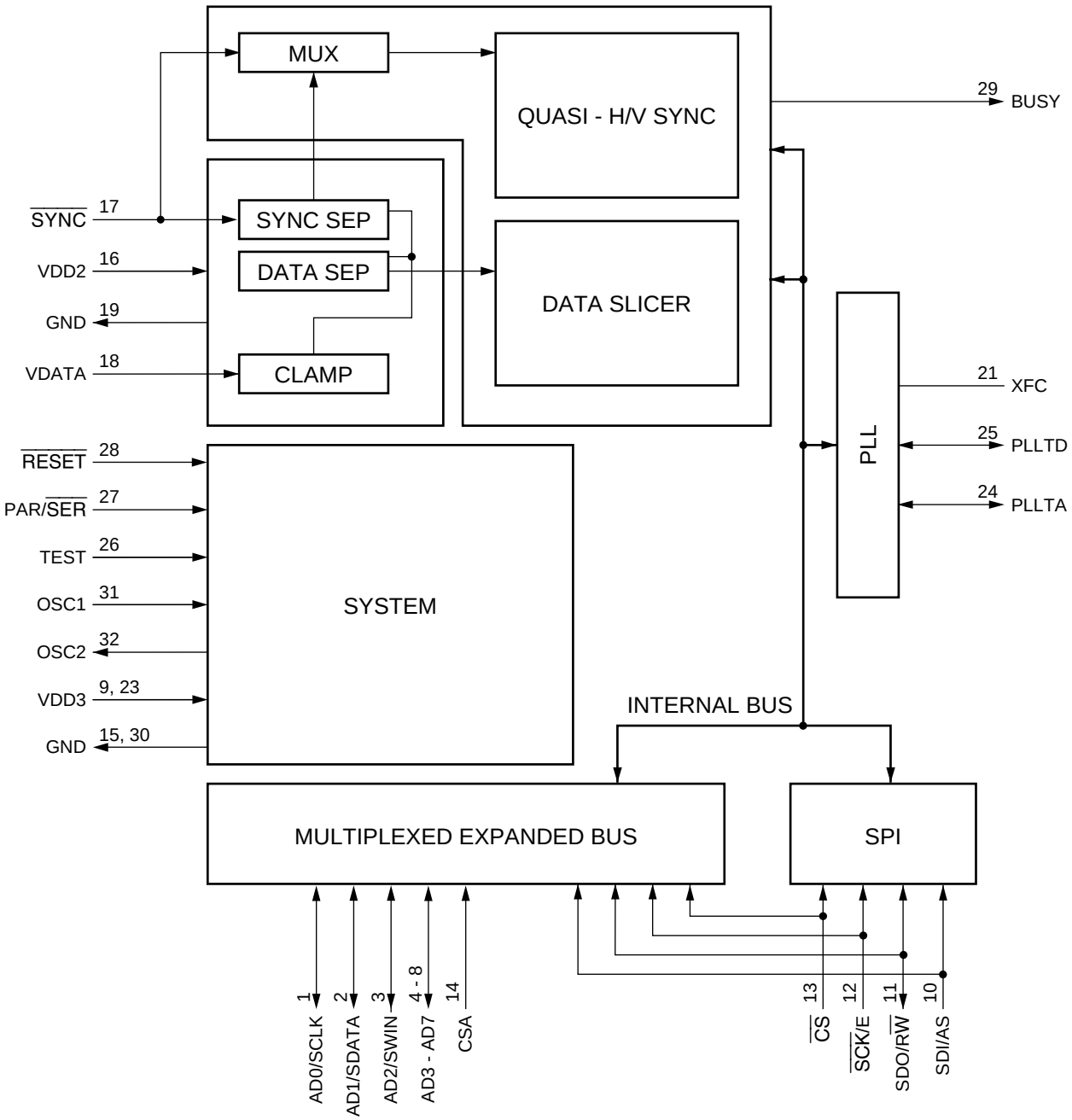
AD0 - AD7 : ADDRESS/DATA BUS
AS : EXPANDED INTERFACE ADDRESS STROBE
$\overline{CS}$: CHIP SELECT
CSA : ALTERNATE CHIP SELECT
E : EXTERNAL PULL-UP RESISTOR CONNECTION
OSC1 : OSCILLATOR
PAR/$\overline{SER}$: EXPANDED INTERFACE/SERIAL COMMUNICATION INTERFACE
RESET : RESET
$\overline{SCK}$: CLOCK
SDI : SERIAL COMMUNICATION DATA
$\overline{SYNC}$: SYNCHRONIZATION SIGNAL
TEST : (FOR TEST)
VDATA : VIDEO SIGNAL
XFC : EXTERNAL PASSIVE COMPONENTS CONNECTION

OUTPUT

BUSY : EXTRACTION REGISTER BUSY
OSC2 : OSCILLATOR
SCLK : DATA SLICER SAMPLING CLOCK
SDATA : DATA SLICER SAMPLED DATA
SDO : SERIAL COMMUNICATION DATA
SWIN : DATA SLICER WINDOW

INPUT/OUTPUT

PLLTA : ANALOG TEST FOR THE EXTRACTION MODULE PLL
PLLTD : DIGITAL TEST FOR THE EXTRACTION MODULE PLL
R$\overline{W}$: MEMORY READ/$\overline{WRITE}$


MUX
QUASI - H/V SYNC
29
BUSY
SYNC
17
SYNC SEP
VDD2
16
DATA SEP
DATA SLICER
GND
19
VDATA
18
CLAMP
21
XFC
PLL
25
PLLTD
24
PLLTA
RESET
28
PAR/SER
27
TEST
26
SYSTEM
OSC1
31
OSC2
32
VDD3
9, 23
GND
15, 30
INTERNAL BUS
MULTIPLEXED EXPANDED BUS
SPI
1
2
3
4 - 8
14
13
12
11
10
AD0/SCLK
AD1/SDATA
AD2/SWIN
AD3 - AD7
CSA
CS
SCK/E
SDO/RW
SDI/AS