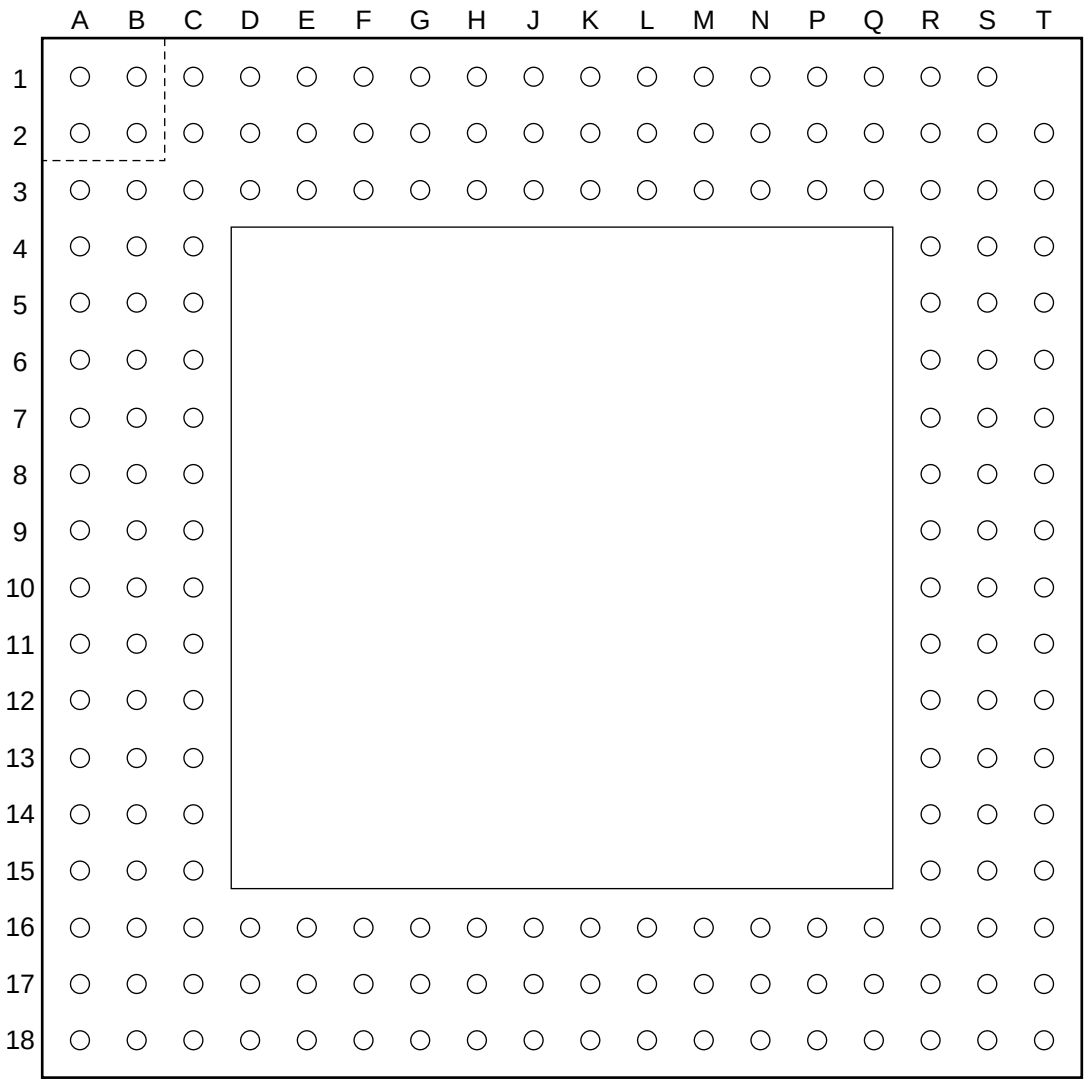
****

IL08

C-MOS 32-BIT MICROPROCESSOR EMBEDDED CONTROLLER

– BOTTOM VIEW–



(V_{DD} = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1A	I/O	A31	3A	I/O	D4	7A	I/O	D9	13A	I/O	D15	17A	I/O	D21
1B	I/O	A29	3B	I/O	D1	7B	I/O	D8	13B	—	GND	17B	—	GND
1C	I/O	A27	3C	I/O	D0	7C	—	GND	13C	—	GND	17C	—	V_{DD}
1D	I/O	A24	3D	I/O	A30	7R	I	BCLK	13R	—	GND	17D	—	GND
1E	I/O	A22	3E	I/O	A28	7S	I	$\overline{RSTI}$	13S	I	$\overline{TEA}$	17E	I/O	D30
1F	I/O	A21	3F	I/O	A25	7T	I	$\overline{IPL1}$	13T	I	$\overline{BG}$	17F	—	GND
1G	I/O	A20	3G	I/O	A23	8A	I/O	D10	14A	I/O	D17	17G	—	V_{DD}
1H	I/O	A18	3H	—	V_{DD}	8B	—	GND	14B	—	V_{DD}	17H	—	GND
1J	I/O	A17	3J	—	V_{DD}	8C	—	V_{DD}	14C	—	V_{DD}	17J	I/O	A2
1K	I/O	A15	3K	—	GND	8R	—	V_{DD}	14R	O	PST2	17K	O	TM2
1L	I/O	A14	3L	—	GND	8S	—	V_{DD}	14S	O	PST1	17L	—	GND
1M	I/O	A13	3M	—	V_{DD}	8T	I	$\overline{IPL0}$	14T	I/O	$\overline{TA}$	17M	—	V_{DD}
1N	I/O	A12	3N	I/O	A11	9A	I/O	D11	15A	I/O	D19	17N	—	GND
1P	I/O	A10	3P	I/O	TT0	9B	—	V_{DD}	15B	—	GND	17P	I/O	SIZ0
1Q	O	UPA1	3Q	O	UPA0	9C	—	GND	15C	I/O	D23	17Q	—	GND
1R	O	$\overline{CIOUT}$	3R	O	$\overline{RSTO}$	9R	I	PCLK	15R	O	$\overline{TIP}$	17R	—	V_{DD}
1S	O	$\overline{IPEND}$	3S	I	TDI	9S	—	GND	15S	—	GND	17S	—	GND
			3T	I	$\overline{TRST}$	9T	—	NC	15T	O	PST0	17T	I/O	$\overline{BB}$
2A	I/O	D3	4A	I/O	D5	10A	I/O	D12	16A	I/O	D20	18A	I/O	D24
2B	—	GND	4B	—	GND	10B	—	GND	16B	I/O	D22	18B	I/O	D26
2C	—	V_{DD}	4C	I/O	D2	10C	—	V_{DD}	16C	I/O	D25	18C	I/O	D28
2D	—	GND	4R	—	GND	10R	—	GND	16D	I/O	D27	18D	I/O	D31
2E	I/O	A26	4S	I	TCK	10S	—	GND	16E	I/O	D29	18E	I/O	A8
2F	—	GND	4T	—	GND	10T	I	$\overline{TCI}$	16F	I/O	A9	18F	I/O	A7
2G	—	V_{DD}	5A	I/O	D6	11A	I/O	D13	16G	I/O	A6	18G	I/O	A5
2H	—	GND	5B	—	V_{DD}	11B	I/O	D16	16H	—	V_{DD}	18H	I/O	A4
2J	I/O	A19	5C	—	V_{DD}	11C	—	GND	16J	—	V_{DD}	18J	I/O	A3
2K	I/O	A16	5R	—	V_{DD}	11R	—	GND	16K	—	GND	18K	I/O	A1
2L	—	GND	5S	I	TMS	11S	I	$\overline{TBI}$	16L	—	V_{DD}	18L	I/O	A0
2M	—	V_{DD}	5T	I	$\overline{CDIS}$	11T	I	$\overline{AVEC}$	16M	—	GND	18M	O	TM1
2N	—	GND	6A	I/O	D7	12A	I/O	D14	16N	I/O	R/$\overline{W}$	18N	O	TM0
2P	I/O	TT1	6B	—	GND	12B	I/O	D18	16P	I/O	SIZ1	18P	O	TLN1
2Q	—	GND	6C	—	GND	12C	—	V_{DD}	16Q	O	$\overline{MI}$	18Q	O	TLN0
2R	—	V_{DD}	6R	—	GND	12R	—	V_{DD}	16R	I/O	$\overline{TS}$	18R	O	$\overline{LOCKE}$
2S	—	GND	6S	—	GND	12S	I	SC1	16S	—	V_{DD}	18S	O	$\overline{LOCK}$
2T	O	TDO	6T	I	$\overline{IPL2}$	12T	I	SC0	16T	O	PST3	18T	O	$\overline{BR}$

INPUT

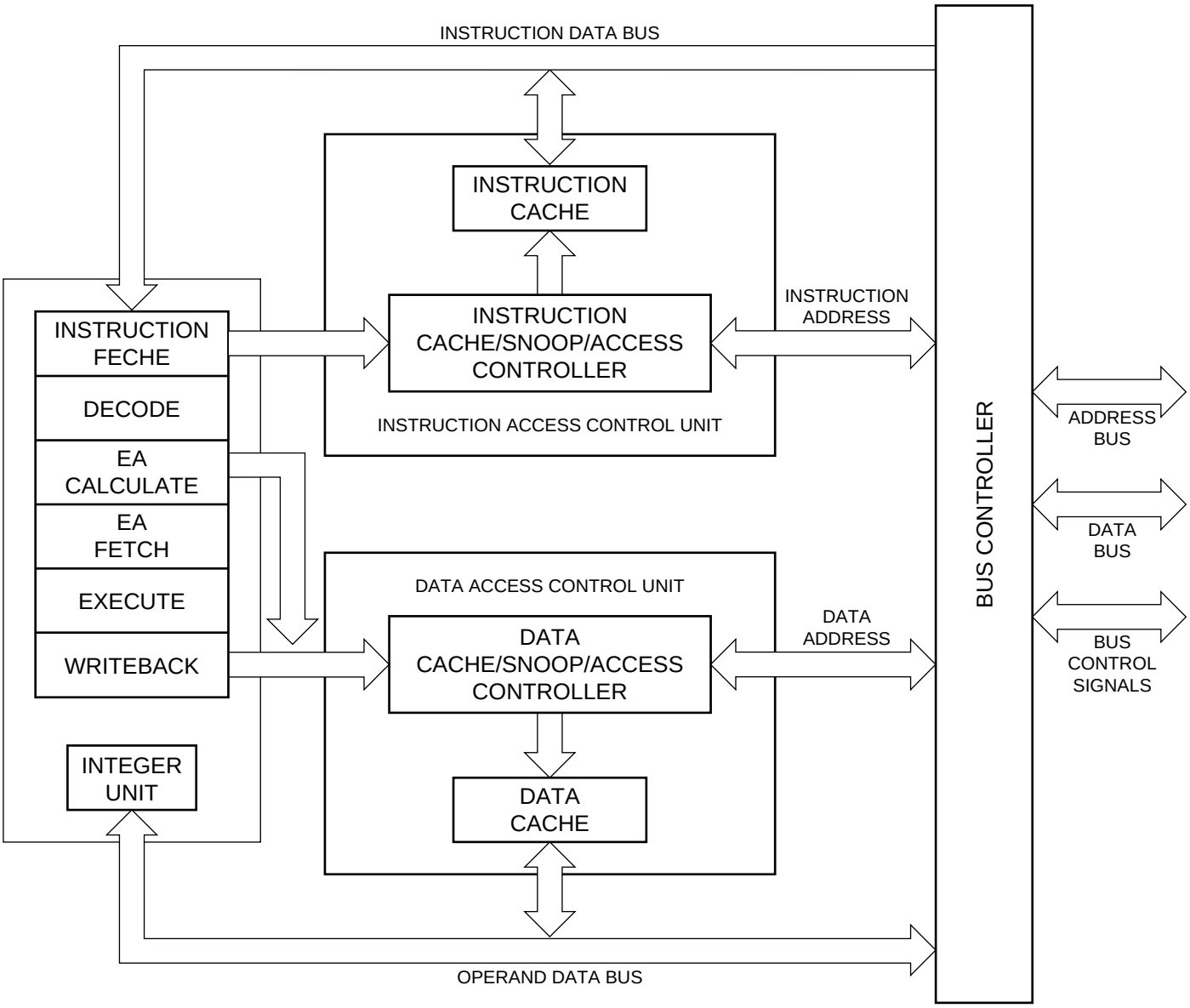
$\overline{\text{AVEC}}$	; AUTOVECTOR
$\overline{\text{BG}}$	; BUS GRANT
$\overline{\text{CDIS}}$	; CACHE DISABLE
BCLK	; BUS CLOCK
$\overline{\text{IPL2}}$ - $\overline{\text{IPL0}}$	; INTERRUPT PRIORITY LEVEL
PCLK	; PROCESSOR CLOCK
$\overline{\text{RSTI}}$	; RESET INPUT
SC1, SC0	; SNOOP CONTROL
$\overline{\text{TBI}}$	; TRANSFER BURST INHIBIT
$\overline{\text{TCI}}$	; TRANSFER CACHE INHIBIT
TCK	; TEST CLOCK
TDI	; TEST DATA INPUT
$\overline{\text{TEA}}$	; TRANSFER ERROR ACKNOWLEDGE
TMS	; TEST MODE SELECT
$\overline{\text{TRST}}$	; TEST RESET

OUTPUT

BR	; BUS REQUEST
$\overline{\text{CIOUT}}$	; CACHE INHIBIT OUT
$\overline{\text{IPEND}}$	; INTERRUPT PENDING
$\overline{\text{LOCK}}$	; BUS LOCK
$\overline{\text{LOCKE}}$	; BUS LOCK END
$\overline{\text{MI}}$	; MEMORY INHIBIT
PST3 - PST0	; PROCESSOR STATUS
$\overline{\text{RSTO}}$	; RESET OUTPUT
TDO	; TEST DATA OUTPUT
$\overline{\text{TIP}}$	; TRANSFER IN PROGRESS
TLN1, TLN0	; TRANSFER LINE NUMBER
TM2, TM0	; TRANSFER MODIFIER
UPA1, UPA0	; USER PROGRAMMABLE ATTRIBUTES

INPUT/OUTPUT

A31 - A0	; ADDRESS BUS
$\overline{\text{BB}}$	; BUS BUSY
D31 - D0	; DATA BUS
R/$\overline{\text{W}}$	; READ/WRITE
SIZ1, SIZ0	; TRANSFER SIZE
$\overline{\text{TA}}$	; TRANSFER ACKNOWLEDGE
$\overline{\text{TS}}$	; TRANSFER START
TT1, TT0	; TRANSFER TYPE


INSTRUCTION DATA BUS
INSTRUCTION CACHE
INSTRUCTION FECHE
DECODE
EA CALCULATE
EA FETCH
EXECUTE
WRITEBACK
INTEGER UNIT
INSTRUCTION CACHE/SNOOP/ACCESS CONTROLLER
INSTRUCTION ADDRESS
INSTRUCTION ACCESS CONTROL UNIT
DATA ACCESS CONTROL UNIT
DATA CACHE/SNOOP/ACCESS CONTROLLER
DATA ADDRESS
DATA CACHE
BUS CONTROLLER
ADDRESS BUS
DATA BUS
BUS CONTROL SIGNALS
OPERAND DATA BUS