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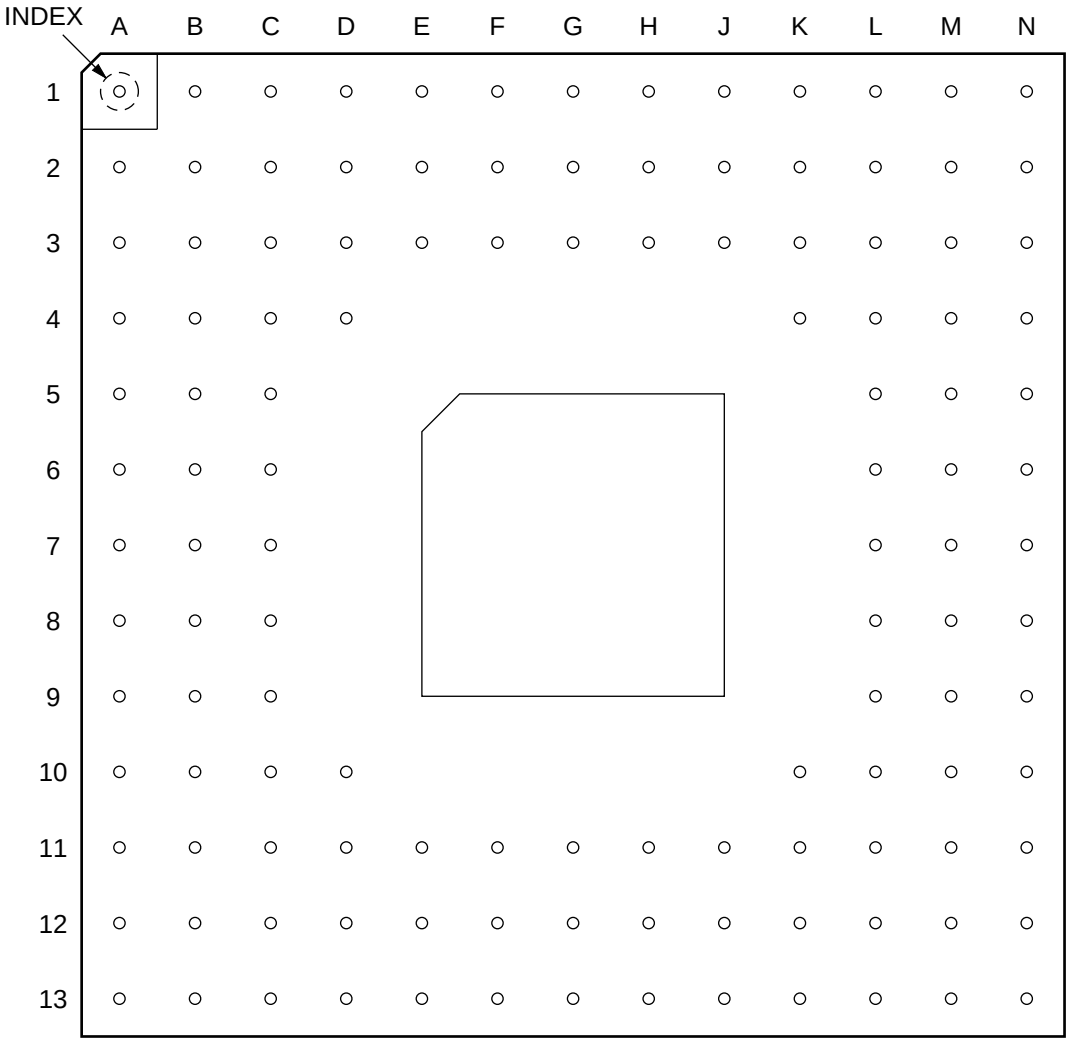
IL08

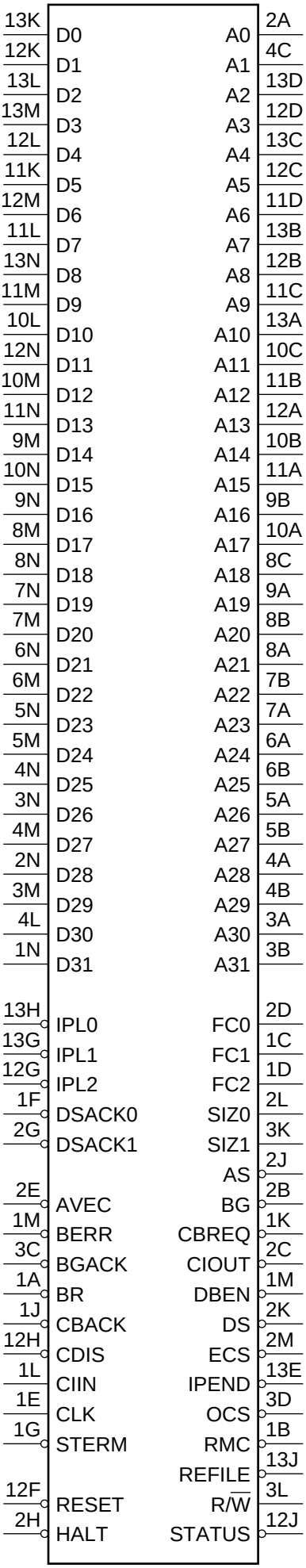
C-MOS 32-BIT MICROPROCESSOR

- BOTTOM VIEW -



(V_{DD} =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1A	I	$\overline{BR}$	3F	–	GND	7L	–	GND	11J	–	GND
1B	O	$\overline{RMC}$	3G	–	GND	7M	I/O	D20	11K	I/O	D5
1C	O	FC1	3H	–	V_{DD}	7N	I/O	D19	11L	I/O	D7
1D	O	FC2	3J	–	GND	8A	O	A21	11M	I/O	D9
1E	I	CLK	3K	O	SIZ1	8B	O	A20	11N	I/O	D13
1F	I	$\overline{DSACK0}$	3L	O	R/$\overline{W}$	8C	O	A18	12A	O	A13
1G	I	$\overline{STERM}$	3M	I/O	D29	8L	–	GND	12B	O	A8
1H	I	$\overline{BERR}$	3N	I/O	D26	8M	I/O	D17	12C	O	A5
1J	I	$\overline{CBACK}$	4A	O	A28	8N	I/O	D18	12D	O	A3
1K	O	$\overline{CBREQ}$	4B	O	A29	9A	O	A19	12E	–	NC
1L	I	C1IN	4C	O	A1	9B	O	A16	12F	I/O	$\overline{RESET}$
1M	O	$\overline{DBEN}$	4D	–	V_{DD}	9C	–	GND	12G	I	$\overline{IPL2}$
1N	I/O	D31	4K	–	V_{DD}	9L	–	GND	12H	I	$\overline{CDIS}$
2A	O	A0	4L	I/O	D30	9M	I/O	D14	12J	O	$\overline{STATUS}$
2B	O	$\overline{BG}$	4M	I/O	D27	9N	I/O	D16	12K	I/O	D1
2C	O	$\overline{C1OUT}$	4N	I/O	D25	10A	O	A17	12L	I/O	D4
2D	O	FC0	5A	O	A26	10B	O	A14	12M	I/O	D6
2E	I	$\overline{AVEC}$	5B	O	A27	10C	O	A11	12N	I/O	D11
2F	–	V_{DD}	5C	–	GND	10D	–	V_{DD}	13A	O	A10
2G	I	$\overline{DSACK1}$	5L	–	GND	10K	–	V_{DD}	13B	O	A7
2H	I/O	$\overline{HALT}$	5M	I/O	D24	10L	I/O	D10	13C	O	A4
2J	O	$\overline{AS}$	5N	I/O	D23	10M	I/O	D12	13D	O	A2
2K	O	$\overline{DS}$	6A	O	A24	10N	I/O	D15	13E	O	$\overline{IPEND}$
2L	O	SIZ0	6B	O	A25	11A	O	A15	13F	–	NC
2M	O	$\overline{ECS}$	6C	–	V_{DD}	11B	O	A12	13G	I	$\overline{IPL1}$
2N	I/O	D28	6L	–	V_{DD}	11C	O	A9	13H	I	$\overline{IPL0}$
3A	O	A30	6M	I/O	D22	11D	O	A6	13J	O	$\overline{REFILE}$
3B	O	A31	6N	I/O	D21	11E	–	GND	13K	I/O	D0
3C	I	$\overline{BGACK}$	7A	O	A23	11F	–	V_{DD}	13L	I/O	D2
3D	O	$\overline{OCS}$	7B	O	A22	11G	–	GND	13M	I/O	D3
3E	–	GND	7C	–	GND	11H	–	V_{DD}	13N	I/O	D8



INPUT

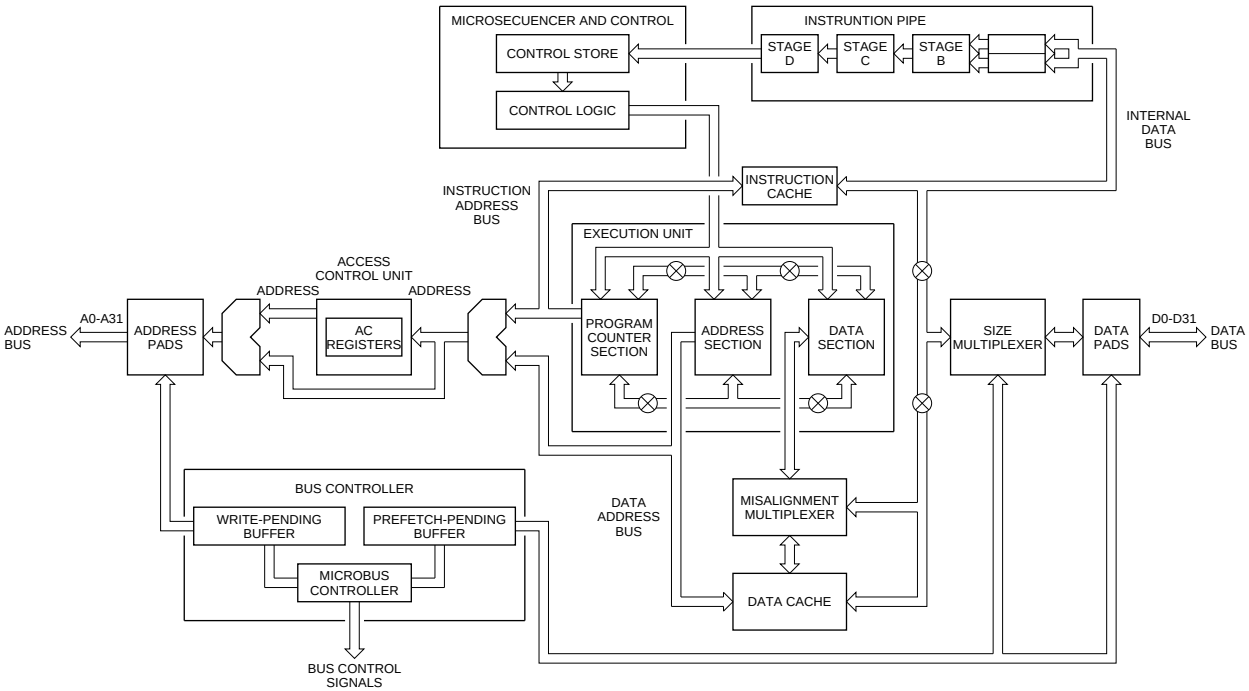
$\overline{\text{AVEC}}$	:	AUTO VECTOR
$\overline{\text{BERR}}$	:	BUS ERROR
$\overline{\text{BGACK}}$	:	BUS GRANT ACKNOWLEDGE
$\overline{\text{BR}}$	:	BUS REQUEST
$\overline{\text{CDIS}}$	:	CACHE DISABLE
CIIN	:	CACHE INHIBIT IN
CLK	:	CLOCK
$\overline{\text{DSACK0}}$, $\overline{\text{DSACK1}}$	:	DATA TRANSFER AND SIZE ACKNOWLEDGE
$\overline{\text{IPL0}}$–$\overline{\text{IPL2}}$	:	INTERRUPT PRIORITY LEVEL
$\overline{\text{STERM}}$	:	SYNCHRONOUS TERMINATION

OUTPUT

A0–A31	:	ADDRESS BUS
$\overline{\text{AS}}$	:	ADDRESS STROBE
$\overline{\text{BG}}$	:	BUS GRANT
$\overline{\text{CBREQ}}$	:	CACHE BURST REQUEST
$\overline{\text{CIOUT}}$	:	CACHE INHIBIT OUT
$\overline{\text{DBEN}}$	:	DATA BUFFER ENABLE
$\overline{\text{DS}}$	:	DATA STROBE
$\overline{\text{ECS}}$	:	EXTERNAL CYCLE START
FC0–FC2	:	FUNCTION CODES
$\overline{\text{IPEND}}$	:	INTERRUPT PENDING
$\overline{\text{OCS}}$	:	OPERAND CYCLE START
R/$\overline{\text{W}}$	:	READ/WRITE
$\overline{\text{REFILE}}$	:	PIPE REFILL
$\overline{\text{RMC}}$	:	READ-MODIFY-WRITE CYCLE
SIZ0, SIZ1	:	SIZE
$\overline{\text{STATUS}}$	:	MICROSEQUENCER STATUS

INPUT/OUTPUT

D0–D31	:	DATA BUS
$\overline{\text{HALT}}$	:	HALT
$\overline{\text{RESET}}$	:	RESET


MICROSECUENCER AND CONTROL
CONTROL STORE
CONTROL LOGIC
INSTRUNTION PIPE
STAGE D
STAGE C
STAGE B
INTERNAL DATA BUS
INSTRUCTION CACHE
INSTRUCTION ADDRESS BUS
EXECUTION UNIT
ACCESS CONTROL UNIT
ADDRESS
ADDRESS
A0-A31
ADDRESS BUS
ADDRESS PADS
AC REGISTERS
PROGRAM COUNTER SECTION
ADDRESS SECTION
DATA SECTION
SIZE MULTIPLEXER
DATA PADS
D0-D31
DATA BUS
BUS CONTROLLER
WRITE-PENDING BUFFER
PREFETCH-PENDING BUFFER
MICROBUS CONTROLLER
BUS CONTROL SIGNALS
DATA ADDRESS BUS
MISALIGNMENT MULTIPLEXER
DATA CACHE