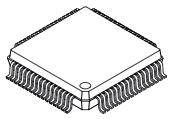
Product Preview

Twisted Pair Interface
for FDDI Local Area Networks

MC68835



FA SUFFIX
TQFP PACKAGE
CASE 931–02

Overview

The FDDI is a LAN standard under ANSI auspices. The standard supports a 100 Mbps fiber–optic–based token ring with up to 1000 stations; total ring length should not exceed 200 Km with up to 2 km between stations. FDDI over twisted–pair cable is also supported by the TP–PMD standard. The twisted pair cable connecting two stations can be up to 100 meters in length. Users are encouraged to refer to the pertinent ANSI standard documents for further information.

Introduction

The MC68835 Twisted–Pair Interface chip (TPIC) is a transceiver capable of transmitting and receiving MLT3 or NRZI encoded data streams, as well as handling clock and data recovery. The TPIC implements the lower portion of the Physical layer (PHY) functions of the FDDI standard. It performs a five–bit parallel to serial conversion during transmission, as well as a five–bit serial to parallel conversion during reception. The TPIC uses the five–bit parallel interface to communicate with the MC68837 Elastic Buffer and Link Manager (ELM) device or other Motorola FDDI devices that incorporate the ELM function internally, such as the 68840 IFDDI, 68848 CAMEL, or the 68847 Quad ELM.

MC68835 Features

- Supports Twisted Pair and Fiber Optic Media
- Supports MLT–3 Line Code in Twisted Pair Mode
- Supports NRZI Line Code in Fiber Mode
- Adaptive Receive Equalization supports TP line lengths of 0 to 100 meters
- Controlled Twisted Pair Output Transition Times May Eliminate Need for Transmit Filter
- TP Receiver Includes Circuitry Which Enables Error Free Reception of Data Distorted with Base Line Wander
- Twisted Pair and Fiber Transmitters Share Same IC pins. Twisted Pair and Fiber Receivers also Share Same IC Pins
- Twisted Pair or Fiber Optic Operation Selected with PORTSEL Input
- Twisted Pair (TP) Transceiver Complies with ANSI X3T9.5 TP–PMD FDDI Standard
- Meets Jitter Requirements of ANSI X3T9.5 TP–PMD
- Pseudo–ECL Interface For Fiber–Optic Media
- Digital Phase–Locked Loop (DPLL) Provides Run Length Immunity
- Transmit Off Capability for True Quiet Line State
- Uses a 25 Mhz External Frequency Reference
- Converts Received Serial Bit Stream to Five–Bit Parallel Form
- Recovers 125 Mhz Clock from Incoming Serial NRZI or MLT3 Data Stream
- Generates 25 Mhz Receive Clock
- Small Number of Passive External Components Required
- Selectable Low Power Mode
- Loop Back Capability
- Single +5V Power Supply
- Utilizes 0.8uM BiCMOS Technology
- 10mM X 10mM, 64 Pin, TQFP Package

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Functional Description

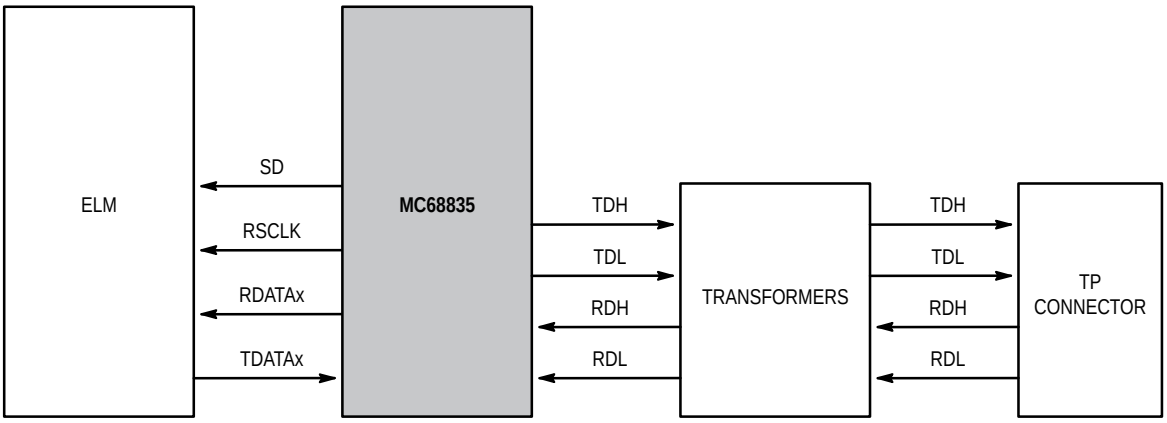


Figure 1. Simplified Block Diagram for Twisted Pair Applications of the MC68835 TPIC

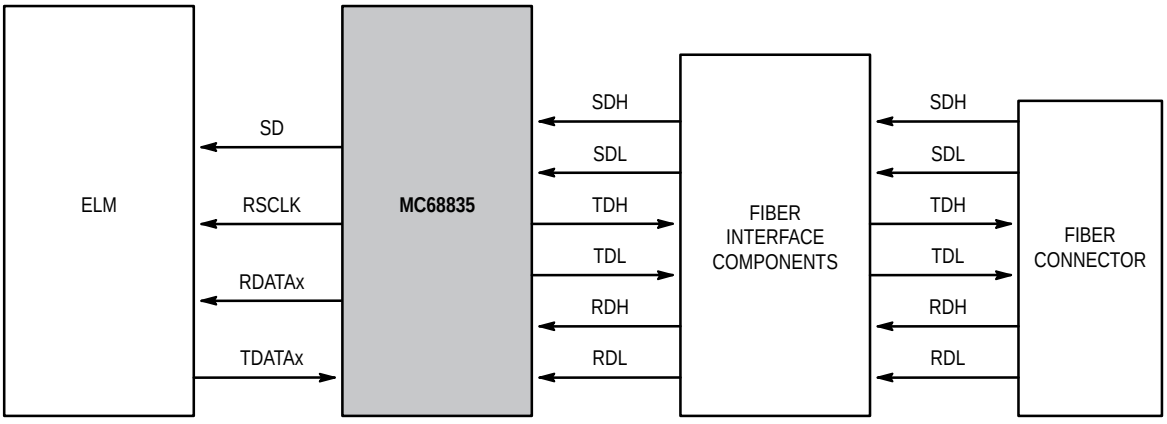


Figure 2. Simplified Block Diagram for Optical Fiber Applications of the MC68835 TPIC

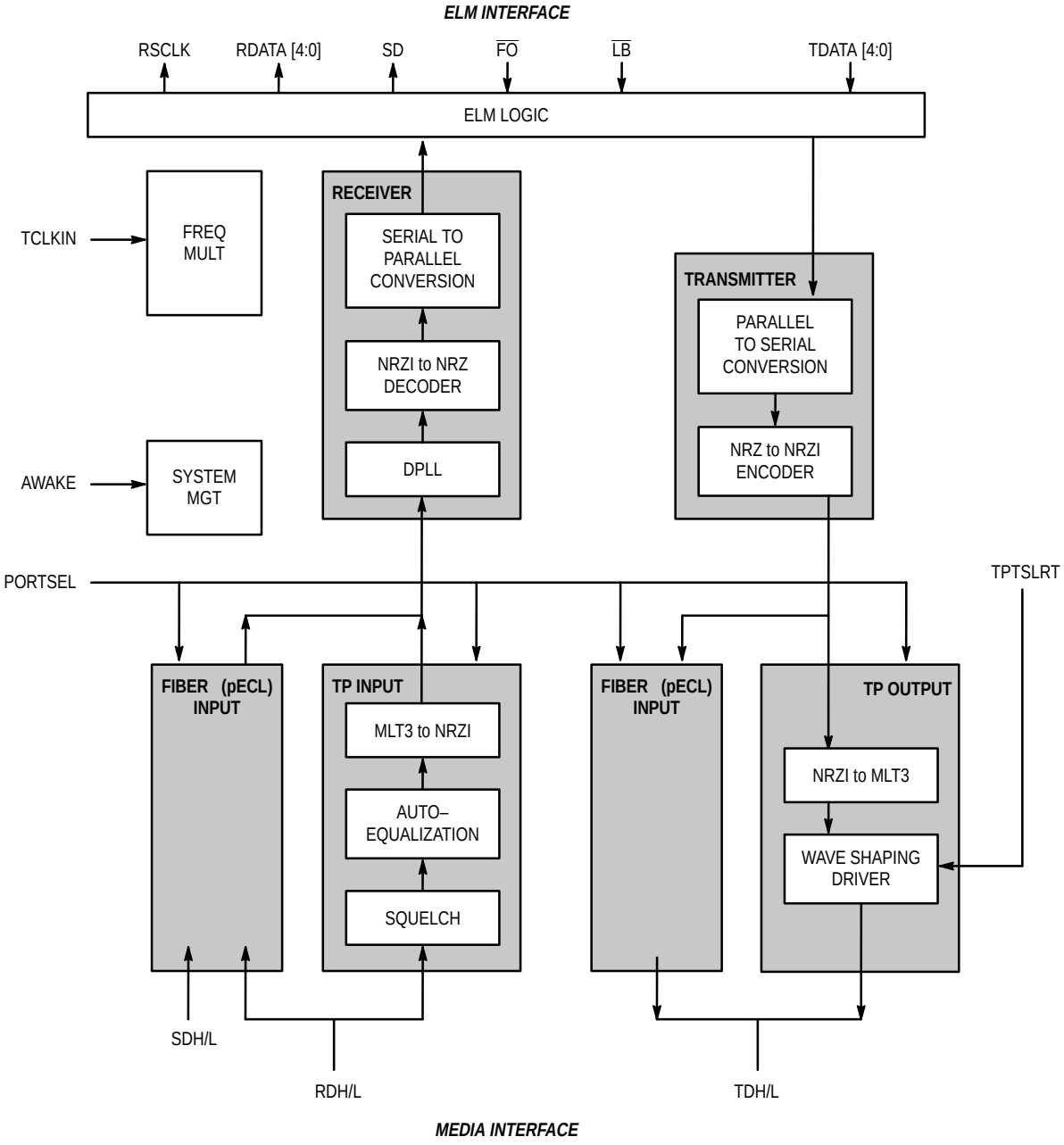


Figure 3. MC68835 Simplified Block Diagram

Pin Assignments

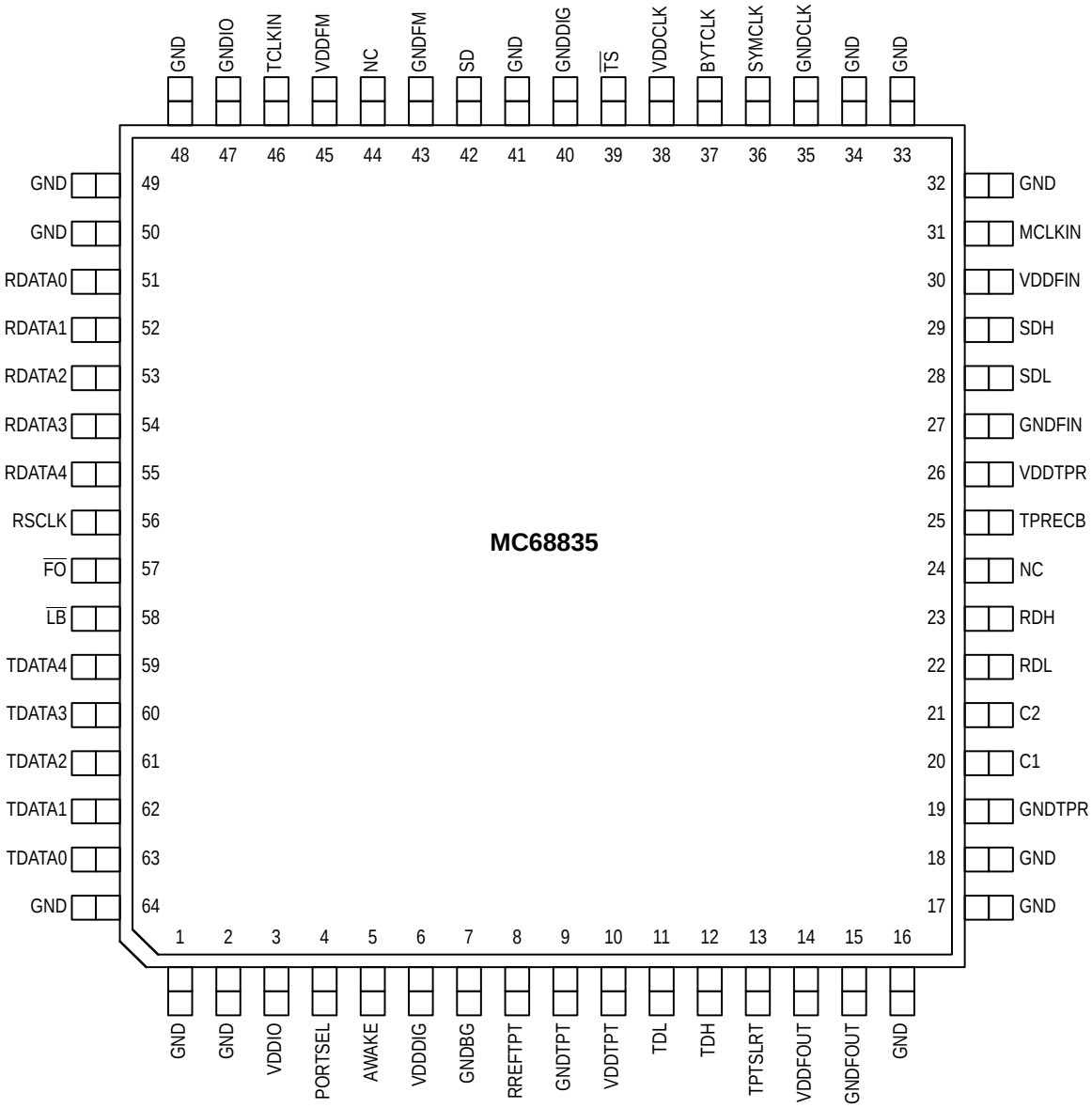


Figure 4. MC68835 Pinout: 64–Lead TQFP Package (Top View)

Table 1. Media Interface Pins

Pin No.	Pin Name	Pin Type	Pin Description
11 12	TDL TDH	O	Differential Transmitter Outputs These pins are shared by two types of transmitters. When PORTSEL is in the high logic state the Twisted Pair Transmitter is enabled. When low the Fiber Transmitter is enabled Twisted Pair Mode: In Twisted Pair Mode MLT–3 coding is used. MLT–3 data contains three logic states: +1, 0, and –1. The +1 logic state is produced when the TDH output is activated while the TDL output is off. The –1 logic state is produced when the TDL output is activated while the TDH output is off. The 0 logic state is produced when both outputs are active. Fiber Mode: in Fiber Mode the transmit data stream is NRZI encoded. A positive differential output voltage represents that light energy is to be transmitted on the fiber media, and a negative differential output voltage represents that no light energy is to be transmitted on the fiber media. The signal changes at a 125 Mbps rate.
22 23	RDL RDH	I	Differential Receiver Inputs These pins are shared by two types of receivers. When PORTSEL is in the high logic state the Twisted Pair Receiver is enabled. When low, the Fiber Receiver is enabled Twisted Pair Mode: The inputs are connected to a receiver which features adaptive equalization and squelch capabilities. The squelch capability blocks signals which do not meet a preset minimum level specification. Fiber Mode: A positive differential voltage applied to these inputs represents active light energy on the fiber media, and a negative differential voltage represents no active light energy on the fiber media. The signal changes at a 125 Mbps rate.
28 29	SDL SDH	I pECL	Fiber Signal Detect Differential Receiver Inputs A positive differential voltage applied to these inputs represents an active fiber link and a negative differential voltage represents an inactive fiber link. This input changes infrequently.

Table 2. Mode Select Pins

Pin No.	Pin Name	Pin Type	Pin Description
4	PORTSEL	I TTL	Port Select When high, the PORTSEL input causes the twisted pair port and MLT3 coding to be selected. When low, it causes the fiber port and NRZI coding to be selected. The power consumption is minimized in the circuitry associated with the unselected port.
5	AWAKE	I TTL	Awake Input When the AWAKE input is set to the high logic state, the MC68835 operates in its normal mode. In the normal mode, only the active port (twisted–pair or fiber–optic) is powered–up. To conserve power, the unused port is powered–down. When neither port is being used, the AWAKE input may be driven to the low logic state where the MC68835 operates in a low power “snooze” mode. In this low power mode the system clocks continue to operate.
13	TPTSLRT	I TTL	Twisted Pair Transmitter Slew Rate Select When the TPTSLRT input is set to the high logic state, the output slew rate will be at about 2.5ns/volt. When the TPTSLRT is set to the low logic state, the slew rate will be at about 4ns/volt.[1] In the low slew rate mode, it may be unnecessary to utilize an external transmit filter.
39	$\overline{TS}$	I TTL	Three State Enable When low, this input causes all the RDATA outputs and the RSCLK and SD outputs to go to the high impedance state.

1. Specification established by design and laboratory characterization

Table 3. Elasticity Link Manager (ELM) Interface Pins

Pin No.	Pin Name	Pin Type	Pin Description
42	SD	O TTL	Signal Detect Output When the LB input is low, the SD output is high. When the LB input is high the function of this pin depends upon the mode selected by the PORTSEL pin. Fiber Mode: When the Fiber Mode is selected, a high level at the SD output indicates a positive differential voltage is applied to the SDH/SDL input pair. A low level at the SD output indicates a negative differential voltage is applied to the SDH/SDL input pair. Twisted Pair Mode: When the Twisted Pair Mode is selected, a high logic state, on the SD output indicates the presence of a received Twisted Pair data signal with an amplitude exceeding a preset squelch threshold.
51 52 53 54 55	RDATA0 RDATA1 RDATA2 RDATA3 RDATA4	O TTL	Receive Data Bus Outputs These outputs deliver recovered receive data to the ELM. The data appearing at each output may change at a 25 Mbps rate. RDATA4 is received from the media first.
56	RSCLK	O TTL	Recovered Symbol Clock Output This clock signal is used to latch data received on RDATAx and to operate the elasticity buffer. The frequency of this signal is nominally 25 MHz.
57	FO	I TTL	Transmit Output Disable Input When the FO input is low the Transmitter Differential Outputs, TDH and TDL are disabled.
58	LB	I TTL	Loopback Enable When low, this input enables Transmitter–Receiver loopback capability, which causes data appearing at the Transmit Data Bus Inputs (TDATAx) to be fed to the Receive Data Bus Outputs (RDATAx) and the Signal Detect output (SD) to be forced high. While in the Loopback mode, the ELM interface will not receive any data from the RDL and RDH inputs, however, the FO input must be forced low to prevent transmit data from appearing on the TDL and TDH outputs.
59 60 61 62 63	TDATA4 TDATA3 TDATA2 TDATA1 TDATA0	I TTL	Transmit Data Bus Inputs These inputs accept data from the ELM which is to be transmitted to the attached media. The data appearing at each input may change at a 25 Mbps rate. TDATA4 is transmitted on the media first.

Table 4. Clock Pins

Pin No.	Pin Name	Pin Type	Pin Description
31	MCLKIN	I TTL	Master Clock Input In “master clock mode” users should connect an external 25MHz reference clock to this input. In “slave clock mode” users should connect this input to ground.
36	SYMCLK	O TTL	Symbol Clock Output This 25MHz output is used only in FDDI master clock mode applications. In master clock mode this output is connected to the TCLKIN input and the SYMCLK input of all other FDDI devices in the system. In slave clock mode this output is unused and should be left unconnected.
37	BYTCLK	O TTL	Byte Clock Output This 12.5MHz output is used only in FDDI master clock mode applications. In master clock mode this output is connected to the BYTCLK input of all other FDDI devices in the system. In slave clock mode this output is unused and should be left unconnected.
46	TCLKIN	I TTL	Transmit Clock Input Users must connect a 25MHz reference clock to this input.

Table 5. External Component Connection Pins

Pin No.	Pin Name	Pin Type	Pin Description
8	RREFTPT	X	Twisted Pair Transmitter External Reference Resistor Connection Pin An external precision resistor must be connected between this pin and ground to set the transmit output current amplitude. To meet the transmit signal levels specified by the ANSI X3T9.5 TP–PMD specification, RREFTPT should be set to 2KΩ ±1%. This value of RREFTPT yields an output current of ±40mA. For 100 ohm characteristic impedance UTP applications, this current results in a 1.0V peak differential output voltage.
20 21	C1 C2	X	Twisted Pair Adaptive Equalizer Feedback Capacitor Connection Pins The external capacitor connected to these pins controls the time constant of the adaptive receive equalizer. The recommended value is 400pF.
25	TPRECB	X	Twisted Pair Receiver Bias Resistor Connection Pin The external precision resistor connected to this pin and ground establishes an internal reference current.This resistor should be set to a value of 3KΩ ±1%.

Table 6. Power Pins

Pin No.	Pin Name	Pin Type	Pin Description
3	VDDIO	P	CMOS I/O Power
47	GNDIO	G	CMOS I/O Ground
6	VDDDIG	P	Digital Logic Power
40	GNDDIG	G	Digital Logic Ground
7	GNDBG	G	Band Gap Regulator Ground
10	VDDTPT	P	TP Transmit Power
9	GNDTPT	G	TP Transmit Ground
14	VDDFOUT	P	Fiber Output Power
13	GNDFOUT	G	Fiber Output Ground
24	VDDTPR	P	TP Receiver Power
19	GNDTPR	G	TP Receiver Ground
30	VDDFIN	P	Fiber Input Power
27	GNDFIN	G	Fiber Input Ground
45	VDDFM	P	Frequency Multiplier Power
43	GNDFM	G	Frequency Multiplier Ground
38	VDDCLK	P	Clock Power
35	GNDCLK	G	Clock Ground
1 2 16 17 18 32 33 34 41 48 49 50 64	GND	G	Substrate Grounds

Table 7. No Connect Pins

Pin No.	Pin Name	Pin Type	Pin Description
24 44	NC	–	No Connect– The No Connect pins must be left disconnected.

Operation of Circuit Blocks

(See Figure 3)

Twisted Pair Transmitter Output and Receiver Input

Output

When the twisted–pair transmitter is selected by the PORTSEL input, it is used to transmit MLT3 coded signals to the twisted–pair transmit transformer as shown in Figure 1. Since transmit waveshaping is employed, an external transmit filter may not be required.

(MLT3 is a coding scheme in which every logical HIGH bit on the transmitter input stream produces alternately a positive or a negative pulse on the output and every logical LOW bit produces no positive nor negative pulse on the output.)

Input

When the twisted–pair receiver is selected by the PORTSEL input, it is used to receive MLT3 coded signals from the twisted–pair receive transformer as shown in Figure 1. A squelch function is applied to determine if sufficient energy exists on the media to effect data recovery. If enough energy is detected, an equalizer filters the receive signal to undo the effects of the media including attenuation, phase distortion and base line wander. The receiver inputs must be driven differentially in order to assure proper operation.

Fiber Transmitter Output and Receiver Input

Output

When the fiber transmitter is selected by the PORTSEL input, it is used to transmit NRZI coded signals to the fiber interface components as shown in Figure 2. Normal ECL termination techniques (with provisions for the positive logic input levels) should be used to interface the outputs with optical transceiver modules.

(NRZI is a method of encoding a clock signal into a data stream. It operates by inverting the polarity of the output signal on every logical HIGH bit and not inverting the output on every logical LOW bit. Hence, every HIGH bit produces a state transition on the output, while every LOW bit produces no such transition. NRZI, along with 4B/5B encoding, assures the receiving PLL of a certain minimum density of clock transitions for any given data pattern.)

Input

When the fiber receiver is selected by the PORTSEL input, it is used to receive differential, pseudo–ECL, NRZI coded signals from the fiber interface components as shown in Figure 2. Normal ECL termination techniques (with provisions for the positive logic input levels) should be used to interface the receive inputs of the optical transceiver modules. The Fiber inputs must be driven differentially in order to assure proper operation.

ELM Interface

The ELM interface is a TTL–level interface composed of five parts: receive data, receive signal detect, transmit data, and two control signals, $\overline{FO}$ and $\overline{LB}$. The transmit and receive parts each have independent clocks.

Receive Data

A Digital–Phase–Lock–Loop is used to recover the incoming nominal 125 MHz data stream from the selected serial port data. The DPLL maintains frequency lock with the received data with only minimal transitions in the data stream. (The FDDI stream cipher algorithm, when combined with FDDI's 4B/5B coding, can generate up to sixty bits, which is 480 nS, without a transition on the media). The recovered data and clock are used by the Decoder to extract the received NRZ data stream.

Data received is output on the RDATA4 – RDATA0 outputs. Five new bits are output on each rising edge of RSCLK. The serial data reception order is: RDATA4, first bit received, and RDATA0, last bit received. RSCLK is derived from the incoming bit stream. Data on RDATA4 – RDATA0 is not aligned to symbol boundaries.

Receive Signal Detect

When the fiber port is selected via PORTSEL, the signal detect output, SD is simply a level translation of the SDH and SDL inputs and indicates whether the receive data, RDH and RDL, is valid. This indicates that enough light energy is being received by the fiber optic receiver. When $\overline{LB}$ is low, SD is driven high and when the AWAKE input is low, the SD output is driven low.

When the twisted–pair port is selected via PORTSEL, SD is derived from a combination of signals from the Squelch and Auto Equalization functions. For SD to be asserted, the squelch must detect sufficient energy on RDH and RDL, and the Equalizer must have equalized.

Transmit Data

The 5–bit data symbols to be transmitted are obtained from the ELM device via the TDATA4 – TDATA0 inputs. A new 5–bit symbol is strobed in on each rising edge of TCLKIN and are output at the TDH/L output. The serial data transmission order is: TDATA4, first bit transmitted, TDATA0, last bit transmitted.

When the fiber mode is selected via PORTSEL, the Encoder converts the transmit data stream into NRZI and the digital serial transmit data stream is output as pseudo–ECL on TDH and TDL.

When the twisted–pair mode is selected via PORTSEL, the NRZI data stream is converted to MLT3 coded data and output at the TDH/TDL outputs.

Transmit Disable ($\overline{FO}$) and Parallel Loopback ($\overline{LB}$) Controls

When the $\overline{FO}$ and $\overline{LB}$ inputs are HIGH, the MC68835 is in its normal mode of operation. When $\overline{FO}$ is LOW, TDH and TDH are both forced LOW (quiet state).

When the $\overline{LB}$ input is HIGH, the MC68835 is in normal operation. When $\overline{LB}$ is LOW, the MC68835 is in LOOPBACK mode. In this mode, the serial transmit data stream that is normally delivered to the TDH and TDL outputs is also routed to the receive data circuit where it is recovered and delivered to the RDATA4 through RDATA0 outputs. If it is undesirable to place the serial data stream on the TDL and TDH outputs, the $\overline{FO}$ input must be driven to the low logic state. Additionally, when the $\overline{LB}$ input is LOW, the RDH and RDL and SDH and SDL inputs are ignored. Furthermore, the signal detect output, SD is driven high when $\overline{LB}$ is in the low logic state.

Frequency Multiplier

The Frequency Multiplier block utilizes the external 25 MHz signal (TCLKIN) as a reference to produce the 125MHz signal which is needed for operation of the digital phase locked loop (DPLL) circuitry.

System Management

The System Management block controls the standby mode.

Electrical Characteristics

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operation sections of this data sheet. Exposure to Absolute Maximum Ratings conditions for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	Tstg	–65	150	deg C
Power Supply Voltage Range	VDD	–0.3	7	V
Voltage on any TTL Compatible Input pin	V	–0.3	VDD+0.3	V
Voltage on RDH/RDL Input Pins with respect to Ground	V	–0.3	VDD+0.3	V
Differential voltage on RDH/RDL Input Pins	V			

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage Range	VDD	4.75	5.25	V
Ambient Operating Temperature Range	Ta	0	70	deg C

ESD

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Motorola employs a human–body model (resistance = 1500 Ω, capacitance – 100pF). The MC68835 will withstand exposure to 2KV standard human body model ESD testing.

TTL/CMOS Input and Output DC Characteristics

(Unless otherwise noted Minimum and Maximum limits apply over the recommended ambient operating temperature and power supply voltage ranges)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TTL Compatible Inputs						
Low State TTL Compatible Input Voltage	Vil (TTL)				0.8	V
High State TTL Compatible Input Voltage	Vih (TTL)		2.0			V
Input Current TTL Compatible Input Pins	Ii (TTL)				±10	uA
TTL/CMOS Compatible Outputs						
Low State TTL/CMOS Compatible Output Voltage	Vol	Iol = 4mA			0.45	V
High State TTL/CMOS Compatible Output Voltage	Voh	Ioh = –400uA	TBD			V
High State TTL/CMOS Compatible Output Voltage	Voh	Ioh = –4mA	2.4			V
Three State Output Leakage Current	Ioz	0V ≤ Voz ≤ VDD			50	uA

Twisted Pair Input and Output DC Characteristics

(Unless otherwise noted Minimum and Maximum limits apply over the recommended ambient operating temperature and power supply voltage ranges)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Twisted Pair Receiver Inputs						
Twisted Pair Common Mode Input Voltage Range	VICMTP	4.75V ≤ VDD ≤ 5.25V	2.2		TBD	V
Twisted Pair Peak Differential Input Voltage	VIDTP	4.75V ≤ VDD ≤ 5.25V			1	V
Twisted Pair Differential Input Resistance	RDIFFTP	4.75V ≤ VDD ≤ 5.25V	10			KΩ
Twisted Pair Common Mode Input Current	IICMTP	4.75V ≤ VDD ≤ 5.25V			10	uA
Twisted Pair Differential Input Squelch Threshold Voltage	VITPSQ	4.75V ≤ VDD ≤ 5.25V	TBD		TBD	V

Twisted Pair Input and Output DC Characteristics (continued)

(Unless otherwise noted Minimum and Maximum limits apply over the recommended ambient operating temperature and power supply voltage ranges)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Twisted Pair Transmitter Outputs						
Twisted Pair Differential Output Current High Current State	IODHTP	4.75V ≤ VDD ≤ 5.25V VO = VDD ± 0.5V RREFTPT =2KΩ ± 1%		40		mA
Twisted Pair Differential Output Current Low Current State	IODLTP	4.75V ≤ VDD ≤ 5.25V VO = VDD ± 0.5V	0	0.5	TBD	mA
Twisted Pair Differential Output Offset Current	IODOSTP	4.75V ≤ VDD ≤ 5.25V VO = VDD ± 0.5V			0.5	mA
Twisted Pair Differential Output Amplitude Error		4.75V ≤ VDD ≤ 5.25V VO = VDD	–5		5	%
Twisted Pair Differential Output Voltage Compliance		4.75V ≤ VDD ≤ 5.25V VO = VDD ± 1.1V	–2		–2	%

1. For a logic high, RDL must be at least Vidiff(min) but no more than Vidiff(max) lower than RDH. For a logic low, RDL must be at least Vidiff(min) but no more than Vidiff(max) higher than RDH.

Fiber Input and Output DC Characteristics

(Unless otherwise noted Minimum and Maximum limits apply over the recommended ambient operating temperature and power supply voltage ranges)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Fiber Receiver Inputs						
Fiber Differential Input Voltage Range[1]	Vidiff	4.75V ≤ VDD ≤ 5.25V	0.5		1.1	V
Fiber Common Mode Input Voltage Range[2]	Vicm	4.75V ≤ VDD ≤ 5.25V	VDD–1.9		VDD–0.8	V
Fiber High State Input Current	Iih	4.75V ≤ VDD ≤ 5.25V Vih = VDD–0.8V			50	µA
Fiber Low State Input Current	Iil	4.75V ≤ VDD ≤ 5.25V Vil = VDD–1.9V			–0.5	µA
Fiber Transmitter Outputs						
Fiber High State Output Voltage	Voh	4.75V ≤ VDD ≤ 5.25V Ioh = –20mA	VDD–1.1		VDD–0.8	V
Fiber Low State Output Voltage	Vol	4.75V ≤ VDD ≤ 5.25V Iol = –20mA	VDD–1.8		VDD–1.6	V

1. For a logic high, RDL must be at least Vidiff(min) but no more than Vidiff(max) lower than RDH. For a logic low, RDL must be at least Vidiff(min) but no more than Vidiff(max) higher than RDH.
2. This is the range of valid signal voltages that may be applied to the RDL and RDH inputs for proper operation in Fiber mode.

Power Supply DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Current	IDD	VDD = 5.25V[1]			300	mA
Power Supply Current Standby Mode (AWAKE Input Low)	IDDSB	VDD = 5.25V			TBD	uA

1. The supply current consumption depends upon the mode of operation selected.

TCLKIN Timing (See Figure 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TCLKIN Period (1)	tCK1			40		nS
TCLKIN Time Low	tCK2		8			nS
TCLKIN Time High	tCK3		8			nS
TCLKIN Transition Time	tCK4				5	nS

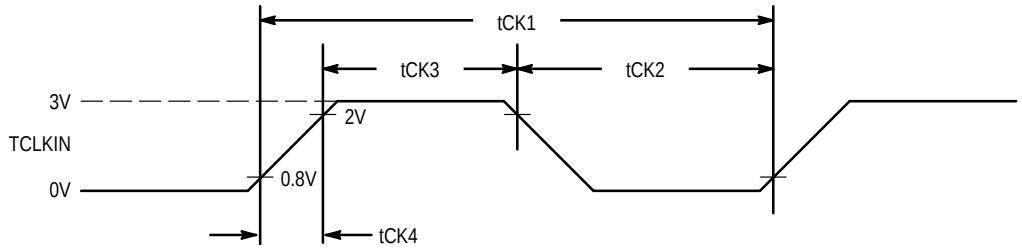


Figure 5. TCLKIN Input Voltage Levels for Timing Measurements

TP Transmit Switching Characteristics (See Figure 7)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Twisted Pair Differential Output Transition Time Zero to Positive	tTPT1	4.75V ≤ VDD ≤ 5.25V[1]		4		nS
Twisted Pair Differential Output Transition Time Zero to Negative	tTPT2	4.75V ≤ VDD ≤ 5.25V[1]		4		nS
Twisted Pair Differential Output Transition Time Positive to Zero	tTPT3	4.75V ≤ VDD ≤ 5.25V[1]		4		nS
Twisted Pair Differential Output Transition Time Negative to Zero	tTPT4	4.75V ≤ VDD ≤ 5.25V[1]		4		nS
Twisted Pair Differential Output Jitter	tTPT5	4.75V ≤ VDD ≤ 5.25V[1,2]		0.8		nS

1. Measured differentially across the output of test load A
2. Specification established by design and laboratory characterization

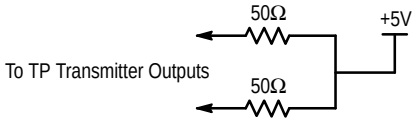


Figure 6. TP Tramitter Test Load

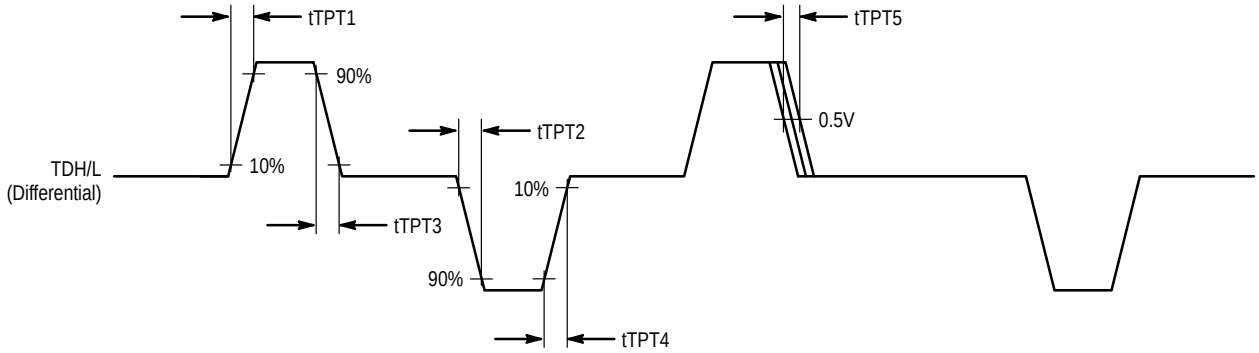


Figure 7. TDH/L Differential Twisted Pair Transmit Output Timing Characteristics
(NOTE: Specification established by design and laboratory characterization)

TP Transmit Switching Characteristics (See Figure 9)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Fiber Differential Output Transition Time Low to High	tFT1	4.75V ≤ VDD ≤ 5.25V	0.9		3	nS
Fiber Differential Output Transition Time High to Low	tFT2	4.75V ≤ VDD ≤ 5.25V	0.9		3	nS
Fiber Differential Output Jitter	tFT3	4.75V ≤ VDD ≤ 5.25V[1]			750	pS

1. Specification established by design and laboratory characterization

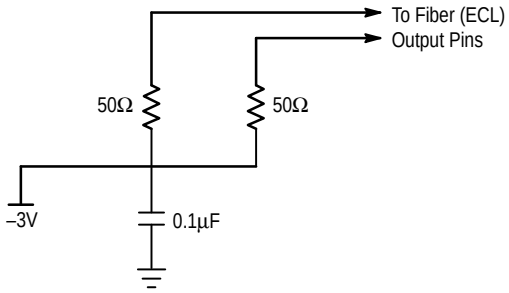


Figure 8. Fiber Differntial Driver Test Load

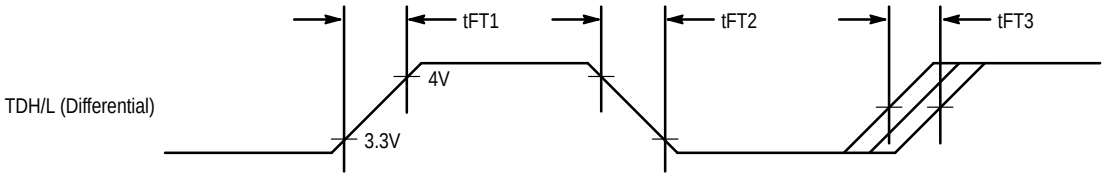


Figure 9. Fiber Transmit Driver Output Timings

Parallel Interface Timing (See Figure 11)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RSCLK Period	tPI1		36	40	44	nS
RSCLK Time Low	tPI2	**1**	18		22	nS
RSCLK Time High	tPI3	**1**	18		22	nS
Time to RDATA Invalid	tPI4		8			nS
Time to RDATA Valid	tPI5				32	nS
TCLKIN Period	tPI6		39		41	nS
TCLKIN Time Low	tPI7		18		22	nS
TCLKIN Time High	tPI8		18		22	nS
TDATA Setup Time	tPI10	**2**	12		40	nS
TDATA Hold Time	tPI11	**2**	0		28	nS

1. This parameter is specified with the receiver operating at 125 MHz.
2. This is with respect to TCLKIN

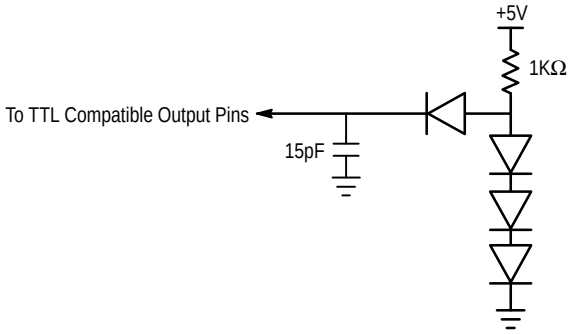


Figure 10. TTL Compatible Output AC Test Load

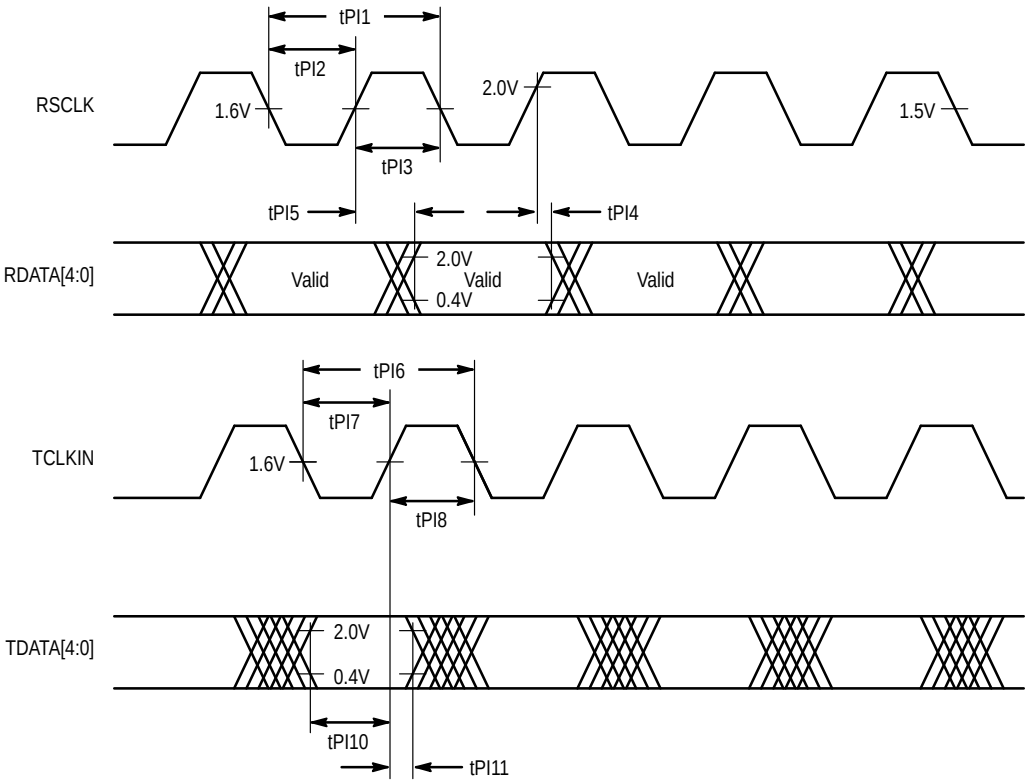
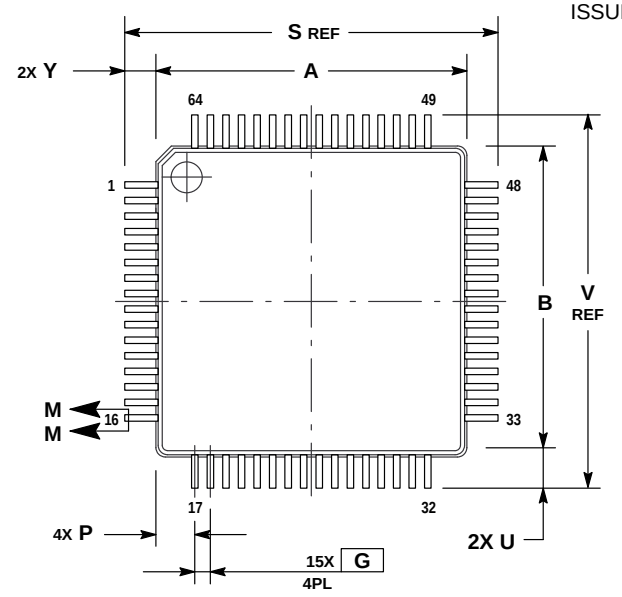
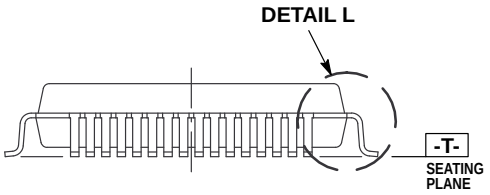


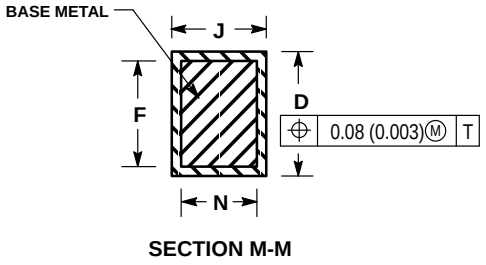
Figure 11. Parallel Interface Timing

OUTLINE DIMENSIONS

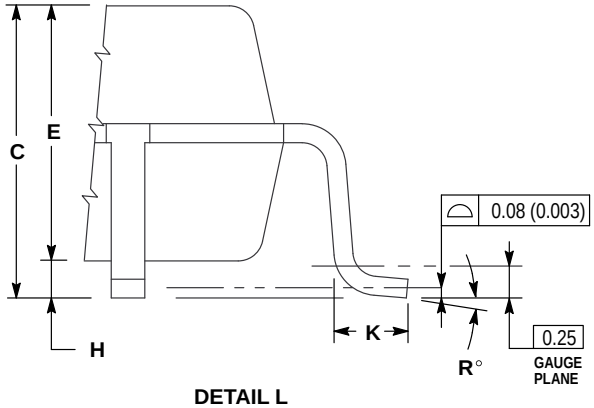
FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 931–02
ISSUE D







SECTION M-M



DETAIL L

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSTION. ALLOWABLE PROTRUSTION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED WHERE THE BOTTOM OF THE LEAD EXITS THE PLASTIC.
4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35 (0.014). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 (0.003).
5. AS PLATED SOLDER THICKNESS SHALL BE 0.0076 (0.0003) / 0.0203 (0.008).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	—	2.45	—	0.096
D	0.17	0.27	0.007	0.011
E	1.80	2.20	0.071	0.087
F	0.17	0.24	0.007	0.009
G	0.50 BSC		0.020 BSC	
H	—	0.35	—	0.014
J	0.09	0.20	0.004	0.008
K	0.45	0.75	0.018	0.030
N	0.09	0.16	0.004	0.006
P	1.20	1.30	0.047	0.051
R	0°	9°	0°	9°
S	12.00 REF		0.472 REF	
U	0.95	1.05	0.037	0.041
V	12.00 REF		0.472 REF	
Y	0.95	1.05	0.037	0.041

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