32K x 18 Bit Asynchronous/ Latched Address Fast Static RAM

The MCM67A518 is a 589,824 bit latched address static random access memory organized as 32,768 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates a 32K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active low chip enable, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address, data in, and chip enable latches are provided. When latch enables (AL for address and chip enables and DL for data in) are high, the address, data in, and chip enable latches are in the transparent state. If latch enables are tied high, the device can be used as an asynchronous SRAM. When latch enables are low, the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data—in hold time in a simple fashion.

Dual write enables ($\overline{\text{LW}}$ and $\overline{\text{UW}}$) are provided to allow individually writeable bytes. $\overline{\text{LW}}$ controls DQ0 – DQ8 (the lower bits) while $\overline{\text{UW}}$ controls DQ9 – DQ17 (the upper bits).

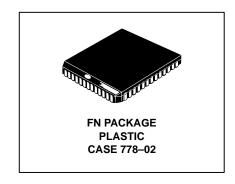
Additional power supply pins have been utilized and placed on the package for maximum performance.

The MCM67A518 will be available in a 52-pin plastic leaded chip carrier (PLCC).

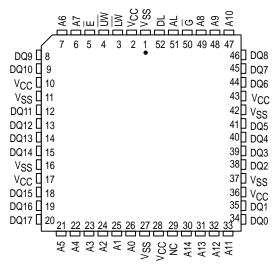
This device is ideally suited for systems which require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 10/12/15 ns Max
- Byte Writeable via Dual Write Enables
- Separate Data Input Latch for Simplified Write Cycles
- · Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- 3.3 V I/O Compatible
- · High Board Density 52-Lead PLCC Package

MCM67A518



PIN ASSIGNMENT



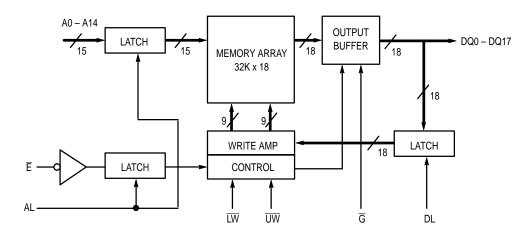
PIN NAMES
A0 - A14 Address Inputs AL Address Latch DL Data Latch \overline{\text{LW}} Lower Byte Write Enable \overline{\text{UW}} Higher Byte Write Enable \overline{\text{E}} Chip Enable \overline{\text{G}} Output Enable \overline{\text{DQ0}} - DQ17 Data Input/Output \text{VCC} +5 \text{V Power Supply} \text{VSS} Ground
NC

All power supply and ground pins must be connected for proper operation of the device.

REV 2 5/95



BLOCK DIAGRAM



TRUTH TABLE

Ē	LW	ŪW	AL*	DL*	G	Mode	Supply Current	I/O Status
Н	Х	Х	Х	Х	Х	Deselected Cycle	I _{SB}	High–Z
L	Х	Х	L	Х	Х	Read or Write Using Latched Addresses	lcc	_
L	Х	Х	Н	Х	Х	Read or Write Using Unlatched Addresses	lcc	_
L	Н	Н	Х	Х	L	Read Cycle	lcc	Data Out
L	Н	Н	Х	Х	Н	Read Cycle	lcc	High-Z
L	L	L	Х	L	Х	Write Both Bytes Using Latched Data In	lcc	High-Z
L	L	L	Х	Н	Х	Write Both Bytes Using Unlatched Data In	lcc	High-Z
L	L	Н	Х	Х	Х	Write Cycle, Lower Byte	Icc	High–Z
L	Н	L	Х	Х	Х	Write Cycle, Lower Byte	Icc	High-Z

^{*}E and Addresses satisfy the specified setup and hold times for the falling edge of AL. Data-in satisfies the specified setup and hold times for falling edge of DL.

NOTE: This truth table shows the application of each function. Combinations of these functions are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = 0$)

Rating	Symbol	Value	Unit
Power Supply Voltage	Vcc	- 0.5 to 7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V _{in} , V _{out}	- 0.5 to V _{CC} + 0.5	٧
Output Current (per I/O)	l _{out}	± 30	mA
Power Dissipation	PD	1.6	W
Temperature Under Bias	T _{bias}	- 10 to + 85	°C
Operating Temperature	TA	0 to + 70	°C
Storage Temperature	T _{stg}	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPER-ATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V \pm 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = 0 V$)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	Vcc	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3**	V
Input Low Voltage	V _{IL}	- 0.5*	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V _{in} = 0 to V _{CC})	l _{lkg(l)}	_	± 1.0	μΑ
Output Leakage Current (G = V _{IH})	llkg(O)	_	± 1.0	μΑ
AC Supply Current (\overline{G} = V _{IH} , I _{Out} = 0 mA, All Inputs = V _{IL} or V _{IH} , V _{IL} = 0.0 V and V _{IH} \geq 3.0, Cycle Time \geq t _{AVAV} min)	ICCA10 ICCA12 ICCA15	_	290 275 260	mA
AC Standby Current (\overline{E} = V _{IH} , I _{Out} = 0 mA, All Inputs = V _{IL} and V _{IH} , V _{IL} = 0.0 V and V _{IH} \geq 3.0 V, f = f _{max})	ISB1	_	75	mA
CMOS Standby Current $(\overline{E} \ge V_{CC} - 0.2$, All Inputs $\ge V_{CC} - 0.2$ V or ≤ 0.2 V, f = f _{max})	I _{SB2}	_	30	mA
Output Low Voltage (I _{OL} = + 8.0 mA)	VOL	_	0.4	V
Output High Voltage (I _{OH} = - 4.0 mA)	Voн	2.4	3.3	V

$\textbf{CAPACITANCE} \; (\text{f} = 1.0 \; \text{MHz}, \, \text{dV} = 3.0 \; \text{V}, \, \text{T}_{\mbox{A}} = 25 ^{\circ} \mbox{C}, \, \text{Periodically Sampled Rather Than 100\% Tested)} \; \\$

Characteristic	Symbol	Тур	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C _{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	C _{I/O}	6	8	pF

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^{*} V_{IL} (min) = -0.5 V dc; V_{IL} (min) = -2.0 V ac (pulse width ≤ 20 ns) for $I \le 20.0$ mA. ** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for $I \le 20.0$ mA.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = $5.0 \text{ V} \pm 10\%$, T_A = $0 \text{ to} + 70^{\circ}\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V	Output Timing Reference Level 1.5 V
Input Pulse Levels 0 to 3.0 V	Output Load Figure 1 Unless Otherwise Noted
Input Rise/Fall Time	

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1 and 2)

		MCM67A518-10 MCM67A518-12		MCM67A518-15					
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read Cycle Times	t _{AVAV}	10	_	12	_	15	_	ns	3
Access Times: Address Valid to Output Valid E Low to Output Valid Output Enable Low to Output Valid	tAVQV tELQV tGLQV	_ _ _	10 10 5	_ _ _	12 12 6	 - -	15 15 7	ns	4
Output Hold from Address Change	†AXQX	4	_	4	_	4	_	ns	
Output Buffer Control:	tELQX tGLQX tEHQZ tGHQZ	3 1 2 2	 5 5	3 1 2 2	 6 6	2 1 2 2	 9 7	ns	5
Power Up Time	^t ELICCA	0	_	0	_	0	_	ns	

NOTES:

- 1. AL and DL are equal to $V_{\mbox{\scriptsize IH}}$ for all asynchronous cycles.
- 2. Both Write Enable signals (\overline{LW} , \overline{UW}) are equal to V_{IH} for all read cycles.
- 3. All read cycle timing is referenced from the last valid address to the first transitioning address.
- 4. Addresses valid prior to or coincident with $\overline{\mathsf{E}}$ going low.
- 5. Transition is measured \pm 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

AC TEST LOADS

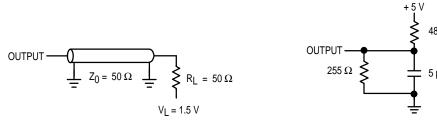
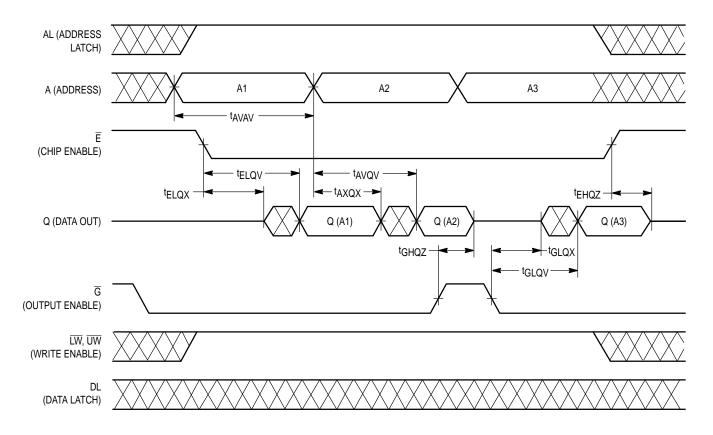


Figure 1A Figure 1B

ASYNCHRONOUS READ CYCLES



MOTOROLA FAST SRAM MCM67A518 5

ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, and 3)

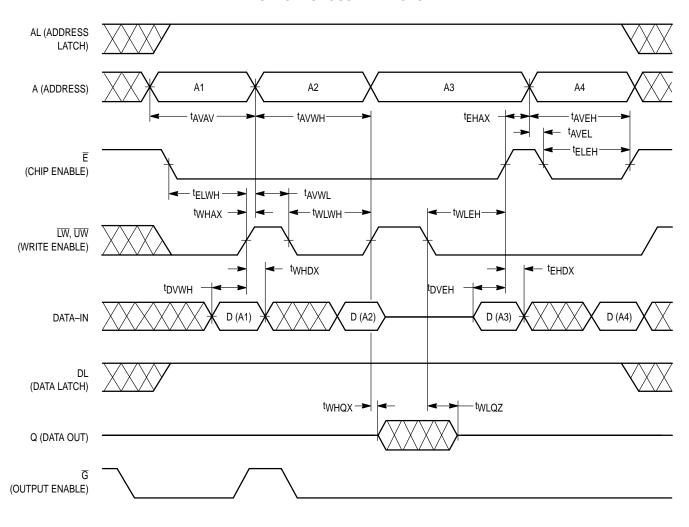
		MCM67	A518–10	MCM67A518-12		MCM67	A518–15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write Cycle Times	t _{AVAV}	10	_	12	_	15	_	ns	4
Setup Times: Address Valid to End of Write Address Valid to E High Address Valid to W Low Address Valid to E Low Address Valid to W High Data Valid E High	tavwh taveh tavwl tavel tdvwh tdveh	9 9 0 0 5 5	_ _ _ _ _	10 10 0 0 6 6		13 13 0 0 7 7		ns	
Hold Times: \overline{W} High to Address Invalid \overline{E} High to Address Invalid \overline{W} High to Data Invalid \overline{E} High to Data Invalid	^t WHAX ^t EHAX ^t WHDX ^t EHDX	0 0 0 0	_ _ _ _	0 0 0 0	 - - -	0 0 0 0	 - - -	ns	
Write Pulse Width: Write Pulse Width (\$\overline{G}\$ Low) Write Pulse Width (\$\overline{G}\$ High) Write Pulse Width Enable to End of Write Enable to End of Write	tWLWH tWLWH tWLEF tELWH tELEH	9 8 9 9	_ _ _ _ _	10 9 10 10	_ _ _ _ _	13 12 13 13	_ _ _ _ _	ns	5 6 5, 6
Output Buffer Control: \overline{W} High to Output Valid \overline{W} High to Output Active \overline{W} Low to Output High–Z	tWHQV tWHQX tWLQZ	10 3 0	_ _ 5	12 3 0	<u> </u>	15 5 0	<u> </u>	ns	7 7, 8

NOTES:

- 1. W (write) refers to either one or both byte write enables \overline{LW} and \overline{UW} .
- 2. AL and DL are equal to V_{IH} for all asynchronous cycles.
- 3. Both Write Enables must be equal to $V_{\mbox{\scriptsize IH}}$ for all address transitions.
- 4. All write cycle timing is referenced from the last valid address to the first transitioning address.
- 5. If \overline{E} goes high coincident with or before \overline{W} goes high the output will remain in a high impedance state.
- 6. If \overline{E} goes low coincident with or after \overline{W} goes low the output will remain in a high impedance state.
- 7. Transition is measured \pm 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
- 8. If \overline{G} goes low coincident with or after \overline{W} goes low the output will remain in a high impedance state.

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ASYNCHRONOUS WRITE CYCLE



MOTOROLA FAST SRAM MCM67A518

LATCHED READ CYCLE TIMING (See Notes 1 and 2)

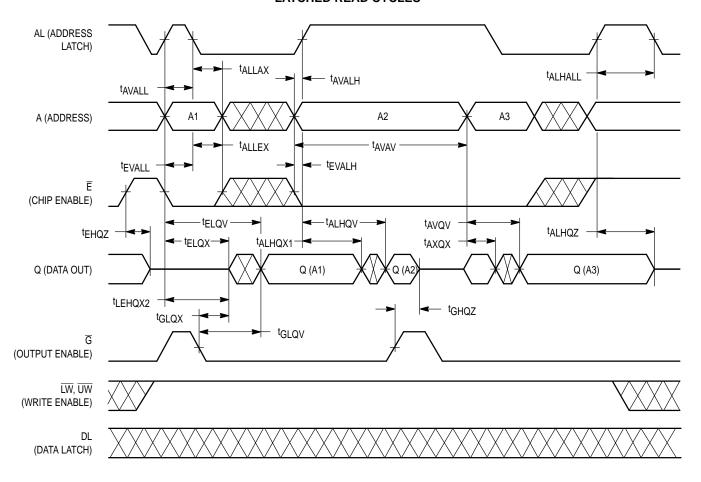
		MCM67A518-10		MCM67	A518–12	MCM67A518-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read Cycle Times	t _{AVAV}	10	_	12	_	15	_	ns	3
Access Times: Address Valid to Output Valid E Low to Output Valid AL High to Output Valid Output Enable Low to Output Valid	^t AVQV ^t ELQV ^t ALHQV ^t GLQV	_ _ _ _	10 10 10 5	_ _ _ _	12 12 12 6	 	15 15 15 7	ns	3 4
Setup Times: Address Valid to AL Low E Valid to AL Low Address Valid to AL High E Valid to AL High	[†] AVALL [†] EVALL [†] AVALH [†] EVALH	2 2 0 0	_ _ _ _	2 2 0 0	_ _ _ _	2 2 0 0	_ _ _ _	ns	4 4
Hold Times: AL Low to Address Invalid AL Low to E Invalid	[†] ALLAX [†] ALLEX	2 2		2 2	_	3 3	_	ns	4
Output Hold: Address Invalid to Output Invalid AL High to Output Invalid	[†] AXQX [†] ALHQX1	4 4	_ _	4 4	_ _	4 4	_ _	ns	
Address Latch Pulse Width	^t ALHALL	5	_	5	_	5	_	ns	
Output Buffer Control: \(\overline{E}\) Low to Output Active \(\overline{G}\) Low to Output Active \(AL\) High to Output Active \(\overline{E}\) High to Output High–Z \(AL\) High to Output High–Z \(\overline{G}\) High to Output High–Z	[†] ELQX [†] GLQZ [†] ALHQX2 [†] EHQZ [†] ALHQZ [†] GHQZ	3 1 3 2 2 2		3 1 3 2 2 2	— — 6 6 6	2 1 2 2 2 2	— — 9 9 7	ns	5

NOTES:

- 1. Both Write Enable Signals (\overline{LW} , \overline{UW}) are equal to V_{IH} for all read cycles.
- 2. All read cycle timing is referenced from the last valid address to the first transitioning address.
- 3. Addresses valid prior to or coincident with $\overline{\mathsf{E}}$ going low.
- 4. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
- 5. Transition is measured \pm 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, tehQZ is less than tehQZ is less than tehQZ is less than tehQZ and tehQZ is less than tehQZ for a given device.

MCM67A518 MOTOROLA FAST SRAM

LATCHED READ CYCLES



MOTOROLA FAST SRAM MCM67A518

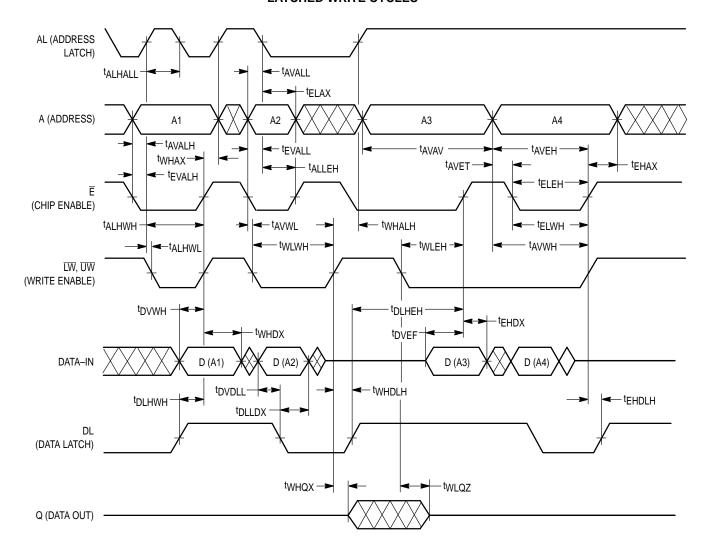
LATCHED WRITE CYCLE TIMING (See Notes 1, 2, and 3)

		MCM67	A518–10	MCM67	A518–12	MCM67	MCM67A518-15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write Cycle Times: Address Valid to Address Valid	^t AVAV	10	_	12	_	15	_	ns	4
Setup Times: Address Valid to End of Write Address Valid to End of Write E Valid to AL Low Address Valid to AL Low E Valid to AL High Address Valid to AL High AL High to W Low Address Valid to E Low Data Valid to DL Low Data Valid to E High DL High to W High DL High to High	tavwh taveh tevall tavalh tavalh tavalh talhwl tavwl tavel tDVDLL tDVWH tDLHWH tDLHEH	9 9 2 2 0 0 0 0 2 5 5		10 10 2 2 0 0 0 0 0 2 6 6 6		13 13 2 2 0 0 0 0 0 2 7 7		ns	
Hold Times: AL Low to E High AL Low to Address Invalid DL Low to Data Invalid W High to Address Invalid E High to Address Invalid W High to Data Invalid E High to Data Invalid W High to DL High High to DL High W High to AL High	tALLEH tALLAX tDLLDX tWHAX tEHAX tEHAX tWHDX tEHDX tWHDLH tEFDLH tWHALH	2 2 2 0 0 0 0 0 0		2 2 2 0 0 0 0 0 0		3 3 3 0 0 0 0 0		ns	4 4
Write Pulse Width: AL High to W High Write Pulse Width (G Low) Write Pulse Width (G High) Write Pulse Width Enable to End of Write Enable to End of Write	talhwh twlwh twlwh twleh telwh teleh	9 9 8 9 9	_ _ _ _ _	10 10 9 10 10	_ _ _ _ _	13 13 12 13 13	_ _ _ _ _	ns	5 6 7 6, 7
Address Latch Pulse Width	^t ALHALL	5	_	12	_	15	_	ns	4
Output Buffer Control: \overline{\pi} \text{ High to Output Valid} \overline{\pi} \text{ High to Output Active} \overline{\pi} \text{ Low to Output High-Z}	^t WHQV ^t WHQX ^t WLQZ	10 3 0	_ _ 5	12 3 0	<u> </u>	15 5 0	<u>—</u> 9	ns	8 8, 9

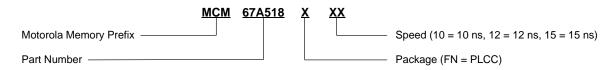
NOTES:

- 1. W (write) refers to either one or both byte write enables \overline{LW} and \overline{UW} .
- 2. A write occurs during the overlap of \overline{E} low and \overline{W} low.
- 3. Both Write Enables must be equal to VIH for all address transitions.
- 4. All write cycle timing is referenced from the last valid address to the first transitioning address.
- 5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
- 6. If \overline{E} goes high coincident with or before \overline{W} goes high the output will remain in a high impedance state.
- 7. If \overline{E} goes low coincident with or after \overline{W} goes low the output will remain in a high impedance state.
- 8. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, two is less than two a given device.
- 9. If \overline{G} goes low coincident with or after \overline{W} goes low the output will remain in a high impedance state.

LATCHED WRITE CYCLES



ORDERING INFORMATION (Order by Full Part Number)



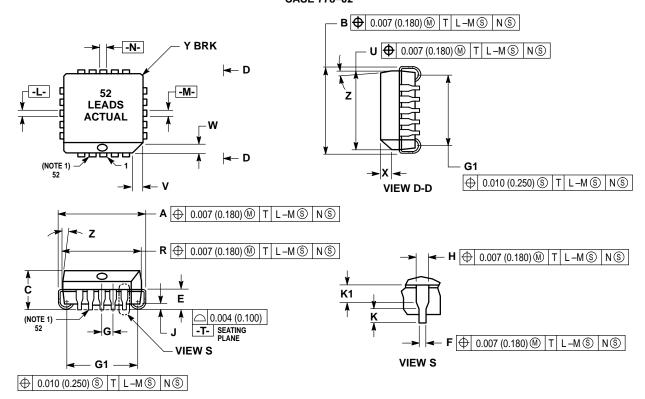
Full Part Numbers — MCM67A518FN10 MCM67A518FN12 MCM67A518FN15

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MOTOROLA FAST SRAM MCM67A518

PACKAGE DIMENSIONS

FN PACKAGE 52-LEAD PLCC **CASE 778-02**



- 1. DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE
 OUTLINE DRAWING RATHER THAN SHOWING ALL 52
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD
- PARTING LINE.
 DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- 4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

 DIMENSION H DOES NOT INCLUDE DAMBAR
 BOOTHIS
- PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIN	METERS
DIM	MIN	MAX	MIN	MAX
Α	0.785	0.795	19.94	20.19
В	0.785	0.795	19.94	20.19
С	0.165	0.180	4.20	4.57
Е	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.05	0 BSC	1.27	BSC
Н	0.026	0.032	0.66	0.81
J	0.020	_	0.51]
K	0.025	_	0.64	
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
Х	0.042	0.056	1.07	1.42
Υ	_	0.020	_	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	_	1.02	_

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USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

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