MCM64T116

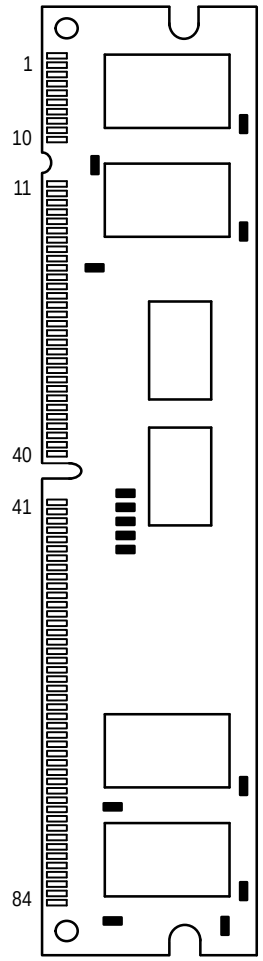
Product Preview

1M x 64 Bit Dynamic Random Access Memory Module

The MCM64T116 is a dynamic random access memory (DRAM) module organized as 1,048,576 x 64 bits. The module is a JEDEC–standard 168–lead dual–in–line memory module (DIMM) with 84 separate contacts per side, consisting of four MCM518160A DRAMs housed in standard 400–mil packages (TSOP), mounted on a substrate along with two 0.22 µF (min) decoupling capacitors mounted adjacent to each DRAM. Buffering is provided for address and all clock pins except RAS. The MCM518160A is a CMOS high speed dynamic random access memory organized as 1,048,576 sixteen–bit words and fabricated with CMOS silicon–gate process technology.

- Three–State Data Output
- Early–Write Common I/O Capability
- Fast Page Mode Capability
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 1024 Cycle Refresh: 16 ms (Max)
- Consists of Four 1M x 16 DRAMs, Eight 0.22 µF (Min) Decoupling Capacitors, and Two 16–Bit Buffers
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Presence Detect Enable (PDE) Controls Access to 8 Bits of Buffered PD Information
- Notch Keys Prevent Accidental Insertion in Low Voltage (3.3 V) Systems
- Fast Access Time (t_{RAC}): MCM64T116–60 = 60 ns (Max)
  MCM64T116–70 = 70 ns (Max)
- Low Active Power Dissipation: MCM64T116–60 = 828 mW (Max)
  MCM64T116–70 = 700 mW (Max)
- Low Standby Power Dissipation: TTL Levels = 80 mW (Max)
  CMOS Levels = 76 mW (Max)

D PACKAGE
DIMM MODULE
CASE 1115B–01



PIN NAMES	
A0, B0, A1 – A9 . . . . . Address Inputs	DQ0 – DQ70* . . . . . Data Input/Output
CAS0 – CAS7 . . Column Address Strobe	RAS0, RAS2 . . . Row Address Strobe
WE0, WE2 . . . . . Write Enable	G0, G2 . . . . . Output Enable
PD1 – PD8 . . . Buffered Presence Detect	ID0, ID1 . . . . . Unbuffered ID Bit
PDE . . . . Presence Detect Output Enable	V_{CC} . . . . . Power (+ 5 V)
V_{SS} . . . . . Ground	NC . . . . . No Connection

*DQ8, DQ17, DQ26, DQ35, DQ44, DQ53, and DQ62 are not present on 64 bit modules.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

10/95

1M x 64 168 DIMM Pinout

Front Side								Back Side							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	22	NC	43	V_{SS}	64	NC	85	V_{SS}	106	NC	127	V_{SS}	148	NC
2	DQ0	23	V_{SS}	44	G2	65	DQ25	86	DQ36	107	V_{SS}	128	NC	149	DQ61
3	DQ1	24	NC	45	$\overline{RAS2}$	66	NC	87	DQ37	108	NC	129	NC	150	NC
4	DQ2	25	NC	46	$\overline{CAS4}$	67	DQ27	88	DQ38	109	NC	130	$\overline{CAS5}$	151	DQ63
5	DQ3	26	V_{CC}	47	$\overline{CAS6}$	68	V_{SS}	89	DQ39	110	V_{CC}	131	$\overline{CAS7}$	152	V_{SS}
6	V_{CC}	27	$\overline{WE0}$	48	$\overline{WE2}$	69	DQ28	90	V_{CC}	111	NC	132	PDE	153	DQ64
7	DQ4	28	$\overline{CAS0}$	49	V_{CC}	70	DQ29	91	DQ40	112	$\overline{CAS1}$	133	V_{CC}	154	DQ65
8	DQ5	29	$\overline{CAS2}$	50	NC	71	DQ30	92	DQ41	113	$\overline{CAS3}$	134	NC	155	DQ66
9	DQ6	30	RAS0	51	NC	72	DQ31	93	DQ42	114	NC	135	NC	156	DQ67
10	DQ7	31	G0	52	DQ18	73	V_{CC}	94	DQ43	115	NC	136	DQ54	157	V_{CC}
11	NC	32	V_{SS}	53	DQ19	74	DQ32	95	NC	116	V_{SS}	137	DQ55	158	DQ68
12	V_{SS}	33	A0	54	V_{SS}	75	DQ33	96	V_{SS}	117	A1	138	V_{SS}	159	DQ69
13	DQ9	34	A2	55	DQ20	76	DQ34	97	DQ45	118	A3	139	DQ56	160	DQ70
14	DQ10	35	A4	56	DQ21	77	NC	98	DQ46	119	A5	140	DQ57	161	NC
15	DQ11	36	A6	57	DQ22	78	V_{SS}	99	DQ47	120	A7	141	DQ58	162	V_{SS}
16	DQ12	37	A8	58	DQ23	79	PD1	100	DQ48	121	A9	142	DQ59	163	PD2
17	DQ13	38	NC	59	V_{CC}	80	PD3	101	DQ49	122	NC	143	V_{CC}	164	PD4
18	V_{CC}	39	NC	60	DQ24	81	PD5	102	V_{CC}	123	NC	144	DQ60	165	PD6
19	DQ14	40	V_{CC}	61	NC	82	PD7	103	DQ50	124	V_{CC}	145	NC	166	PD8
20	DQ15	41	NC	62	NC	83	ID0	104	DQ51	125	NC	146	NC	167	ID1
21	DQ16	42	NC	63	NC	84	V_{CC}	105	DQ52	126	B0	147	NC	168	V_{CC}

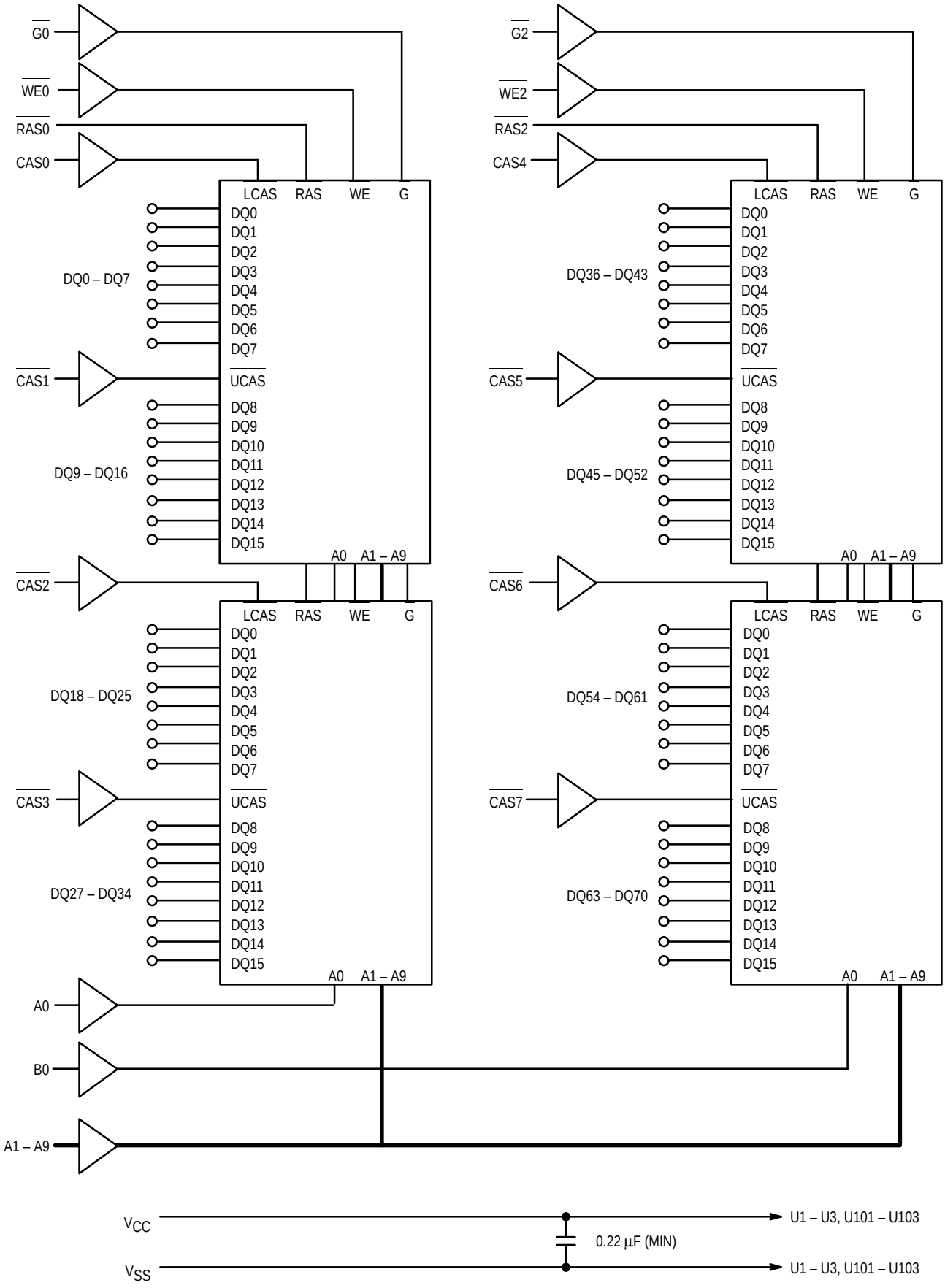
NOTE: Contact your Motorola representative for additional information on the availability of other configurations and densities of modules in the new 168 pin DIMM family.

Presence Detect/ID Bit Populations

Pin Name	60 ns	70 ns
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	NC
PD4	V_{SS}	V_{SS}
PD5	V_{SS}	V_{SS}
PD6	NC	V_{SS}
PD7	NC	NC
PD8	NC	NC
ID0	V_{SS}	V_{SS}
ID1	V_{SS}	V_{SS}

NOTE: PDs and IDs must each be pulled up through a resistor to V_{CC} at the next higher level of assembly. PDs are buffered and gated to the edge connector by the PDE (Presence Detect Enable) signal.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	11.3	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5	—	0.8	V

DC CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM64T116–60, t_{RC} = 110 ns MCM64T116–70, t_{RC} = 130 ns	I_{CC1}	— —	828 700	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{IH})		I_{CC2}	—	80	mA	
V_{CC} Power Supply Current During RAS only Refresh Cycles	MCM64T116–60, t_{RC} = 110 ns MCM64T116–70, t_{RC} = 130 ns	I_{CC3}	— —	812 686	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle	MCM64T116–60, t_{PC} = 45 ns MCM64T116–70, t_{PC} = 45 ns	I_{CC4}	— —	525 485	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{CC} – 0.2 V)		I_{CC5}	—	76	mA	
V_{CC} Power Supply Current During CAS Before RAS Refresh Cycle	MCM64T116–60, t_{RC} = 110 ns MCM64T116–70, t_{RC} = 130 ns	I_{CC6}	— —	828 700	mA	1
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)		$I_{lkg(I)}$	– 20	+ 20	µA	
Output Leakage Current (CAS at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)		$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column Address can be changed once or less while RAS = V_{IL} and CAS = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance	A0 – A9, G, CAS, W, PDE RAS	C_{11} C_{12}	—	16 24	pF
I/O Capacitance	DQ0 – DQ31	C_{DQ}	—	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 55°C, Unless Otherwise Noted)

READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM64T116–60		MCM64T116–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	5
Read–Write Cycle Time	t_{RELREL}	t_{RWC}	155	—	180	—	ns	5
Access Time from RAS	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7
Access Time from CAS	t_{CELQV}	t_{CAC}	—	22	—	27	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	37	—	42	ns	6, 9
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	42	—	47	ns	6
CAS to Output in Low–Z	t_{CELQX}	t_{CLZ}	2	—	2	—	ns	6
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	2	22	2	22	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
RAS Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	22	—	27	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	58	—	68	—	ns	
CAS Precharge to RAS Hold Time	t_{CEHREH}	t_{RHCP}	42	—	47	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	15	10 k	20	10 k	ns	
RAS to CAS Delay Time	t_{RELCEL}	t_{RCD}	18	37	18	43	ns	11
RAS to Column Address Delay Time	t_{RELAV}	t_{RAD}	13	23	13	28	ns	12
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	12	—	12	—	ns	
CAS Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	7	—	7	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	8	—	8	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	2	—	2	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	15	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	37	—	42	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	2	—	2	—	ns	
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	2	—	2	—	ns	13
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

READ, WRITE, AND READ–WRITE CYCLES (Continued)

Parameter	Symbol		MCM64T116–60		MCM64T116–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	22	—	27	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	15	—	20	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	2	—	2	—	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	17	—	22	—	ns	14
Write Command Setup Time	t_{WLCEL}	t_{WCS}	2	—	2	—	ns	15
CAS to Write Delay	t_{CELWL}	t_{CWD}	42	—	47	—	ns	15
RAS to Write Delay	t_{RELWL}	t_{RWD}	92	—	102	—	ns	15
Column Address to Write Delay	t_{AVWL}	t_{AWD}	62	—	67	—	ns	15
Refresh Period	t_{RVRV}	t_{RFSH}	—	16	—	16	ms	
CAS Setup Time for CAS Before RAS Refresh	t_{RELCEL}	t_{CSR}	7	—	7	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	8	—	13	—	ns	
RAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
CAS Precharge Time for CAS Before RAS Counter Time	t_{CEHCEL}	t_{CPT}	20	—	30	—	ns	
RAS Hold Time Referenced to G	t_{GLREH}	t_{ROH}	8	—	8	—	ns	
G Access Time	t_{GLQV}	t_{GA}	—	22	—	27	ns	
G to Data Delay	t_{GLHDX}	t_{GD}	22	—	22	—	ns	
Output Buffer Turn–Off Delay Time from G	t_{GLHQZ}	t_{GZ}	2	13	2	13	ns	16
G Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	ns	
Output Disable Setup Time	t_{GHCEL}	t_{GDS}	2	—	2	—	ns	
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
PDE to Valid Presence Detect		t_{PD}	2	10	2	10	ns	
PDE Inactive to Presence Detects Inactive		t_{PDOFF}	2	10	2	10	ns	

NOTES:

14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write or read–write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
16. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

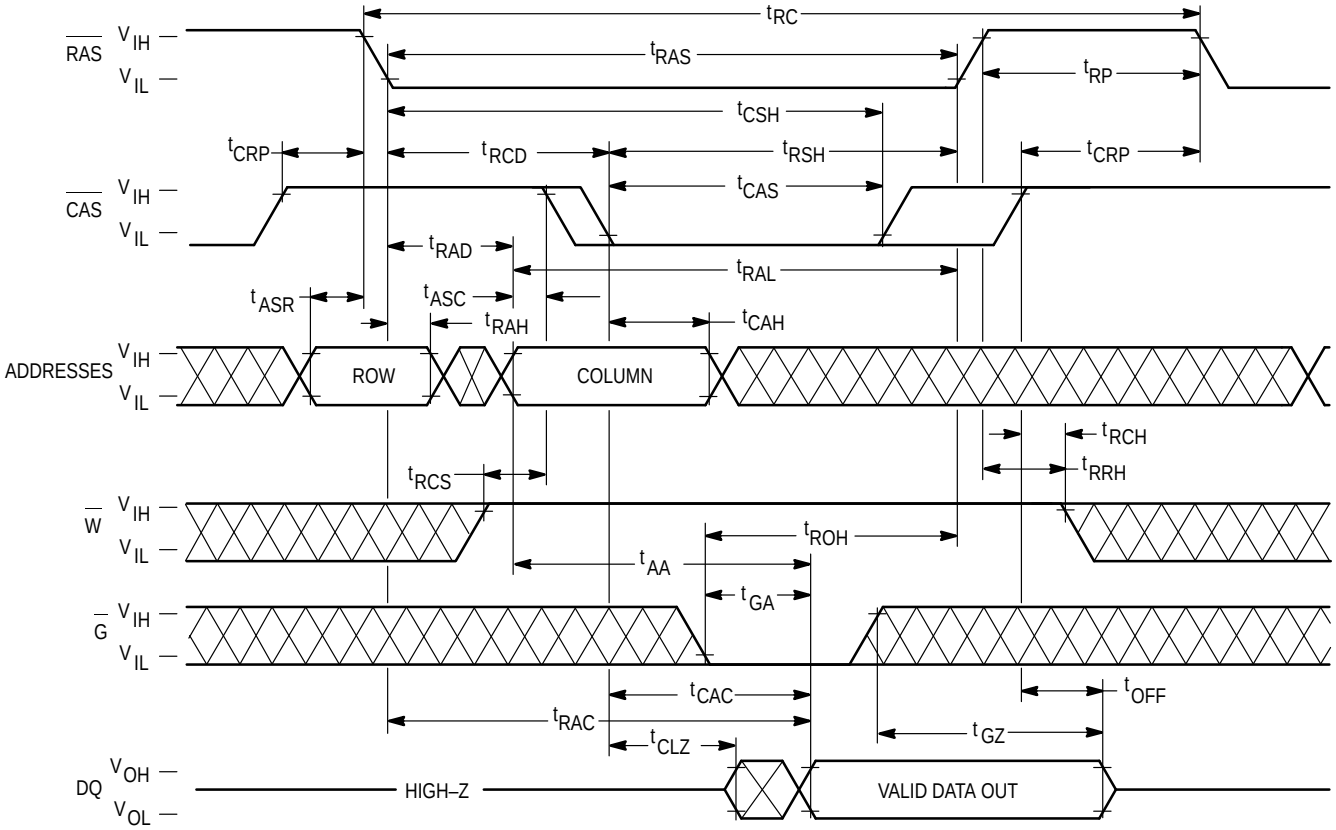
FAST PAGE MODE READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM64T116–60		MCM64T116–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
CAS Precharge to RAS Hold Time (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
Fast Page Mode Read–Write Cycle Time	t_{CELCEL}	t_{PRWC}	85	—	90	—	ns	
RAS Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100 k	70	200 k	ns	
CAS Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	62	—	67	—	ns	15

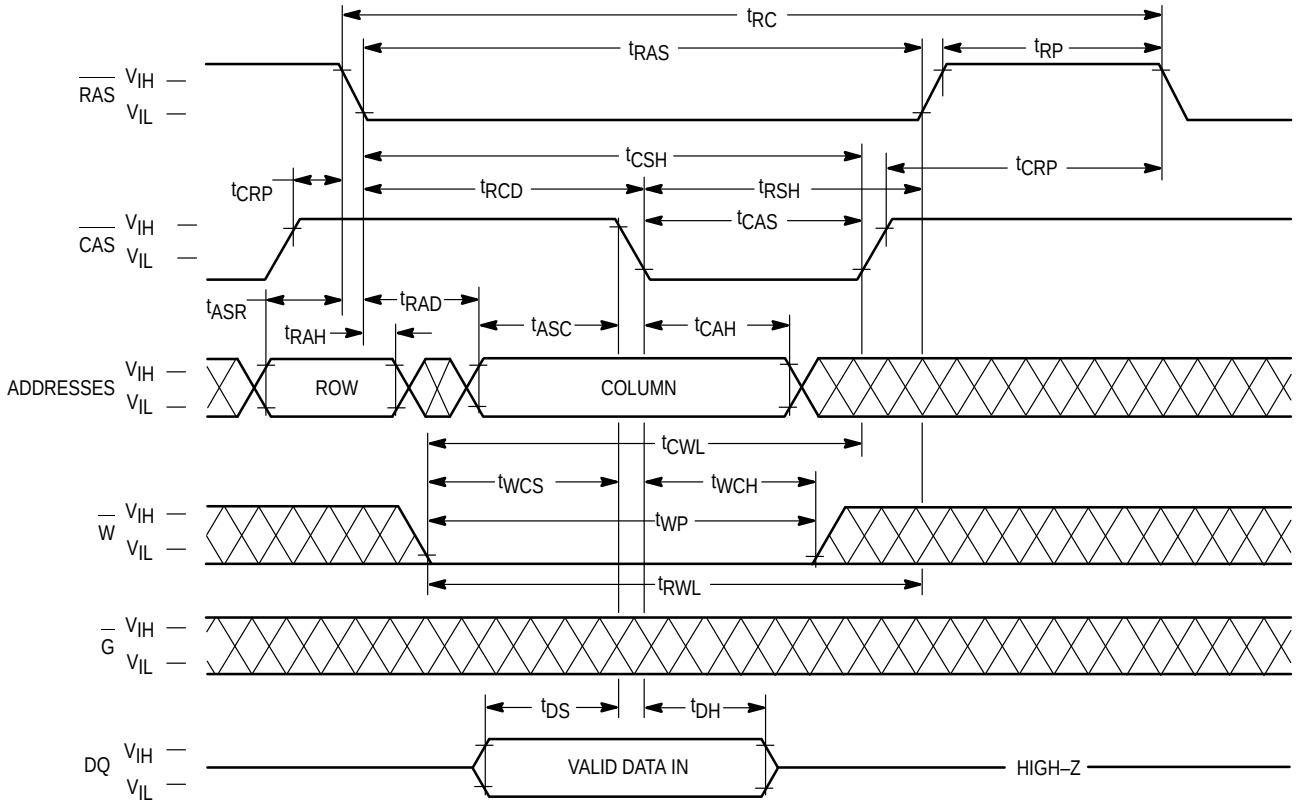
NOTES:

1. $_{IH}$ (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through–out the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

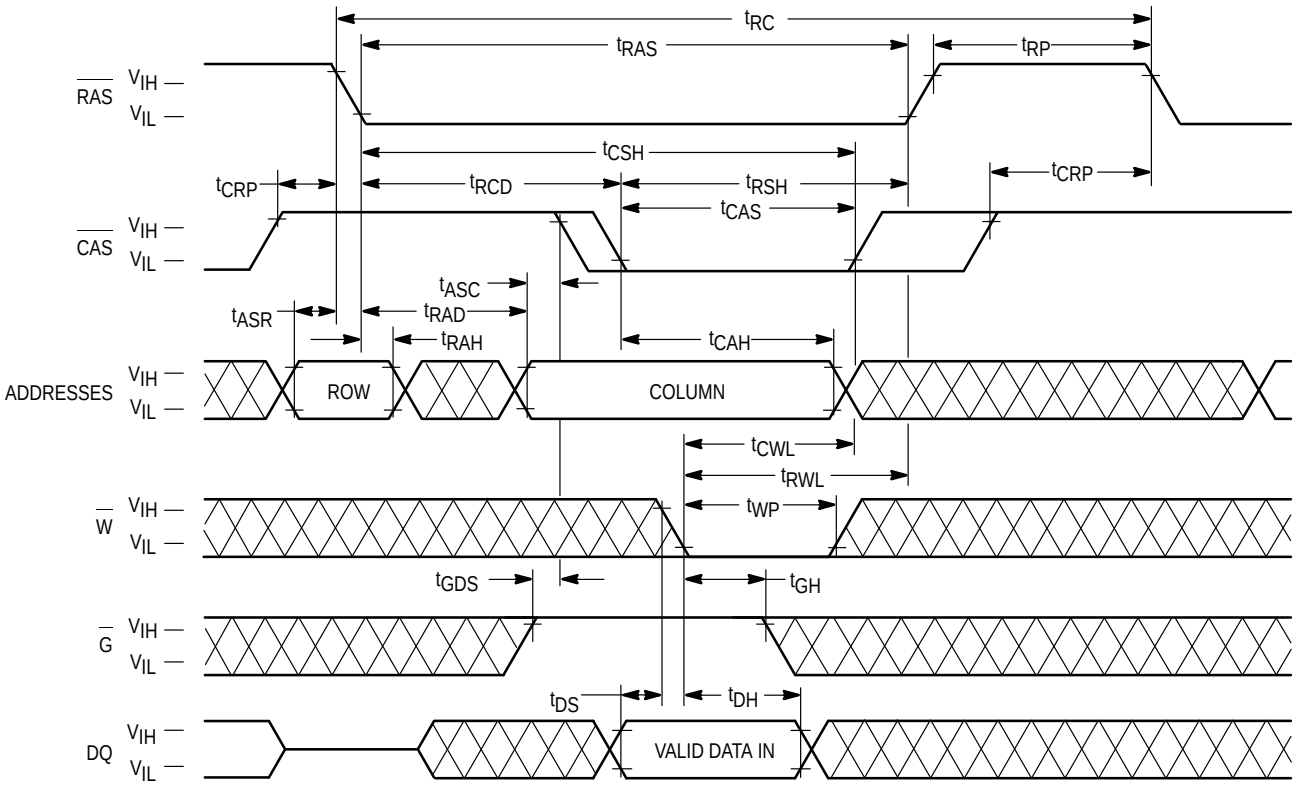
READ CYCLE (FAST PAGE MODE)



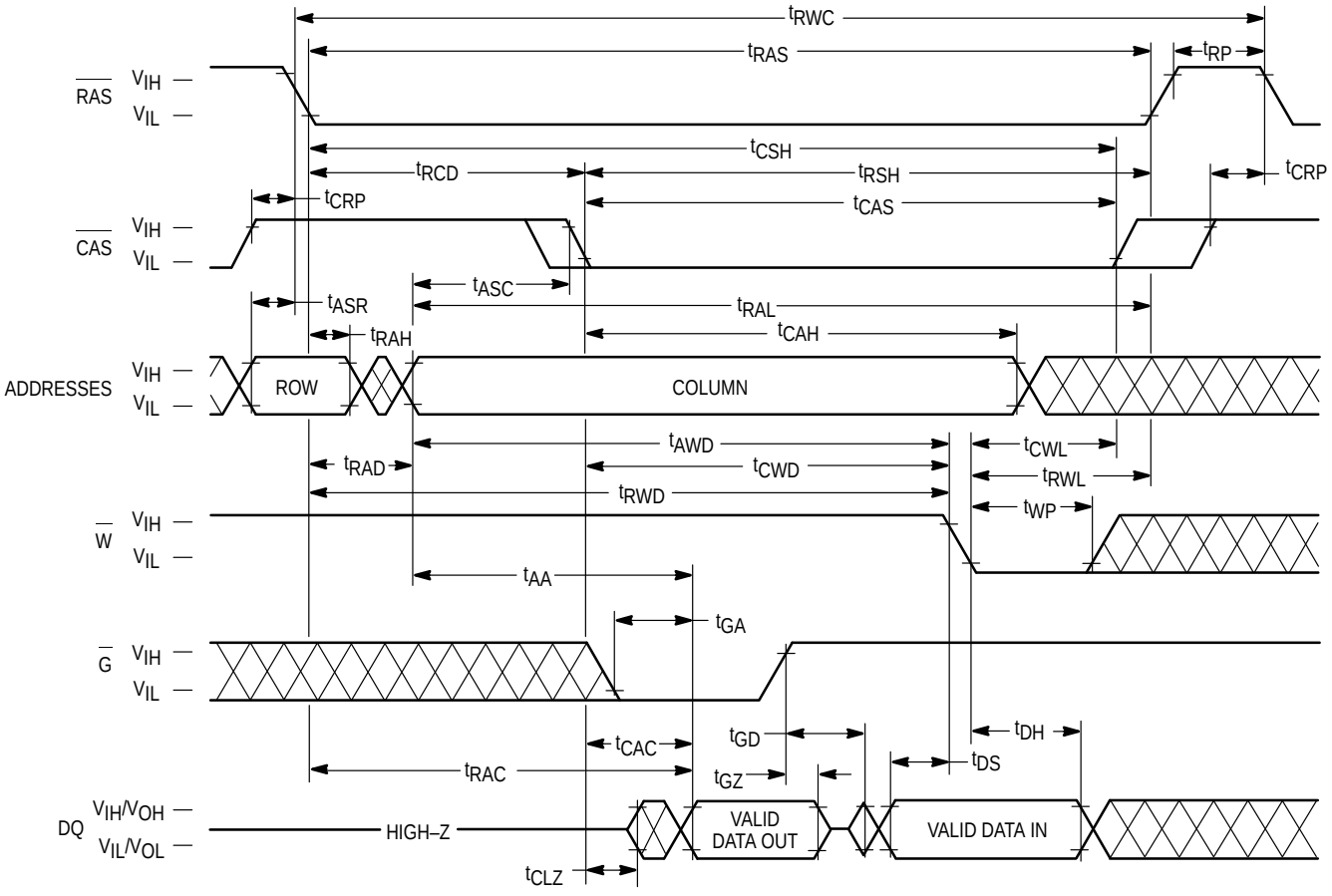
EARLY WRITE CYCLE



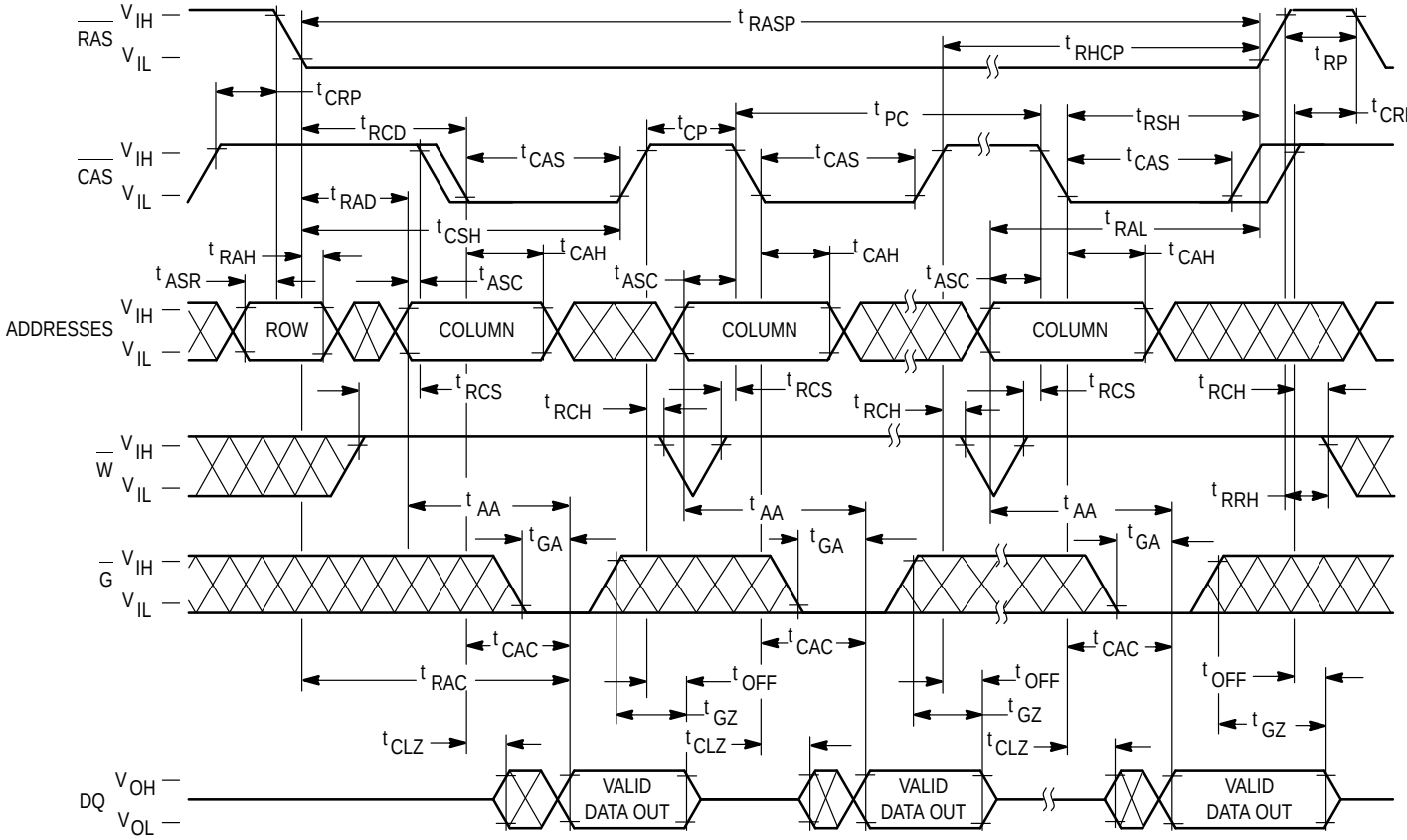
$\overline{G}$ CONTROLLED LATE WRITE CYCLE



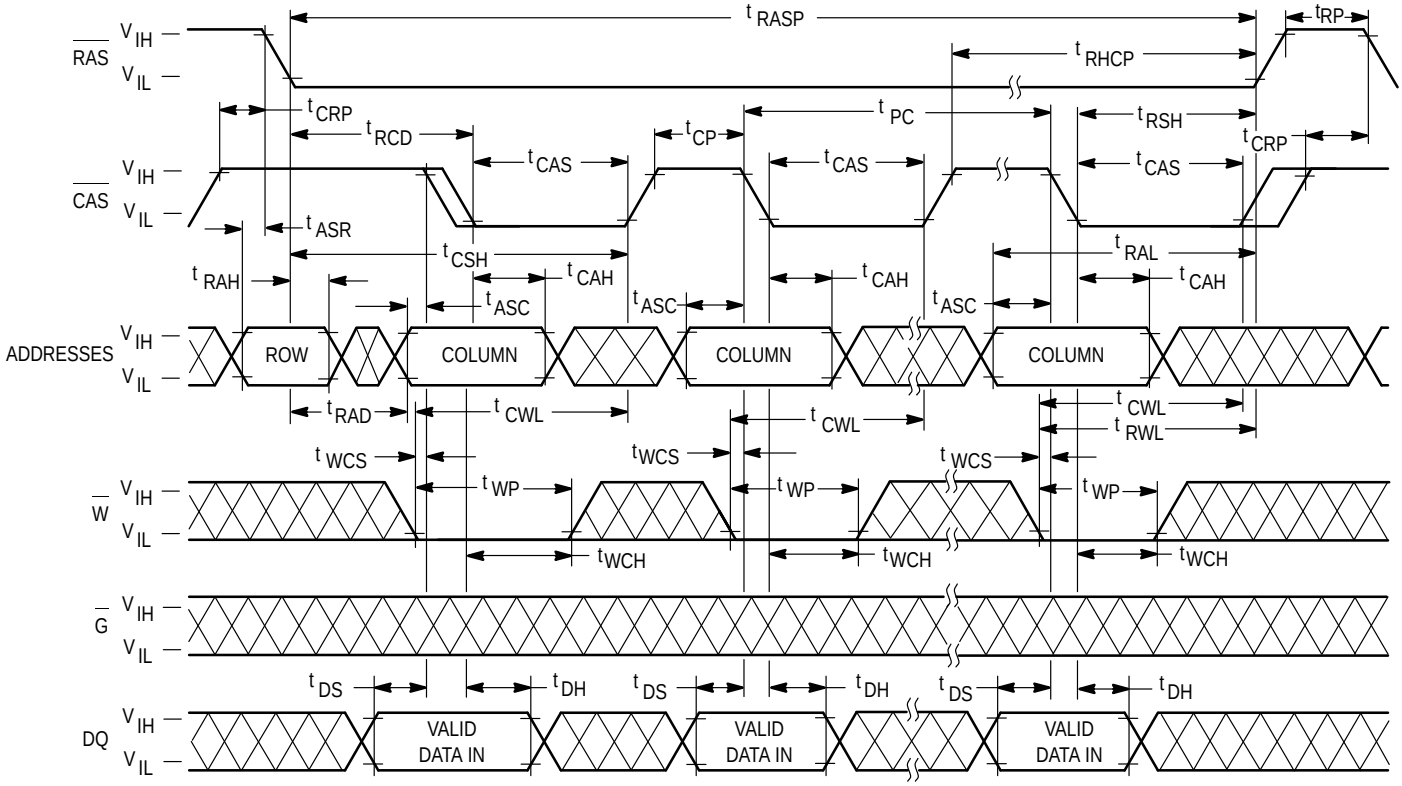
READ–WRITE CYCLE



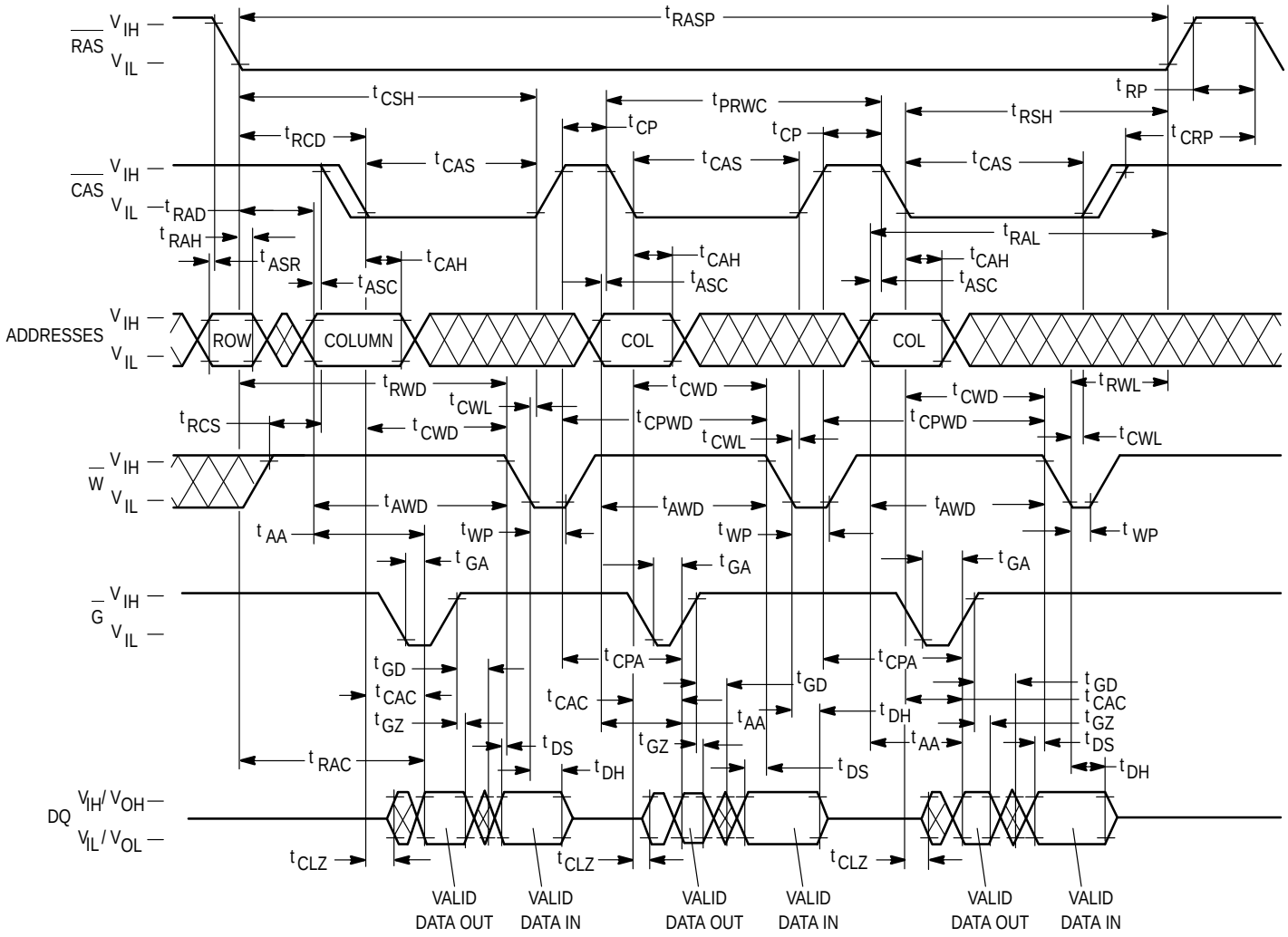
FAST PAGE MODE READ CYCLE



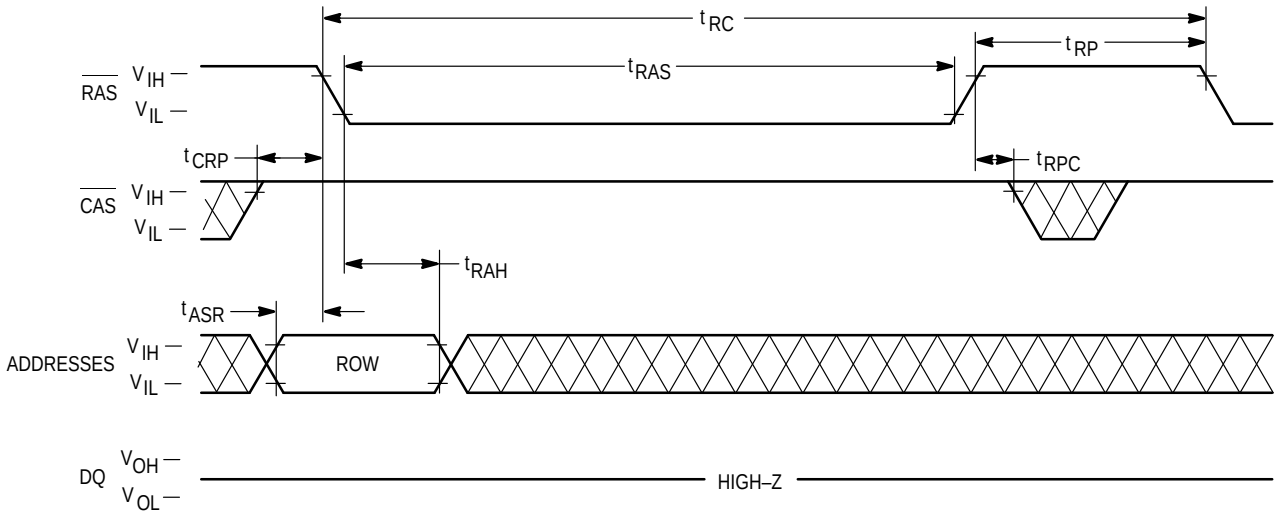
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ–WRITE CYCLE

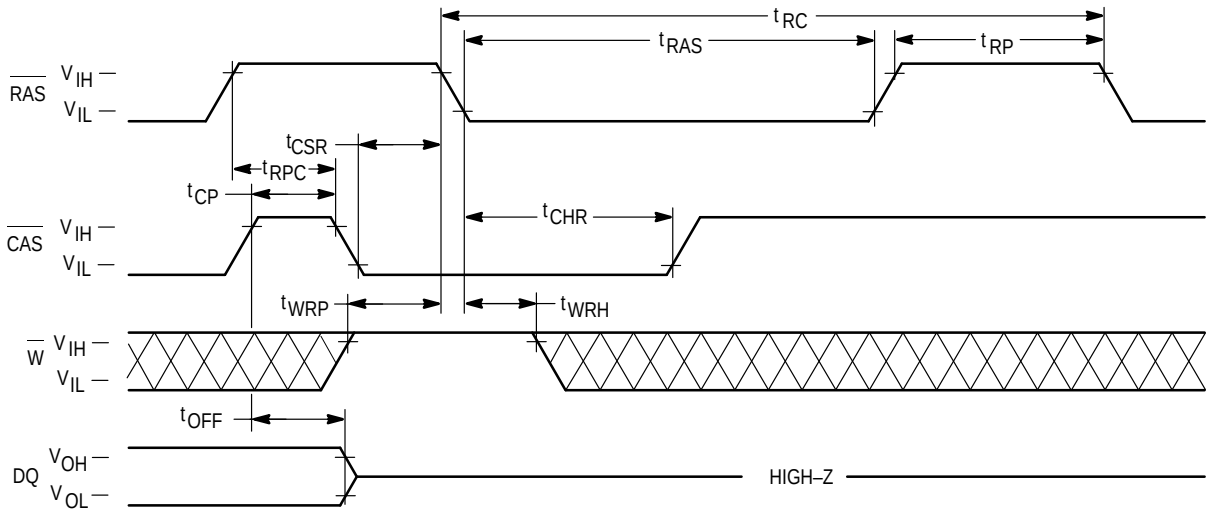


RAS–ONLY REFRESH CYCLE
(W and G are Don't Care)

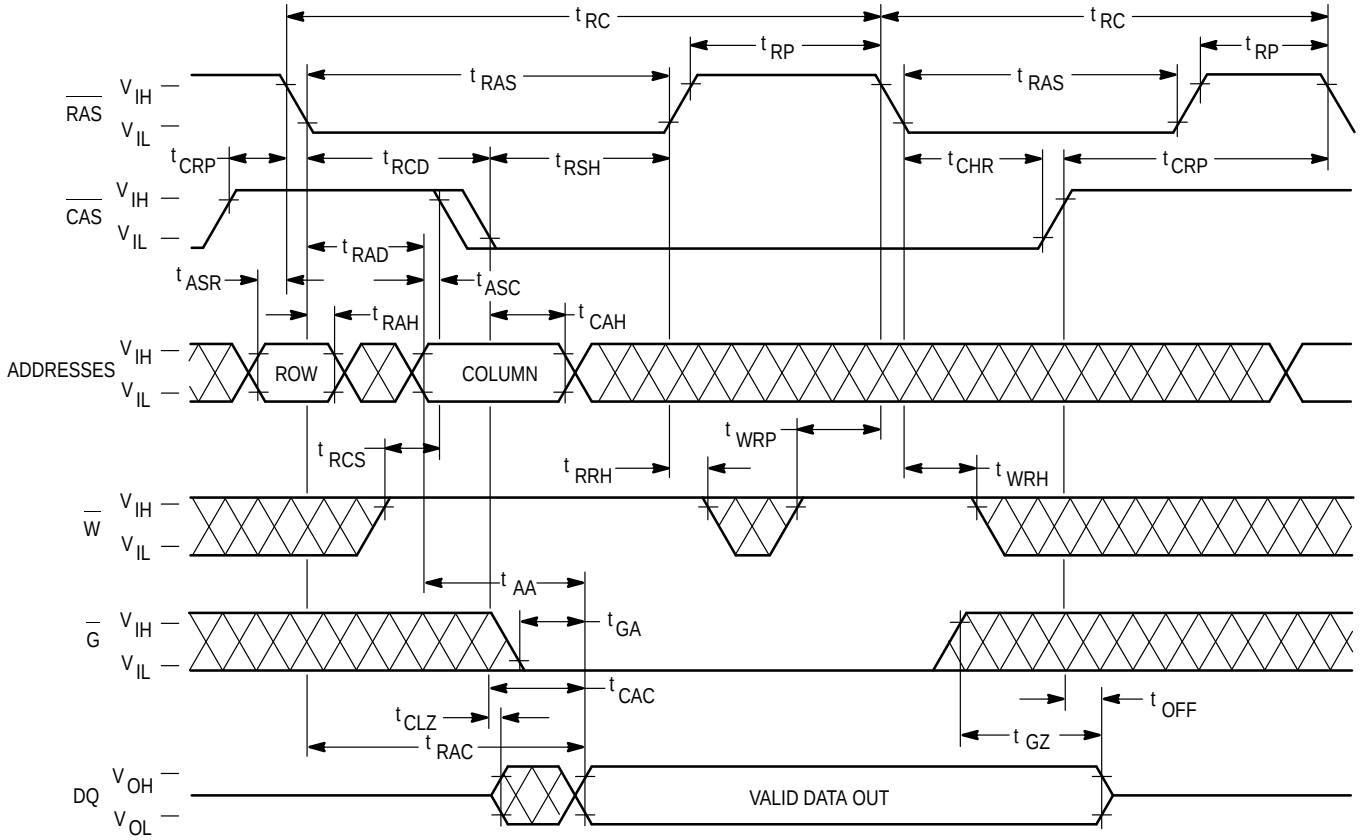


$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

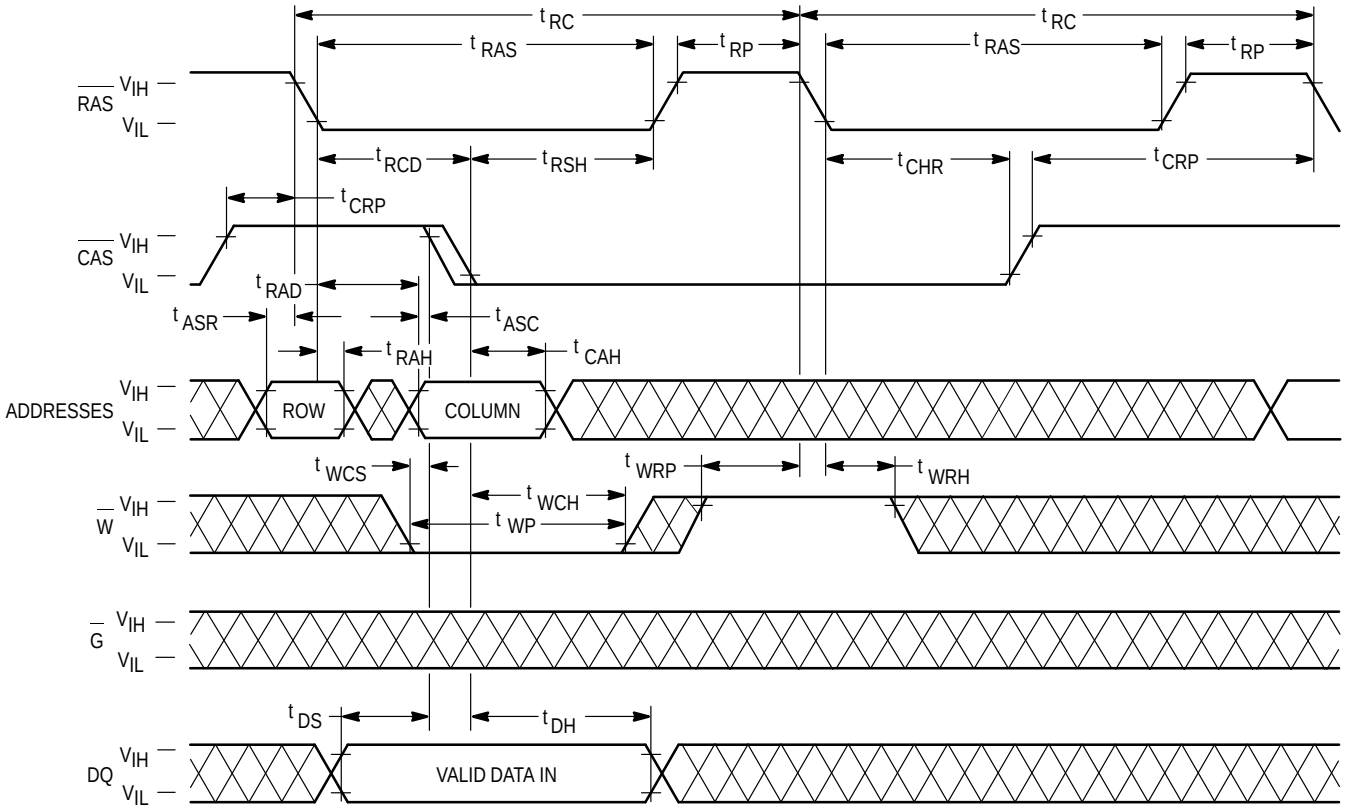
(G and A0 – A10 are Don't Care)



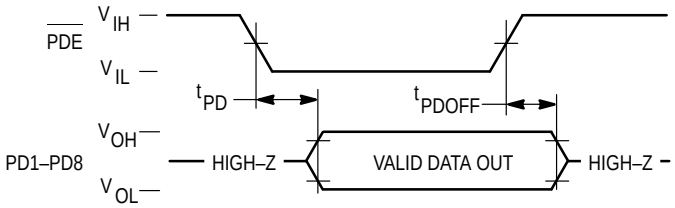
HIDDEN REFRESH CYCLE (READ) (FAST PAGE MODE)



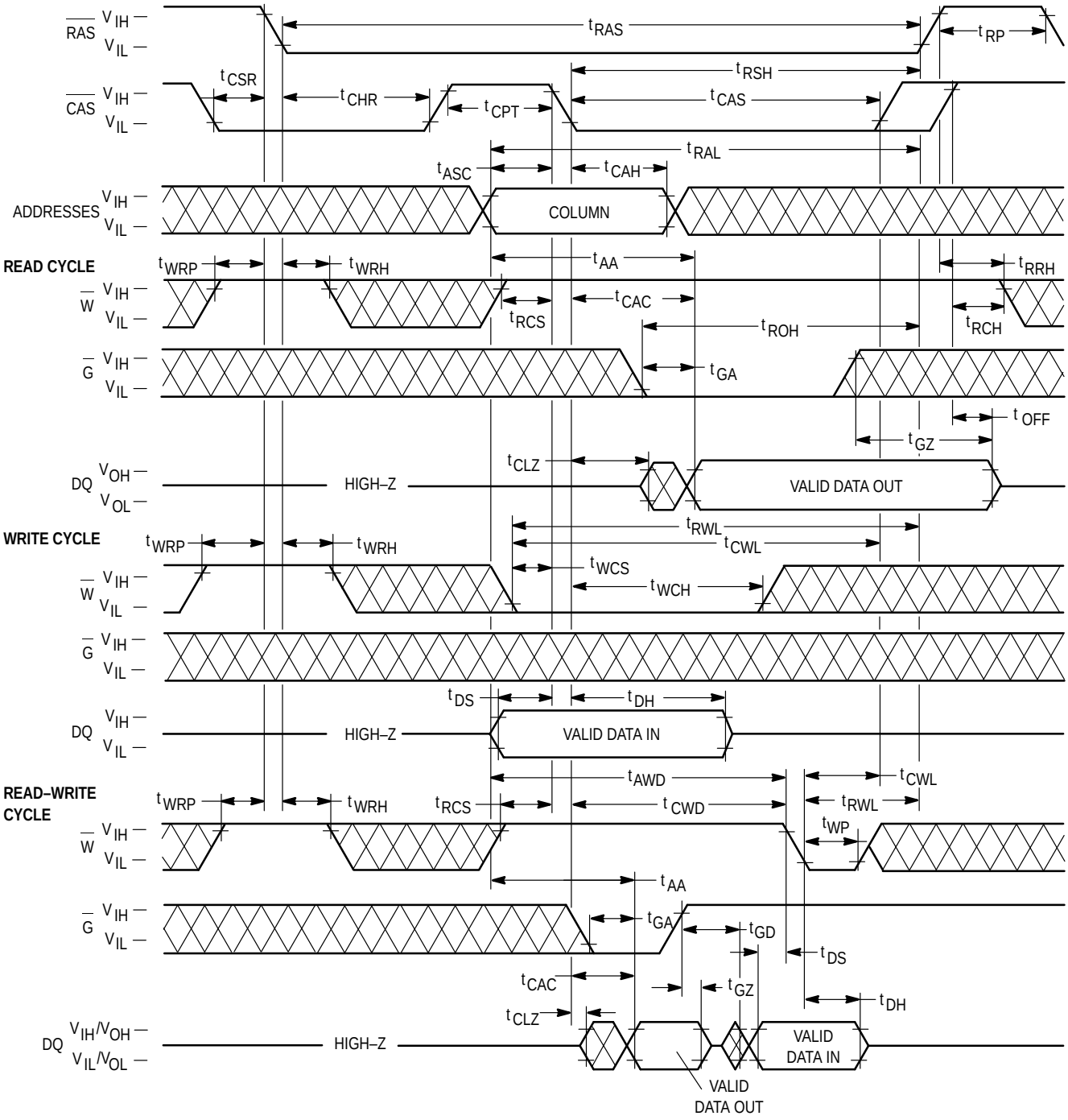
HIDDEN REFRESH CYCLE (EARLY WRITE)



PRESENCE DETECT ENABLE CYCLE



$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate 10–bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the device. RAS active transition is followed by CAS active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the module: **RAS only refresh cycle, CAS before RAS refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a normal random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. CAS controls read access time: CAS must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from RAS active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the CAS clock active transition (t_{CAC}).

The RAS and CAS clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. W must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after RAS or CAS inactive transition, respectively, to maintain the data at that bit location. Once RAS transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the CAS clock is active. When the CAS clock transitions to inactive, the output will switch to High–Z (three–state) t_{OFF} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with either an early write or a page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active (V_{IL}). Early write mode is distinguished by the active transition of W, with respect to CAS. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by W active transition at minimum time t_{WCS} before CAS active transition. Data in (DQ) is referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC}. Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL}. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS–Only Refresh

RAS–only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **CAS before RAS refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write 0s into all memory cells (normal write mode).
2. Select a column address, and read 0 out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write 1 into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read 1s (normal read mode), which were written at step three.
5. Repeat steps one through four using complement data.

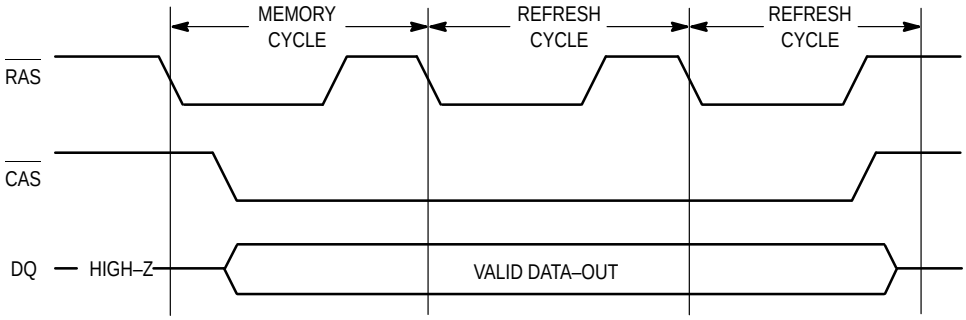
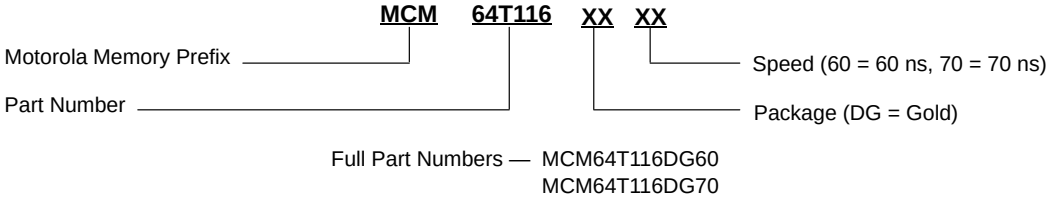


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)



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