

MCM63P532*Product Preview***32K x 32 Bit Pipelined BurstRAM™
Synchronous Fast Static RAM**

The MCM63P532 is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 32K words of 32 bits each, fabricated with Motorola's high performance silicon gate CMOS technology. This device integrates input registers, an output register, a 2-bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable (\overline{G}) and Linear Burst Order (\overline{LBO}) are clock (K) controlled through positive-edge-triggered noninverting registers.

Bursts can be initiated with either \overline{ADSP} or \overline{ADSC} input pins. Subsequent burst addresses can be generated internally by the MCM63P532 (burst sequence operates in linear or interleaved mode dependent upon state of \overline{LBO}) and controlled by the burst address advance (\overline{ADV}) input pin.

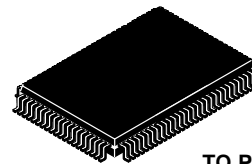
Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write (\overline{SBx}), synchronous global write (\overline{SGW}), and synchronous write enable \overline{SW} are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". \overline{SBa} controls DQa, \overline{SBb} controls DQb, etc. Individual bytes are written if the selected byte writes \overline{SBx} are asserted with \overline{SW} . All bytes are written if either \overline{SGW} is asserted or if all \overline{SBx} and \overline{SW} are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge-triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM63P532 operates from a 3.3 V power supply, all inputs and outputs are LVTTTL compatible. All address and control inputs are 5 V tolerant.

- MCM63P532-7 = 7 ns access / 13.3 ns cycle
MCM63P532-8 = 8 ns access / 15 ns cycle
MCM63P532-9 = 9 ns access / 16.6 ns cycle
- Single 3.3 V + 10%, - 5% Power Supply
- \overline{ADSP} , \overline{ADSC} , and \overline{ADV} Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self-Timed Write Cycle
- Byte Write and Global Write Control
- Sleep Mode (ZZ)
- 5 V Tolerant Address and Control Inputs
- 100 Pin TQFP Package



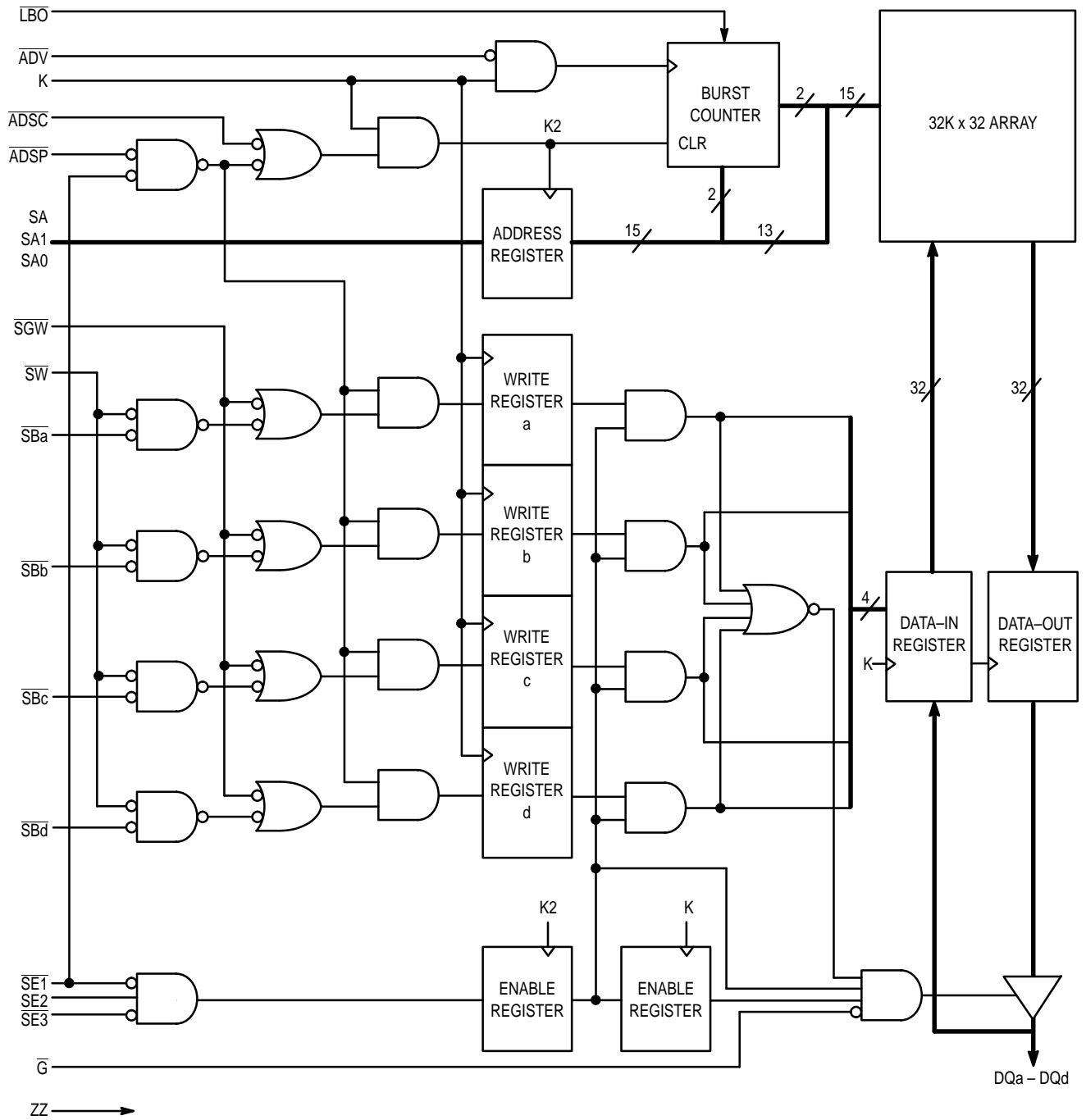
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CASE 983A-01**

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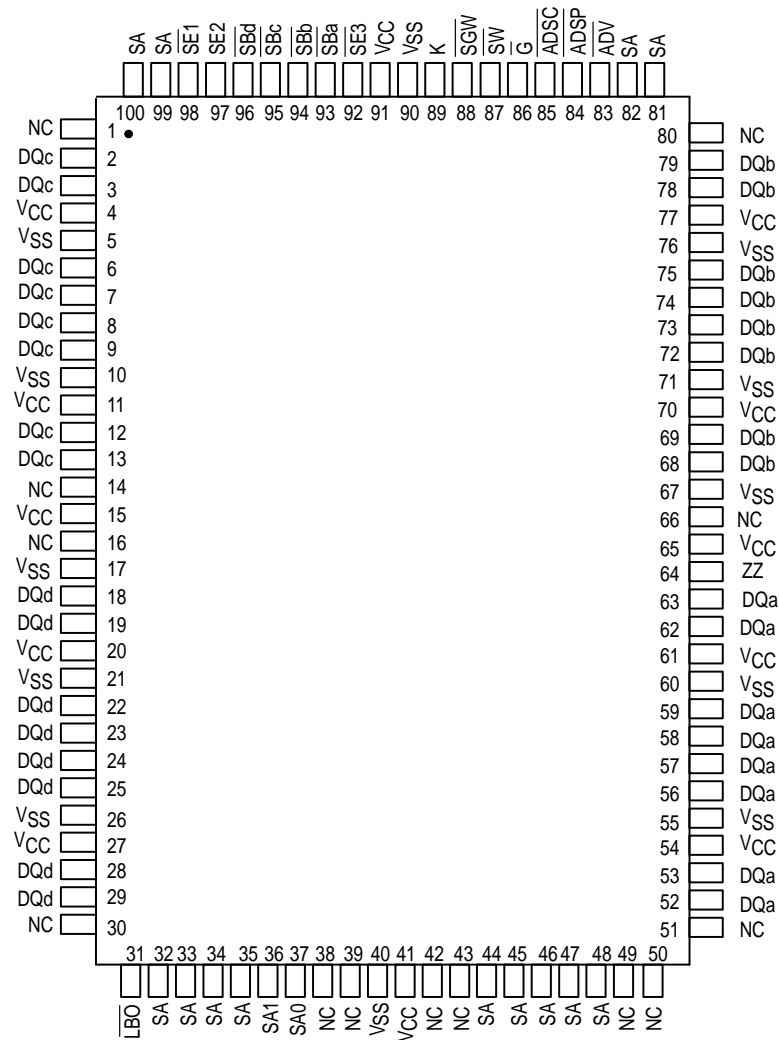
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FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except \overline{G} , \overline{LBO} , and ZZ.
93, 94, 95, 96 (a) (b) (c) (d)	\overline{SBx}	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). \overline{SGW} overrides \overline{SBx} .
87	\overline{SW}	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write \overline{SBx} pins. If only byte write signals \overline{SBx} are being used, tie this pin low.
88	\overline{SGW}	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the \overline{SBx} and \overline{SW} signals. If only byte write signals \overline{SBx} are being used, tie this pin high.
84	\overline{ADSP}	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception – chip deselect does not occur when \overline{ADSP} is asserted and SE1 is high).
85	\overline{ADSC}	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
83	\overline{ADV}	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high—blocks \overline{ADSP} or deselects chip when \overline{ADSC} is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
31	\overline{LBO}	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low—linear burst counter (68K/PowerPC) High—interleaved burst counter (486/i960/Pentium)
64	ZZ	Input	Sleep Mode: This active high asynchronous signal places the RAM into the lowest power mode. The ZZ pin disables the RAMs internal clock when placed in this mode. When ZZ is negated, the RAM remains in low power mode until it is commanded to READ or WRITE. Data integrity is maintained upon returning to normal operation.
86	\overline{G}	Input	Asynchronous Output Enable Input: Low—enables output buffers (DQx pins). High – DQx pins are high impedance.
(a) 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79 (c) 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V _{CC}	Supply	Power Supply: 3.3 V + 10%, –5%
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V _{SS}	Supply	Ground
1, 14, 16, 30, 38, 39, 42, 43, 49, 50, 51, 66, 80	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	SE1	SE2	SE3	ADSP	ADSC	ADV	G ³	DQx	Write 2, 4
Deselect	None	1	X	X	X	0	X	X	High-Z	X
Deselect	None	0	X	1	0	X	X	X	High-Z	X
Deselect	None	0	0	X	0	X	X	X	High-Z	X
Deselect	None	X	X	1	1	0	X	X	High-Z	X
Deselect	None	X	0	X	1	0	X	X	High-Z	X
Begin Read	External	0	1	0	0	X	X	X	High-Z	READ ⁵
Begin Read	External	0	1	0	1	0	X	X	High-Z	READ ⁵
Continue Read	Next	X	X	X	1	1	0	1	High-Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High-Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High-Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High-Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High-Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High-Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High-Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High-Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High-Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High-Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High-Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.

2. Write is defined as either 1) any SBx and SW low or 2) SGW is low.

3. G is an asynchronous signal and is not sampled by the clock K. G drives the bus immediately (t_{GLQX}) following G going low.

4. On write cycles that follow read cycles, G must be negated prior to the start of the write cycle to ensure proper write data setup times.

G must also remain negated at the completion of the write cycle to ensure proper write data hold times.

5. This READ assumes the RAM was previously deselected.

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	G	I/O Status
Read	L	L	Data Out (DQx)
Read	L	H	High-Z
Write	L	X	High-Z
Deselected	L	X	High-Z
Sleep	H	X	High-Z

LINEAR BURST ADDRESS TABLE (LB \overline{O} = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X ... X00	X ... X01	X ... X10	X ... X11
X ... X01	X ... X10	X ... X11	X ... X00
X ... X10	X ... X11	X ... X00	X ... X01
X ... X11	X ... X00	X ... X01	X ... X10

INTERLEAVED BURST ADDRESS TABLE (LB \overline{O} = V_{CC})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X ... X00	X ... X01	X ... X10	X ... X11
X ... X01	X ... X00	X ... X11	X ... X10
X ... X10	X ... X11	X ... X00	X ... X01
X ... X11	X ... X10	X ... X01	X ... X00

WRITE TRUTH TABLE

Cycle Type	SGW	SW	SBa	SBb	SBc	SBd
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	− 10 to 85	°C
Storage Temperature	T_{stg}	− 55 to 125	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

PACKAGE THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit	Notes
Thermal Resistance	—	—	—	1
Junction to Ambient (@ 200 lfm)	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)	$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)	$R_{\theta JC}$	9	°C/W	4

NOTES:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS
($V_{CC} = 3.3\text{ V} + 10\%, -5\%$, $T_J = 20\text{ to }110^\circ\text{C}$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.6	V
Operating Temperature	T_J	20	—	110	$^\circ\text{C}$
Input Low Voltage	V_{IL}	-0.5^*	—	0.8	V
Input High Voltage Address and Control Inputs \ddagger DQx	V_{IH}	2.0	—	5.5 $V_{CC}+0.5^{**}$	V

* $V_{IL} \geq -1\text{ V}$ for $t \leq t_{KHKH}/2$.

** $V_{IH} \leq V_{CC} + 1\text{ V}$ for $t \leq t_{KHKH}/2$.

\ddagger Control includes K, SA $\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$, $\overline{\text{ADV}}$, $\overline{\text{SE1}}$, $\overline{\text{SE2}}$, $\overline{\text{SE3}}$, $\overline{\text{SW}}$, $\overline{\text{SGW}}$, $\overline{\text{SBx}}$, $\overline{\text{G}}$, $\overline{\text{ZZ}}$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current ($0\text{ V} \leq V_{in} \leq V_{CC}$)	$I_{lkg(I)}$	—	—	± 1	μA
Output Leakage Current ($0\text{ V} \leq V_{in} \leq V_{CC}$)	$I_{lkg(O)}$	—	—	± 1	μA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time $\geq t_{KHKH}$ min)	I_{CCA}	—	—	TBD	mA
CMOS Standby Supply Current (Deselected ¹ , Clock (K) Cycle Time $\geq t_{KHKH}$, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS} + 0.2\text{ V}$ or $\geq V_{CC} - 0.2\text{ V}$)	I_{SB1}	—	—	TBD	mA
Clock Running Supply Current (Deselected ¹ , Clock (K) Cycle Time $\geq t_{KHKH}$, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS} + 0.2\text{ V}$ or $\geq V_{CC} - 0.2\text{ V}$)	I_{SB2}	—	—	TBD	mA
Sleep Mode Supply Current (Sleep Mode ² , Clock (K) Cycle Time $\geq t_{KHKH}$, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS} + 0.2\text{ V}$ or $\geq V_{CC} - 0.2\text{ V}$)	I_{ZZ}	—	—	TBD	mA
Output Low Voltage ($I_{OL} = 8\text{ mA}$)	V_{OL}	—	—	0.4	V
Output High Voltage ($I_{OH} = -4\text{ mA}$)	V_{OH}	2.4	—	—	V

NOTE:

1. Device in Deselected mode as defined by the Truth Table.

2. Device in Sleep Mode as defined by the Asynchronous Truth Table.

CAPACITANCE ($f = 1.0\text{ MHz}$, $dV = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	3	5	pF
Input/Output Capacitance	$C_{I/O}$	—	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 3.3 \text{ V} + 10\%, -5\%$, $T_J = 20 \text{ to } 110^\circ\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V
 Input Rise/Fall Time 2 ns

Output Timing Reference Level 1.5 V
 Output Load See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM63P532-7		MCM63P532-8		MCM63P532-9		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	13.3	—	15	—	16.6	—	ns	
Clock High Pulse Width	t_{KHKL}	4.5	—	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4.5	—	5	—	5	—	ns	
Clock Access Time	t_{KHQV}	—	7	—	8	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	—	6	—	6	—	7	ns	5
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	5
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	5
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5
Output Disable to Q High-Z	t_{GHQZ}	—	7	—	8	—	9	ns	6
Clock High to Q High-Z	t_{KHQZ}	2	7	2	8	2	9	ns	6
Setup Times: Address $\overline{\text{ADSP}}, \overline{\text{ADSC}}, \overline{\text{ADV}}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	4
Hold Times: Address $\overline{\text{ADSP}}, \overline{\text{ADSC}}, \overline{\text{ADV}}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	4

NOTES:

1. Write applies to all $\overline{\text{SBx}}$, $\overline{\text{SW}}$, and $\overline{\text{SGW}}$ signals when the chip is selected and $\overline{\text{ADSP}}$ high.
2. Chip Enable applies to all $\overline{\text{SE1}}$, $\overline{\text{SE2}}$ and $\overline{\text{SE3}}$ signals whenever $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is asserted.
3. All read and write cycle timings are referenced from K or $\overline{\text{G}}$.
4. $\overline{\text{G}}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{\text{G}}$ should be negated prior to start of write cycle.
5. Tested per AC Test Load.
6. Measured at $\pm 200 \text{ mV}$ from steady state. Tested per High-Z Test Load.

AC TEST LOADS

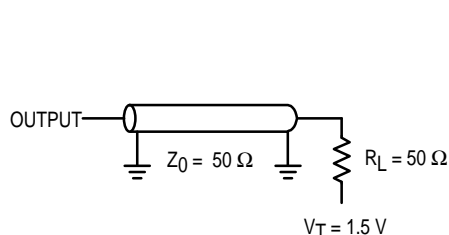


Figure 1A. AC Test Load

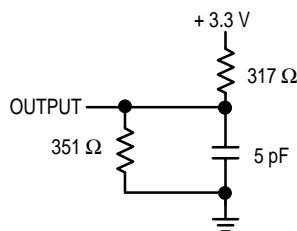
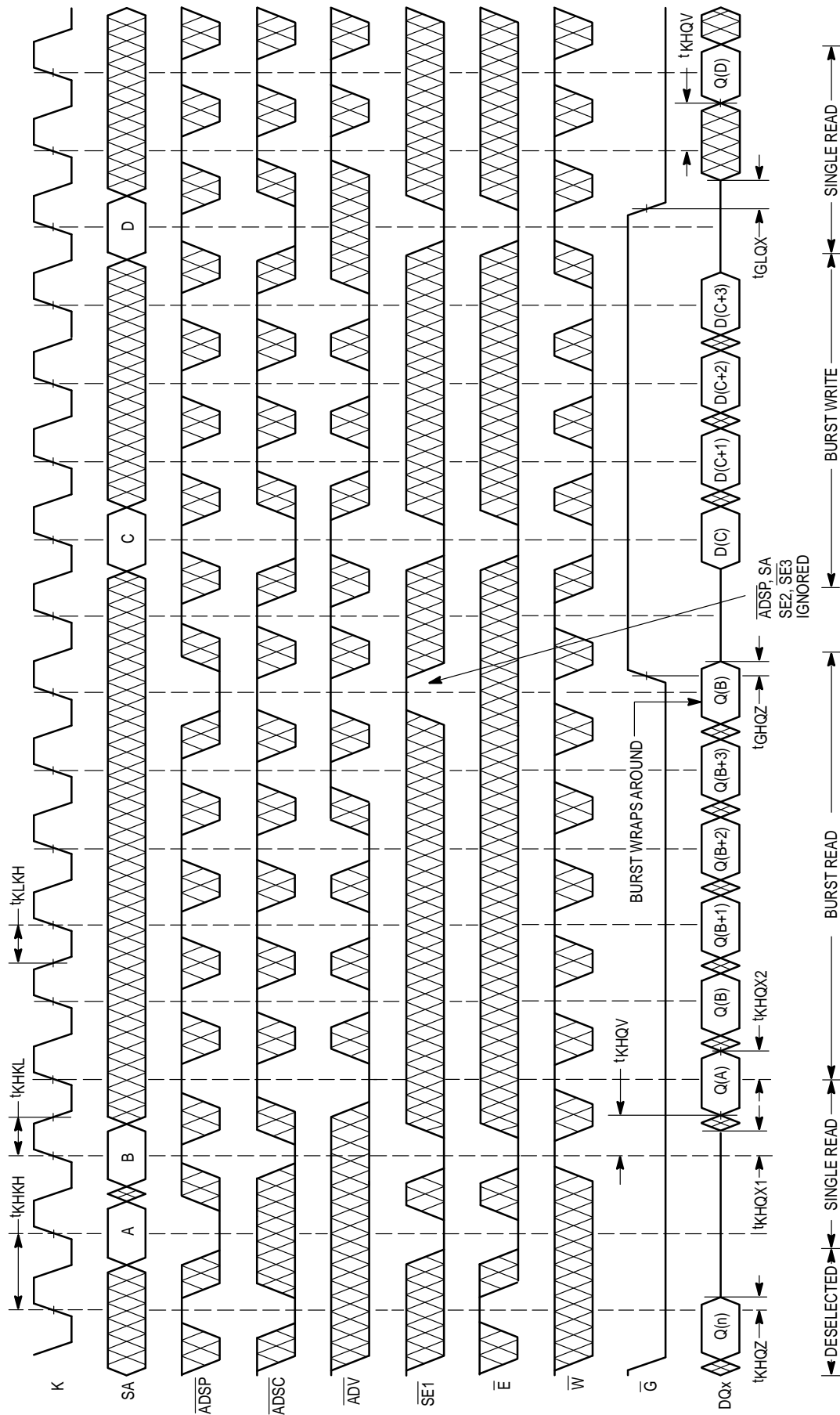


Figure 1B. High-Z Test Load

READ/WRITE CYCLES



Note: \overline{E} low = $\overline{SE2}$ high and $\overline{SE3}$ low.

\overline{W} low = \overline{SGW} low and / or \overline{SW} and \overline{SBx} low.

APPLICATION INFORMATION

The MCM63P532 BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high-end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non-pipelined (flow-through) BurstRAMs can be used since their access times meet the speed requirements for a minimum-latency, zero-wait state L2 cache interface. Latency is a measure (time) of “dead” time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi-bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx32 BurstRAM (MCM63P532) allows the designer to maintain zero-wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock-to-valid-data) of a pipelined BurstRAM is inherently faster than a non-pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – “dead” time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero-wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM63P532 as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM63P532) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer

more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support (“H” part), etc. options. A single MCM63P532 device can replace two of the 5 V 32Kx18 devices assuming parity bits are not required. The MCM63P532 can be configured to function as if it were one of the 5 V BurstRAMs. Below is a table that lists control pins on the MCM63P532 that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	ADSP	ADSC	ADV	SE1	LBO
MCM67C518	—	—	—	L	H
MCM67J518	—	—	—	—	H
MCM67N518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON-BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K-, PowerPC-, 486-, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM63P532. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non-Burst	ADSP	ADSC	ADV	SE1	LBO
Sync Non-Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

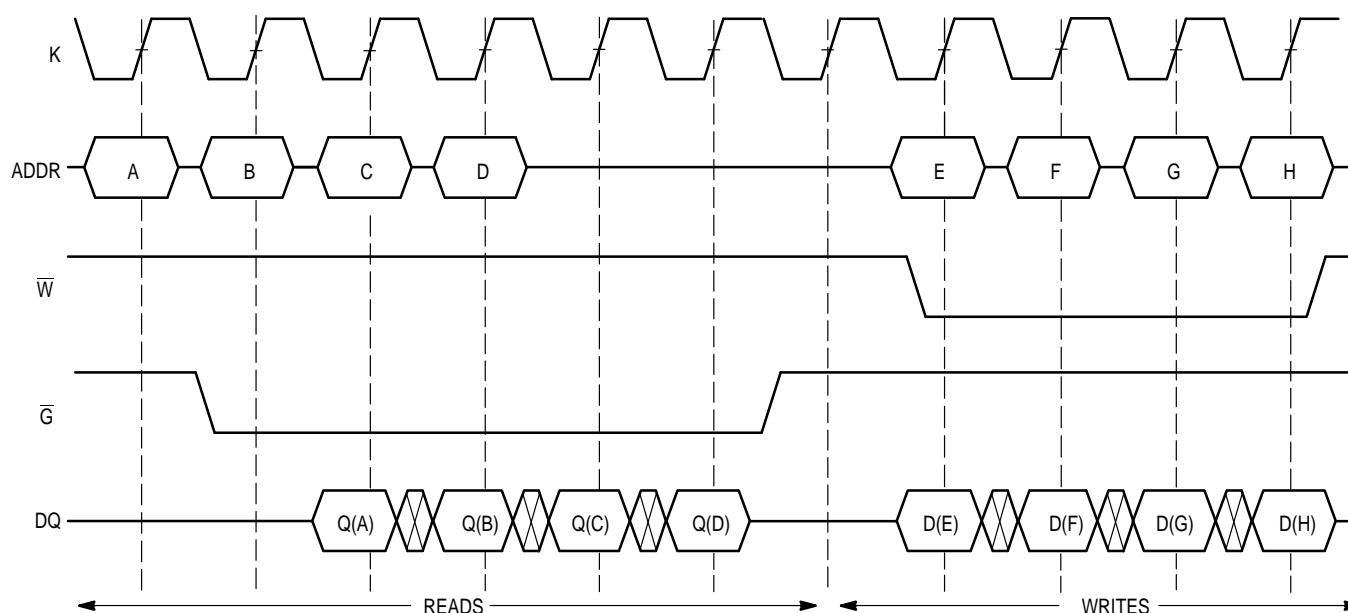
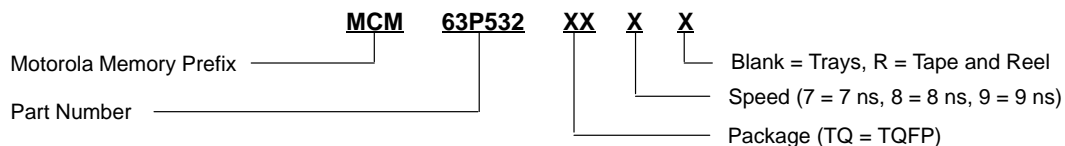



Figure 2. Configured as Non-Burst Pipelined Synchronous SRAM

ORDERING INFORMATION

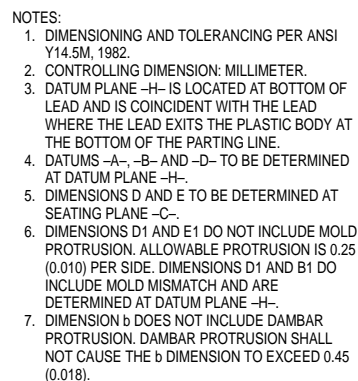
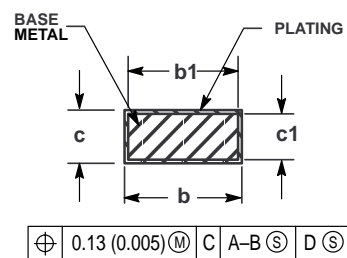
(Order by Full Part Number)



Full Part Numbers — MCM63P532TQ7 MCM63P532TQ8 MCM63P532TQ9
 MCM63P532TQ7R MCM63P532TQ8R MCM63P532TQ9R

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CASE 983A-01



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0 °	7 °	0 °	7 °
θ1	0 °	—	0 °	—
θ2	11 °	13 °	11 °	13 °
θ3	11 °	13 °	11 °	13 °

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

