

## Product Preview

# 256K x 4 Bit Static Random Access Memory

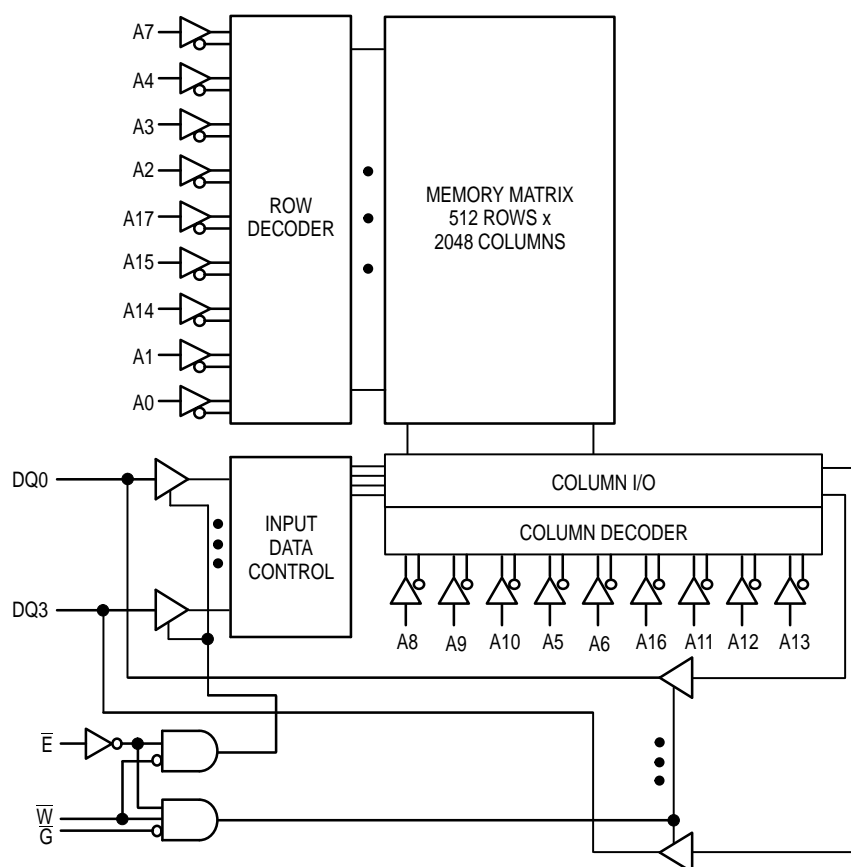
The MCM6229BA is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6229BA is equipped with both chip enable ( $\bar{E}$ ) and output enable ( $\bar{G}$ ) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs to high impedance.

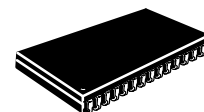
The MCM6229BA is available in 300 mil and 400 mil, 28-lead surface-mount SOJ packages.

- Single 5 V  $\pm$  10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Low Power Operation: 120/115/110/105/100 mA Maximum, Active AC

### BLOCK DIAGRAM



## MCM6229BA



J PACKAGE  
300 MIL SOJ  
CASE 810B-03

WJ PACKAGE  
400 MIL SOJ  
CASE 810-03

### PIN ASSIGNMENT

A0	1	28	VCC
A1	2	27	A17
A2	3	26	A16
A3	4	25	A15
A4	5	24	A14
A5	6	23	A13
A6	7	22	A12
A7	8	21	A11
A8	9	20	NC*
A9	10	19	DQ3
A10	11	18	DQ2
$\bar{E}$	12	17	DQ1
$\bar{G}$	13	16	DQ0
VSS	14	15	$\bar{W}$

### PIN NAMES

A0 – A17 ..... Address Inputs  
 $\bar{W}$  ..... Write Enable  
 $\bar{G}$  ..... Output Enable  
 $\bar{E}$  ..... Chip Enable  
DQ0 – DQ3 ..... Data Inputs/Outputs  
VCC ..... + 5 V Power Supply  
VSS ..... Ground  
NC\* ..... No Connection

\*If not used for no connect, then do not exceed voltages of  $-0.5$  to  $V_{CC} + 0.5$  V. This pin is used for manufacturing diagnostics.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

## TRUTH TABLE

$\bar{E}$	$\bar{G}$	$\bar{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	$I_{SB1}, I_{SB2}$
L	H	H	Output Disabled	High-Z	—	$I_{CCA}$
L	L	H	Read	D <sub>out</sub>	Read	$I_{CCA}$
L	X	L	Write	D <sub>in</sub>	Write	$I_{CCA}$

H = High, L = Low, X = Don't Care

## ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to $V_{SS}$	$V_{CC}$	- 0.5 to 7.0	V
Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$	$V_{in}, V_{out}$	- 0.5 to $V_{CC} + 0.5$	V
Output Current (per I/O)	$I_{out}$	$\pm 20$	mA
Power Dissipation	$P_D$	1.0	W
Temperature Under Bias	$T_{bias}$	- 10 to + 85	°C
Operating Temperature	$T_A$	0 to + 70	°C
Storage Temperature	$T_{stg}$	- 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = 0 \text{ to } 70^\circ\text{C}$ , Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.5	V
Input High Voltage	$V_{IH}$	2.2	$V_{CC} + 0.3^{**}$	V
Input Low Voltage	$V_{IL}$	- 0.5*	0.8	V

\*  $V_{IL}(\text{min}) = -0.5 \text{ V dc}$ ;  $V_{IL}(\text{min}) = -2.0 \text{ V ac}$  (pulse width  $\leq 20 \text{ ns}$ ).

\*\*  $V_{IH}(\text{max}) = V_{CC} + 0.3 \text{ V dc}$ ;  $V_{IH}(\text{max}) = V_{CC} + 2 \text{ V ac}$  (pulse width  $\leq 20 \text{ ns}$ ).

### DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0 \text{ to } V_{CC}$ )	$I_{lkg(I)}$	—	$\pm 1$	$\mu\text{A}$
Output Leakage Current ( $\bar{E} = V_{IH}$ , $V_{out} = 0 \text{ to } V_{CC}$ )	$I_{lkg(O)}$	—	$\pm 1$	$\mu\text{A}$
AC Active Supply Current ( $I_{out} = 0 \text{ mA}$ , all inputs = $V_{IL}$ or $V_{IH}$ , $V_{IL} = 0$ , $V_{IH} \geq 3 \text{ V}$ , cycle time $\geq t_{AVAV} \text{ min}$ , $V_{CC} = \text{max}$ )	$I_{CCA}$	—	135 120 115 110 100	mA
AC Standby Current ( $V_{CC} = \text{max}$ , $\bar{E} = V_{IH}$ , $f = f_{\text{max}}$ )	$I_{SB1}$	—	45 40 35 30 25	mA
CMOS Standby Current ( $\bar{E} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$ , $V_{CC} = \text{max}$ , $f = 0 \text{ MHz}$ )	$I_{SB2}$	—	5	mA
Output Low Voltage ( $I_{OL} = + 8.0 \text{ mA}$ )	$V_{OL}$	—	0.4	V
Output High Voltage ( $I_{OH} = - 4.0 \text{ mA}$ )	$V_{OH}$	2.4	—	V

**CAPACITANCE** ( $f = 1.0 \text{ MHz}$ ,  $dV = 3.0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance All Inputs except Clocks & DQs $\overline{E}$ , $\overline{G}$ , and $\overline{W}$	$C_{in}$	4	6	pF
	$C_{ck}$	5	8	pF
Input/Output Capacitance DQ	$C_{I/O}$	5	9	pF

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = 0 \text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

Input Pulse Levels	0 to 3.0 V	Output Timing Measurement Reference Level	1.5 V
Input Rise/Fall Time	2 ns	Output Load	See Figure 1A
Input Timing Measurement Reference Level	1.5 V		

## READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6229BA-15		6229BA-17		6229BA-20		6229BA-25		6229BA-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	$t_{AVAV}$	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	$t_{AVQV}$	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	$t_{ELQV}$	—	15	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	$t_{GLQV}$	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	$t_{AXQX}$	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	$t_{ELQX}$	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	$t_{GLQX}$	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High-Z	$t_{EHQZ}$	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Output Enable High to Output High-Z	$t_{GHQZ}$	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7

### NOTES:

1.  $\overline{W}$  is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with  $\overline{E}$  going low.
5. At any given voltage and temperature,  $t_{EHQZ}$  max is less than  $t_{ELQX}$  min, and  $t_{GHQZ}$  max is less than  $t_{GLQX}$  min, both for a given device and from device to device.
6. Transition is measured  $\pm 500 \text{ mV}$  from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ( $\overline{E} \leq V_{IL}$ ,  $\overline{G} \leq V_{IL}$ ).

## AC TEST LOADS

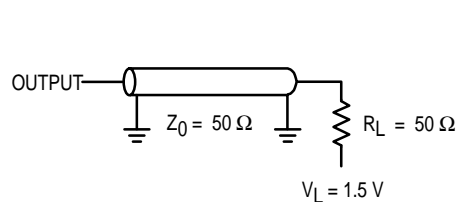


Figure 1A

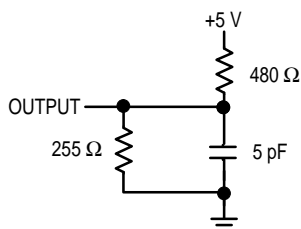
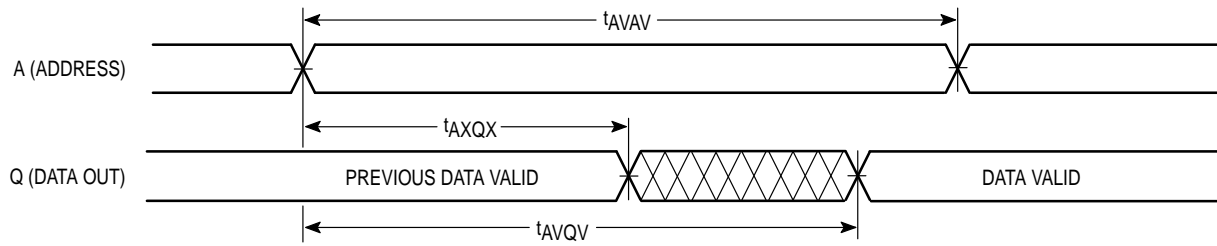


Figure 1B

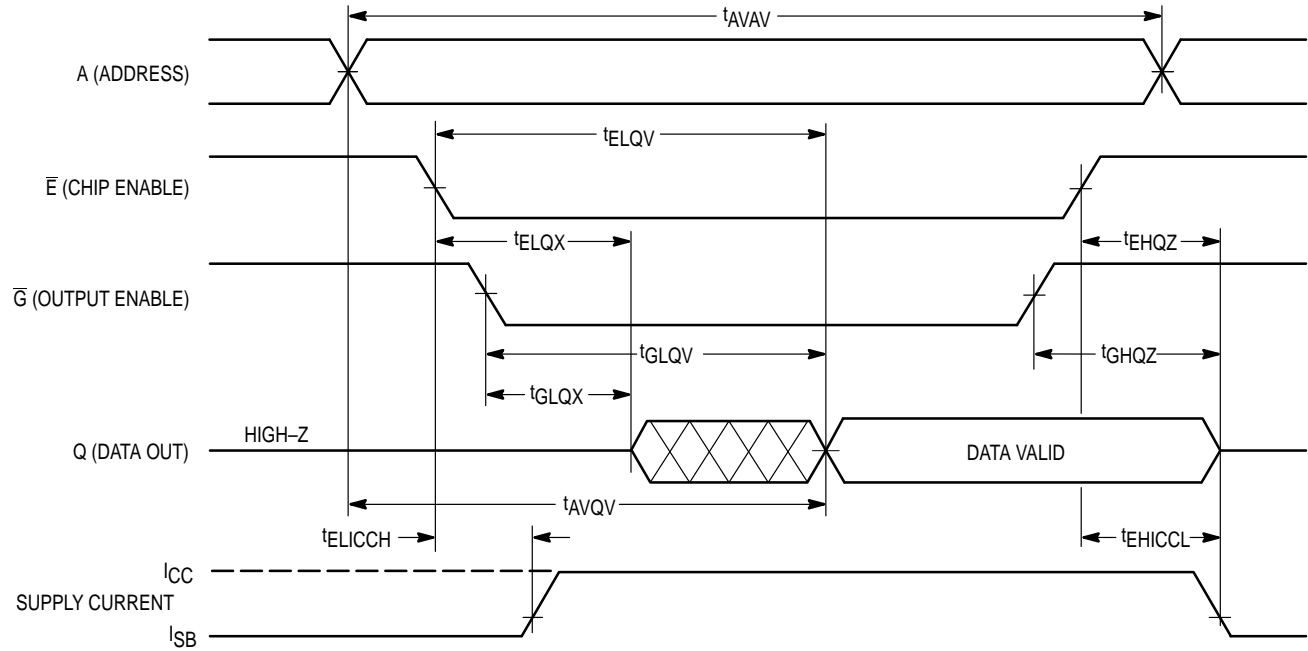
## TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

### READ CYCLE 1 (See Notes 1, 2, and 8)



### READ CYCLE 2 (See Note 8)



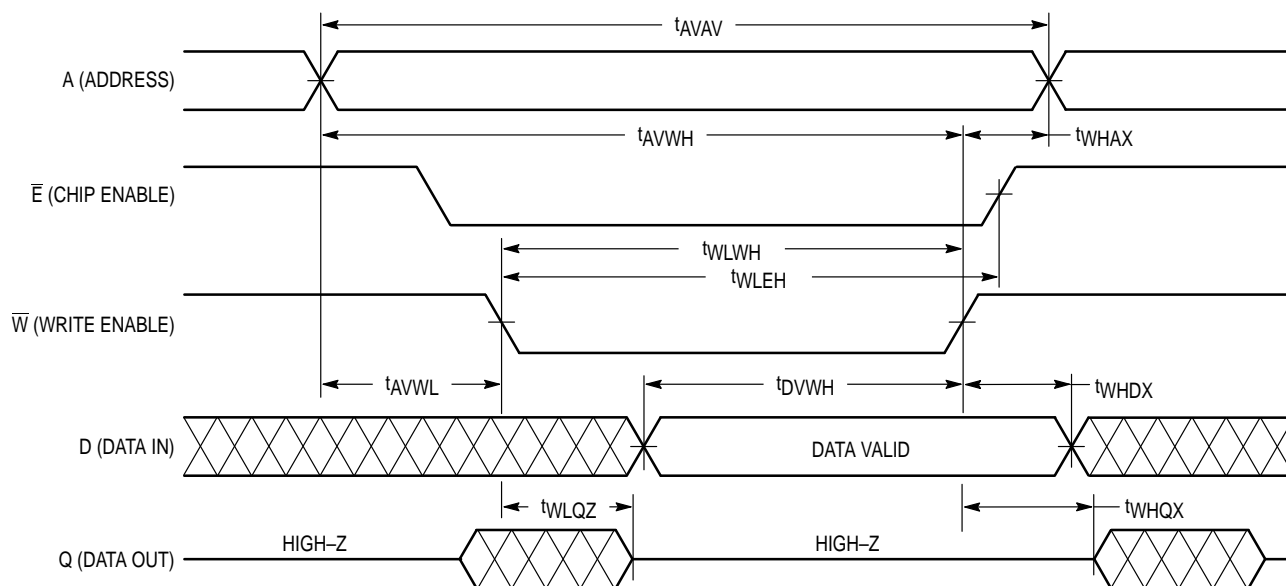
# **WRITE CYCLE 1** ( $\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229BA-15		6229BA-17		6229BA-20		6229BA-25		6229BA-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	$t_{AVWL}$	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	$t_{WLWH}$ , $t_{WLEH}$	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	$t_{DVWH}$	7	—	8	—	9	—	10	—	11	—	ns	
Data Hold Time	$t_{WHDX}$	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	$t_{WLQZ}$	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Write High to Output Active	$t_{WHQX}$	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Write Recovery Time	$t_{WHAX}$	0	—	0	—	0	—	0	—	0	—	ns	

## NOTES:

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If  $\overline{G}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature,  $t_{WLQZ}$  max is less than  $t_{WHQX}$  min both for a given device and from device to device.

## **WRITE CYCLE 1** ( $\overline{W}$ Controlled See Notes 1, 2, and 3)



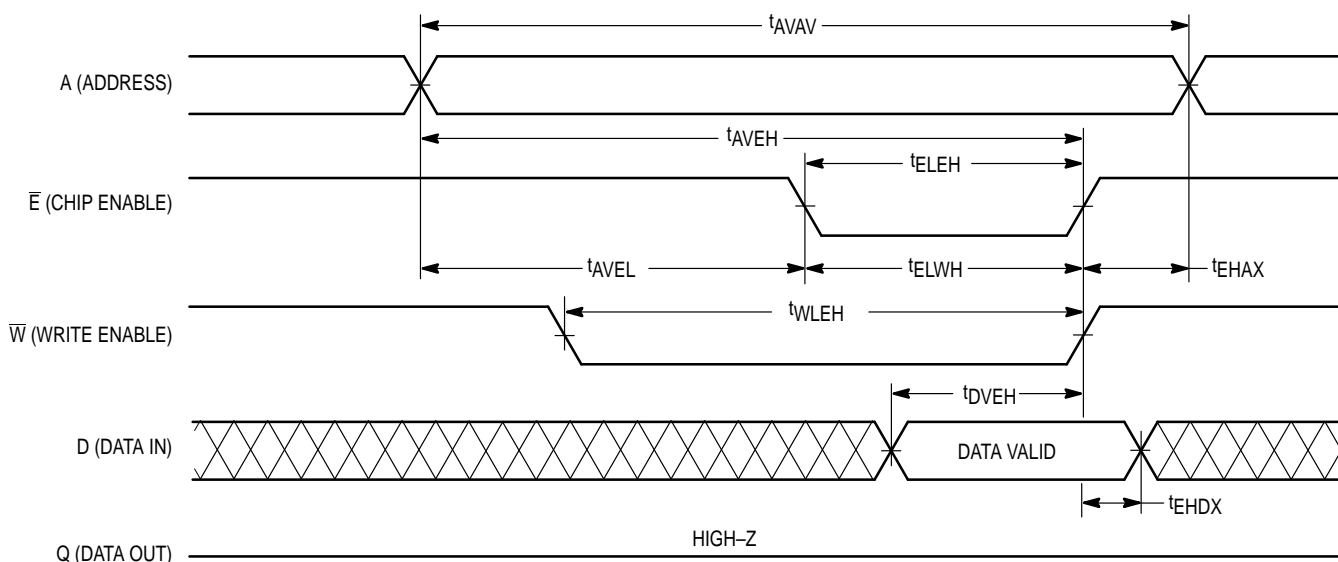
# **WRITE CYCLE 2** ( $\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229BA-15		6229BA-17		6229BA-20		6229BA-25		6229BA-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	$t_{AVEL}$	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVEH}$	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	$t_{ELEH}$ , $t_{ELWH}$	12	—	14	—	15	—	17	—	20	—	ns	5, 6
Write Pulse Width	$t_{WLEH}$	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	$t_{DVEH}$	8	—	9	—	9	—	10	—	11	—	ns	
Data Hold Time	$t_{EHDX}$	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	0	—	0	—	0	—	0	—	ns	

## **NOTES:**

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If  $\overline{G}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If  $\overline{E}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
6. If  $\overline{E}$  goes high coincident with or before  $\overline{W}$  goes high, the output will remain in a high-impedance state.

## **WRITE CYCLE 2** ( $\overline{E}$ Controlled See Notes 1, 2, and 3)

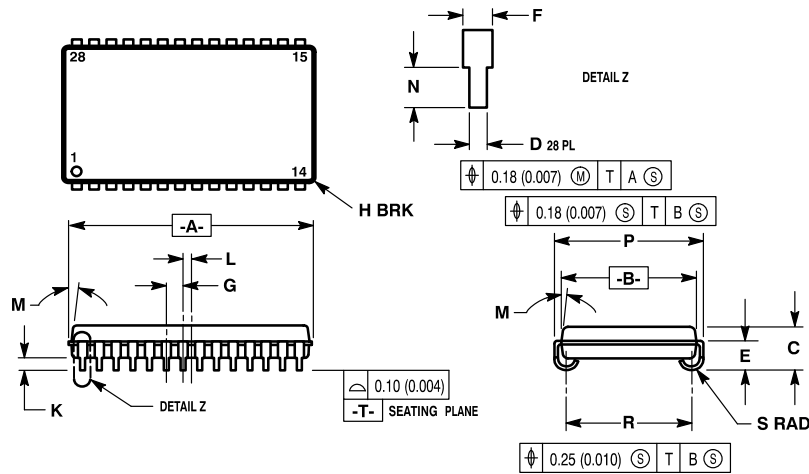


## **ORDERING INFORMATION** (Order by Full Part Number)

<b>MCM</b>	<b>6229BA</b>	<b>XX</b>	<b>XX</b>	<b>X</b>	
Motorola Memory Prefix					Shipping Method (R = Tape and Reel, Blank = Rails)
Part Number					Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
					Package (J = 300 mil SOJ, WJ = 400 mil SOJ)
Full Part Numbers —					
MCM6229BAJ15	MCM6229BAJ15R	MCM6229BAWJ15	MCM6229BAWJ15R		
MCM6229BAJ17	MCM6229BAJ17R	MCM6229BAWJ17	MCM6229BAWJ17R		
MCM6229BAJ20	MCM6229BAJ20R	MCM6229BAWJ20	MCM6229BAWJ20R		
MCM6229BAJ25	MCM6229BAJ25R	MCM6229BAWJ25	MCM6229BAWJ25R		
MCM6229BAJ35	MCM6229BAJ35R	MCM6229BAWJ35	MCM6229BAWJ35R		

## PACKAGE DIMENSIONS

### 28 LEAD 400 MIL SOJ CASE 810-03

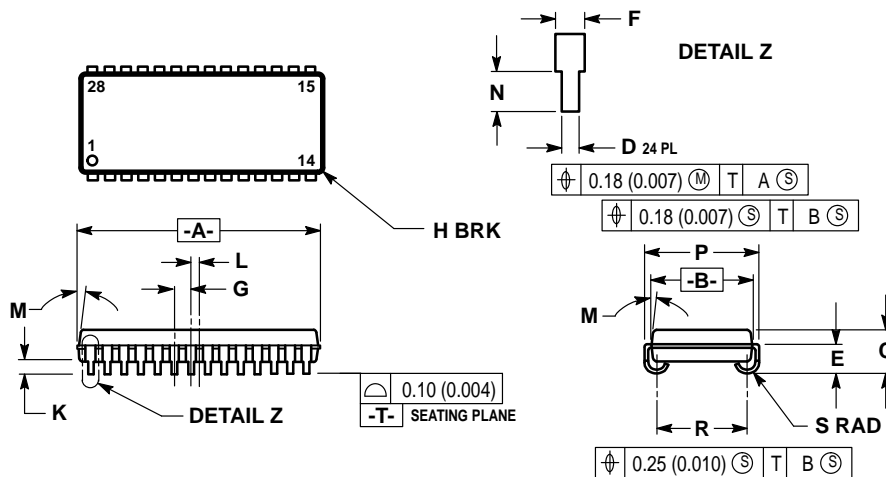


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	10.04	10.28	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.76	1.14	0.030	0.045
P	11.05	11.30	0.435	0.445
R	9.15	9.65	0.360	0.380
S	0.77	1.01	0.030	0.040


### 28 LEAD 300 MIL SOJ CASE 810B-03



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T.
5. 810B-01 AND -02 OBSOLETE, NEW STANDARD 810B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	10°	0°	10°
N	0.76	1.14	0.030	0.045
P	8.38	8.64	0.330	0.340
R	6.60	6.86	0.260	0.270
S	0.77	1.01	0.030	0.040

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**Literature Distribution Centers:**

USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.



**MOTOROLA**

◇ CODELINE TO BE PLACED HERE

**MCM6229BA/D**

