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MOTOROLA

MC44826

Advance Information

PLL Tuning Circuit with I2C Bus

The MC44826 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz. The circuit has a band decoder that provides the band switching signal for the mixer/oscillator circuit. The decoder is controlled by the buffer bits or independently by extra bits T_6 and T_7.

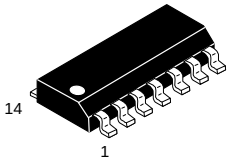
The MC44826 has a programmable 512/1024 reference divider and is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I2C Bus)
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider
- Reference Divider: Programmable for Division Ratios 512 and 1024
- Tri–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Programmable Chip Addresses
- Integrated Band Decoder for the Mixer/Oscillator Circuit
- Band Buffers with Low "On" Voltage (0.4 V Maximum at 15 mA)
- Fully ESD Protected to MIL–STD–883C, Method 3015.7 (2000 V, 1.5 kΩ, 150 pF)

MOSAIC is a trademark of Motorola, Inc.

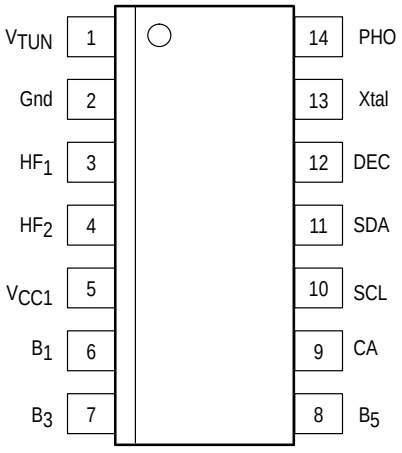
TV AND VCR
I2C PLL TUNING CIRCUIT
WITH 1.3 GHz PRESCALER
AND MIX/OSC DECODER

SEMICONDUCTOR
TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



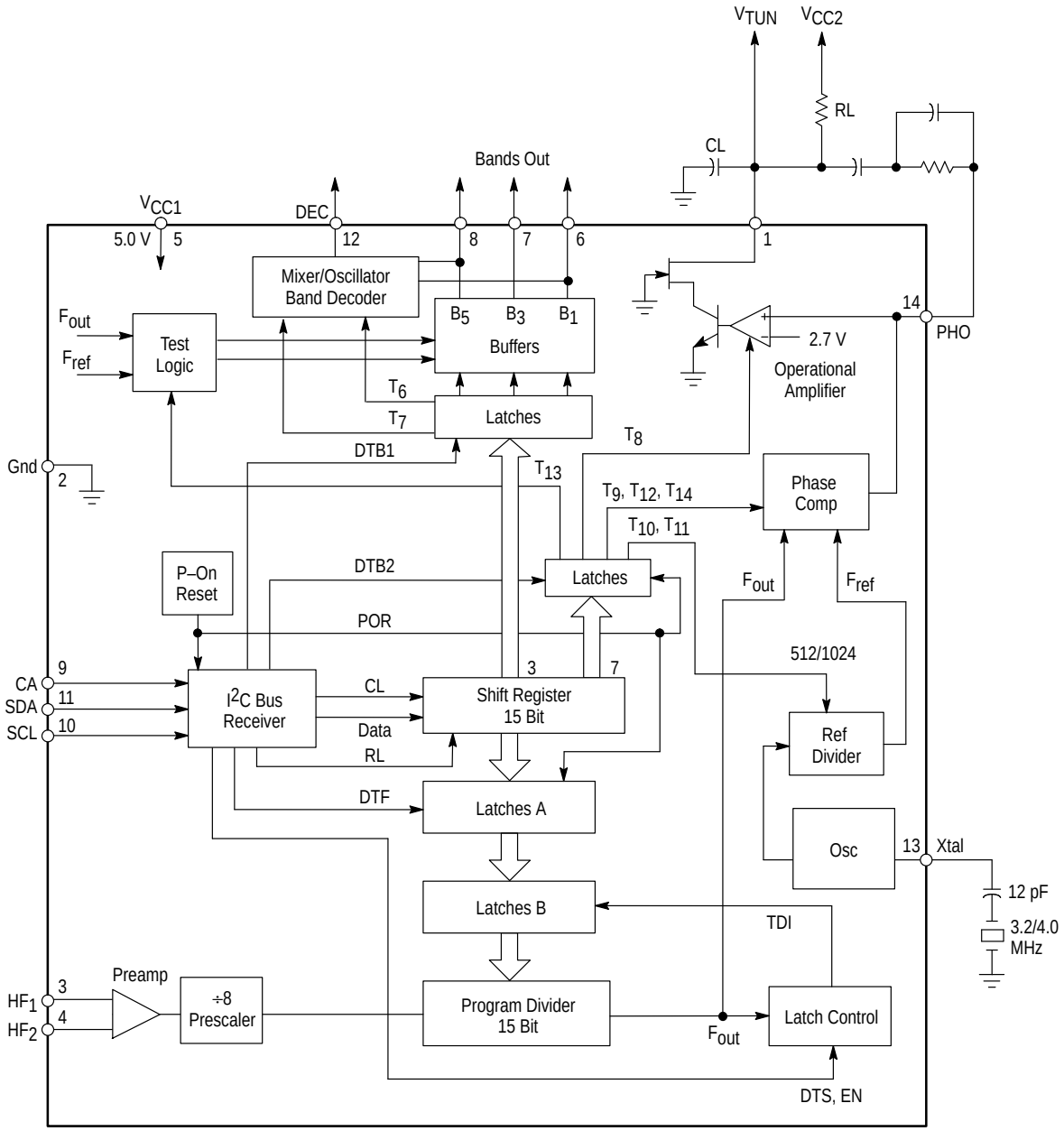
(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44826D	T_A = –20° to +80°C	SO–14

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Representative Block Diagram



This device contains 3,204 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	5	6.0	V
Band Buffer “Off” Voltage	6, 7, 8	15	V
Band Buffer “On” Current	6, 7, 8	20	mA
Operational Amplifier Power Supply (V_{CC2})	1	40	V
RF Input Level 10 MHz to 1.3 GHz	3, 4	1.5	Vrms
Storage Temperature	–	–65 to +150	°C
Operating Temperature Range	–	–20 to +80	°C
Bus Input Voltage (Positive)	10, 11	7	V
Bus Input Voltage (Negative)	10, 11	–0.5	V

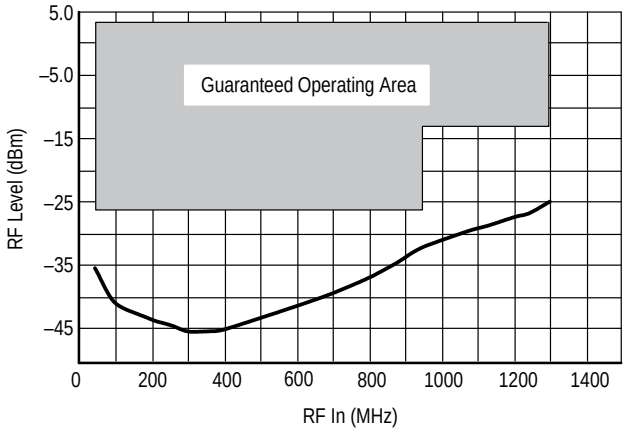
ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 33 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	5	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V)	5	25	35	50	mA
Band Buffer Leakage Current when “Off” at 12 V	6, 7, 8	–	0.01	1.0	μA
Band Buffer Saturation Voltage when “On” at 15 mA	6, 7, 8	–	0.2	0.4	V
Data/Clock Current at 0 V (Acknowledge “Off”)	10, 11	–10	–	0	μA
Data/Clock Current at 5.0 V (Acknowledge “Off”)	10, 11	0	–	1.0	μA
Data/Clock Input Voltage Low	10, 11	–	–	1.5	V
Data/Clock Input Voltage High	10, 11	3.0	–	–	V
Data Saturation Voltage at 3.0 mA (Acknowledge “On”)	11	–	0.25	0.4	V
Decoder “High” Level Sourcing 100 μA	12	3.4	–	V_{CC1}	V
Decoder “Medium” Level Sourcing 15 μA	12	1.8	–	2.1	V
Decoder “Low” Level Sinking 20 μA	12	0	–	0.8	V
Clock Frequency Range	10	–	–	100	kHz
Oscillator Frequency Range	13	3.15	3.2	4.05	MHz
Operational Amplifier Internal Reference Voltage	–	2.0	2.75	3.2	V
Operational Amplifier Input Current	14	–15	0	15	nA
DC Open Loop Gain (R_L = 22 kΩ)	14, 1	100	250	1000	V/V
Gain Bandwidth Product (C_L = 0.5 nF)	14, 1	0.3	–	–	MHz
V_{out} Low (R_L = 22 kΩ)	1	–	0.25	0.4	V
Phase Detector Current in High Impedance State	14	–15	0	15	nA
Charge Pump Current of Phase Comparator (T_{14} = 0)	14	30	40	50	μA
Charge Pump Current of Phase Comparator (T_{14} = 1)	14	90	125	150	μA
V_{CC2} Supply Voltage Range	1	25	33	36	V

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	V_{TUN}/V_{CC2}	Output of the tuning voltage amplifier. Needs an external pull–up resistor to drive the varicaps
2	Gnd	Ground
3, 4	HF_1/ HF_2	Symmetric HF inputs from local oscillator
5	V_{CC1}	Supply voltage. Typical 5.0 V
6, 7, 8	B_1, B_3, B_5	Band buffer outputs
9	CA	Chip address selection pin
10	SCL	Clock input of the I^2C bus
11	SDA	Data input
12	DEC	Band decoder output for the mixer/oscillator circuit
13	Xtal	Crystal input
14	PHO	Input of tuning voltage amplifier

Figure 1. Typical Prescaler Input Sensitivity

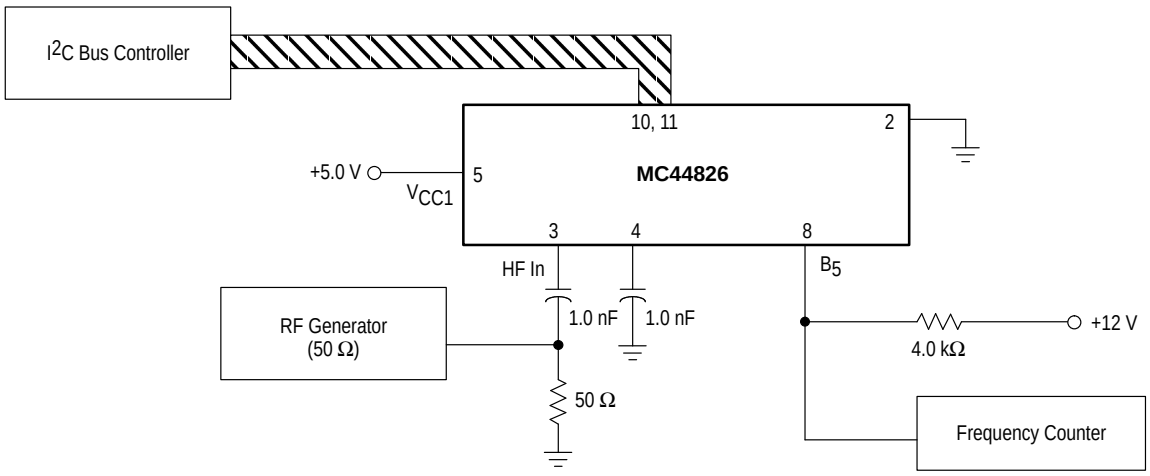


NOTE: V_{CC} = 4.5 to 5.5 V, T_A = – 20° to +80°C

HF CHARACTERISTICS (See Figure NO TAG)

Characteristic	Pin	Min	Typ	Max	Unit
DC Bias	3, 4	–	1.6	–	V
Input Voltage Range					mVrms
50–950 MHz	3, 4	10	–	315	
950–1300 MHz	3, 4	50	–	315	

Figure 2. RF Sensitivity Test Circuit



Device is in test mode, B_5 is “On”, B_1 and B_3 are “Off”.
Sensitivity is the level of the HF generator on 50 Ω load.

Figure 3. Typical HF Input Impedance

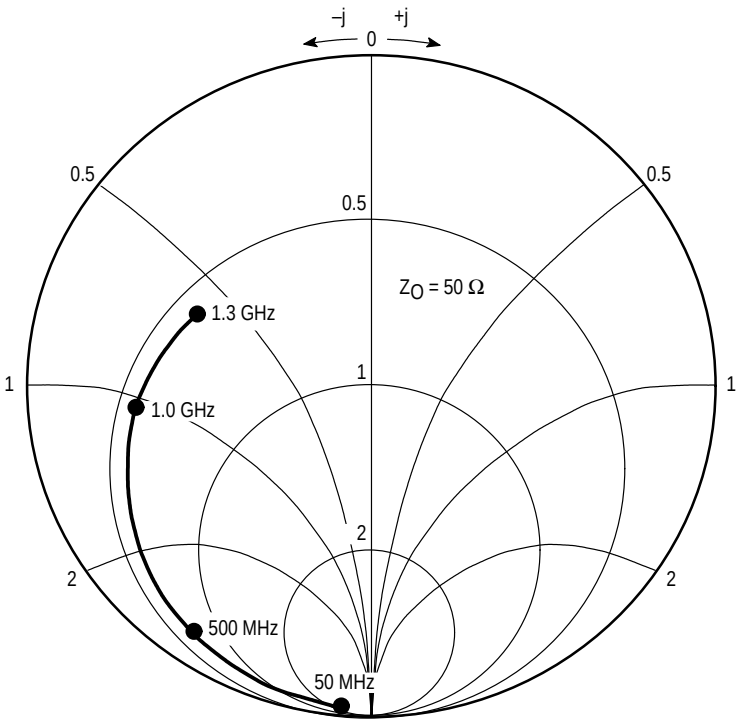
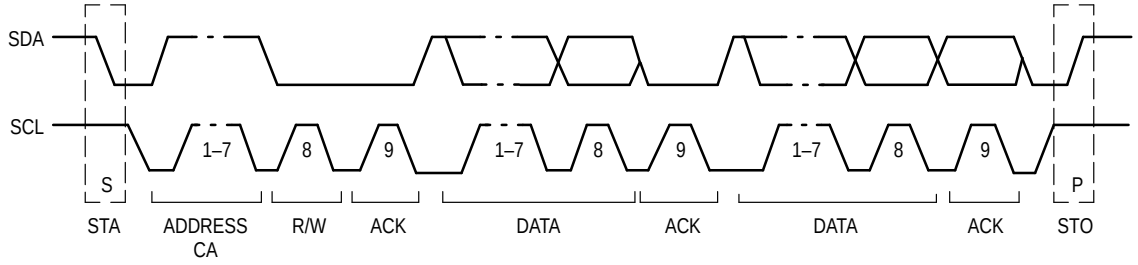


Figure 4. Complete Data Transfer Process



Data Format and Bus Receiver

The circuit receives the information for tuning and control via the I^2C bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I^2C bus receiver. The definition of the permissible bus protocol is shown below:

1_STA	CA	CO	BA	STO		
2_STA	CA	FM	FL	STO		
3_STA	CA	CO	BA	FM	FL	STO
4_STA	CA	FM	FL	CO	BA	STO

STA = Start Condition
STO = Stop Condition
CA = Chip Address Byte
CO = Data Byte for Control Information
BA = Band Information
FM = Data Byte for Frequency Information (MSB's)
FL = Data Byte for Frequency Information (LSB's)

Figure NO TAG shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allows the IC to distinguish between frequency information and control plus band information.

Frequency information is preceded by a Logic "0". If the function bit is Logic "1" the two following bytes contain control and band information. The first data byte, shifted after the chip address, may be byte CO or byte FM.

The two permissible bus protocols with five bytes are shown in Figure NO TAG.

The Data and Clock inputs (Pins 10 and 11) are high impedance when the supply voltage V_{CC1} is between 0 and 5.5 V.

Chip Address

The chip address is programmable by Pin 9 (CA – Address Select).

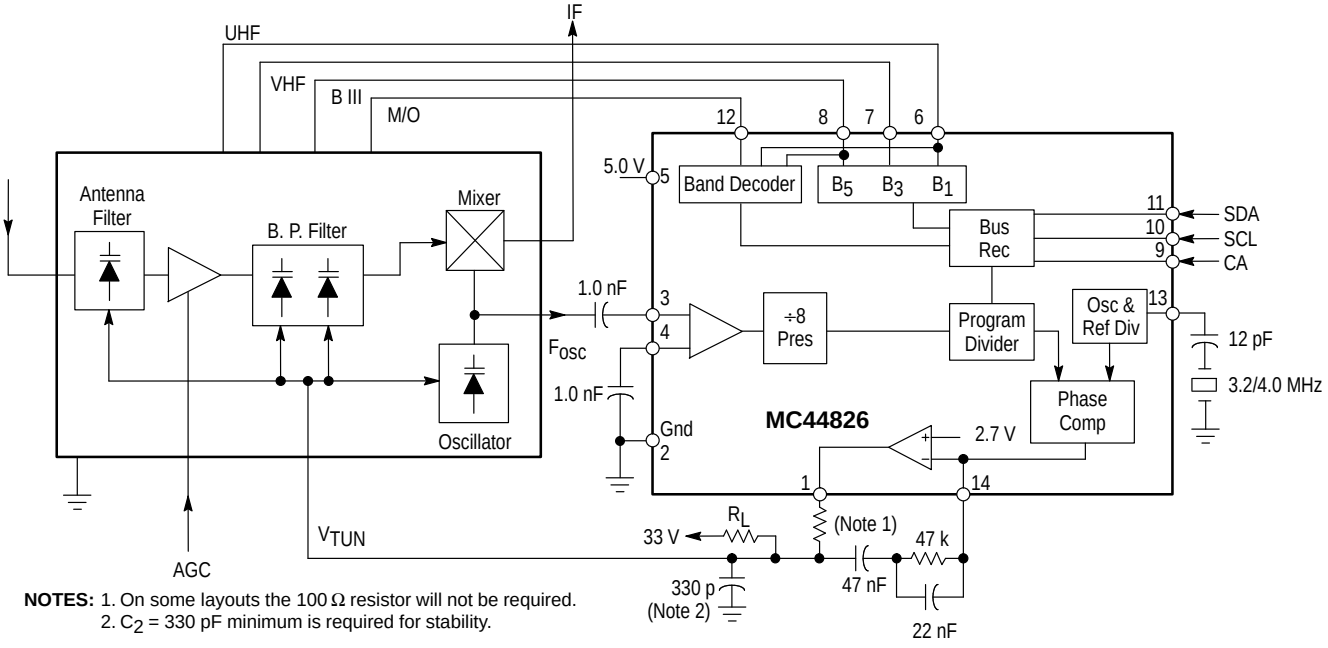
CA – Pin 9	Address (HEX.)
–0.04 V_{CC1} to 0.1 V_{CC1}	C6
Open or 0.2 V_{CC1} to 0.3 V_{CC1}	C4
0.42 V_{CC1} to 0.75 V_{CC1}	C2
0.9 V_{CC1} to 1.2 V_{CC1}	C0

Figure 5. Definition of Bytes

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
CO_Information	(1)	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	T_7	T_6	B_5	X	B_3	X	B_1	X	ACK
FM_Frequency Information	(0)	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
FM_Frequency Information	(0)	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK
CO_Information	(1)	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	T_7	T_6	B_5	X	B_3	X	B_1	X	ACK

Figure 6. Typical Tuner Application



NOTES: 1. On some layouts the 100 Ω resistor will not be required.
2. C_2 = 330 pF minimum is required for stability.

Bits B_1, B_3, B_5: Control the Band Buffers

B_1, B_3, B_5 = 0	Buffer “Off”
= 1	Buffer “On”

Bit T_8: Controls the Output of the Operational Amplifier

T_8 = 0	Normal Operation Operational Amplifier Active
= 1	Output State of Operational Amplifier Switched “Off”, Output Pulls High Through the External Pull–Up Resistor R_L

Bits T_9, T_{12}: Control the Phase Comparator

T_9	T_{12}	Function
1	0	Normal Operation
1	1	High Impedance
0	0	Upper Source “On” Only
0	1	Lower Source “On” Only

Bits T_{10}, T_{11}: Control the Reference Divider

T_{10}	T_{11}	Division Ratio
0	0	512
0	1	1024
1	0	1024
1	1	512

Bit T_{13}: Switches the Internal Signals F_{ref} and F_{BY2} to the Band Buffer Outputs (Test)

T_{13} = 0	Normal Operation
= 1	Test Mode F_{ref} Output at B_3 (Pin 7) F_{BY2} Output at B_5 (Pin 8)

Bits B_3 and B_5 have to be “On”, $B_3 = B_5 = 1$ in the test mode.
F_{ref} is the reference frequency.
F_{BY2} is the output frequency of the programmable divider, divided by two.

Bit T_{14}: Controls the Charge Pump Current of the Phase Comparator

T_{14} = 0	Pump Current 40 μA Typical
= 1	Normal Operation. Pump Current 125 μA Typical

Bits T_6, T_7: Mixer/Oscillator Band Decoder

The band decoder provides the band switching signal for the mixer/oscillator circuit. The buffer bits control the decoder output. The decoder can be controlled by the buffer bits or independently by the control bits T_6 and T_7 as per the tables below.

T_7	T_6	Decoder Output DEC
0	0	Decoder Output Controlled by Buffer Bits B_1, B_3, B_5
0	1	0 to 0.8 V
1	0	1.8 to 2.1 V
1	1	3.4 V to V_{CC1} (V_{CC1} = 4.5 to 5.5 V)

B_5	B_3	B_1	Decoder Output DEC
0	X	0	1.8 to 2.1 V
0	X	1	0 to 0.8 V
1	X	0	3.4 V to V_{CC1} (V_{CC1} = 4.5 to 5.5 V)
1	X	1	Undefined

BA_Band Information

T_7	T_6	B_5	X	B_3	X	B_1	X	ACK

The band buffers are open collector buffers and are active “low” at Bn = 1. They are designed for 15 mA with a typical “On” voltage of 200 mV. These buffers are designed to withstand relative high output voltage in the “Off” state.

B_3 and B_5 buffers may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for test purposes.

The bit B_3 and/or B_5 have to be one if the buffers are used for these additional functions.

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N_{14} + 8192 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$

Maximum Ratio 32767

Minimum Ratio 256

Where N_0 … N_{14} are the different bits for frequency information.

The counter may be used for any ratio between 256 and 32767, and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the I^2C bus.

At power–on the whole bus receiver is reset and the bit N_8 of the programmable divider is set to $N_8 = 1$. Thus the programmable divider starts with a division ratio of 256 or higher.

The first I^2C message must be sent only when the POWER ON RESET is completed. Division ratios of N < 256 are not allowed.

The Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Tuning Voltage Amplifier

The amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The tuning voltage amplifier needs an external pull–up resistor to generate the tuning voltage.

The amplifier can be switched “Off” through bit T_8. When bit T_8 is “One”, the amplifier is “Off”. The tuning voltage is then pulled high by the external pull–up resistor.

Figure NO TAG shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

The Oscillator

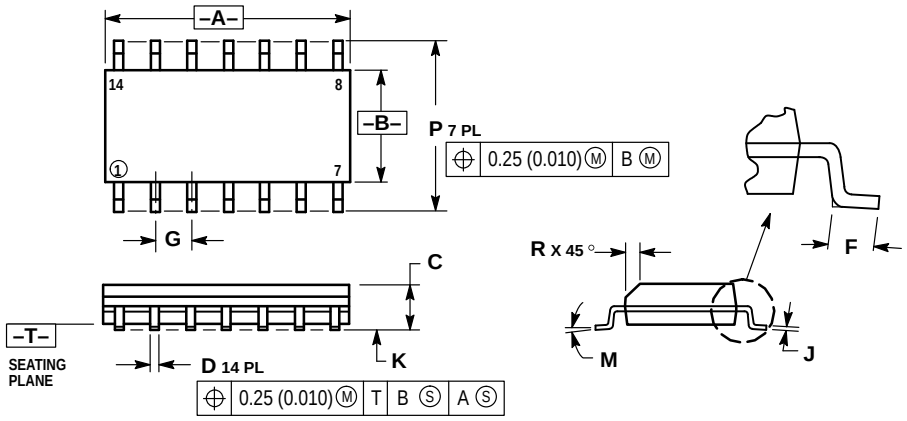
The oscillator uses a 3.2 or 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in its series resonance mode.

The voltage at Pin 13, has low amplitude and low harmonic distortion.

The negative impedance of the crystal input (Pin 13) is about 3.0 kΩ.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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