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MOTOROLA

MC44824/25

TV AND VCR PLL TUNING CIRCUITS WITH 1.3 GHz PRESCALER AND I2C BUS

PLL Tuning Circuits with I2C Bus

The MC44824/25 are tuning circuits for TV and VCR tuner applications. They contain on one chip all the functions required for PLL control of a VCO. The integrated circuits also contain a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44824/25 are manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I2C Bus). Data and Clock Inputs are 3–Wire Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider
- Reference Divider: Programmable for Division Ratios 512 and 1024
- Tri–State Phase/Frequency Comparator
- 4 Programmable Chip Addresses
- 3 Output Buffers (MC44824) respectively 5 Output Buffers (MC44825) for 10 mA/15 V
- Operational Amplifier for use with External NPN Transistor
- SO–14 Package for MC44824 and SO–16 for MC44825
- High Sensitivity Preamplifier
- Fully ESD Protected

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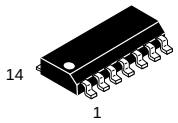
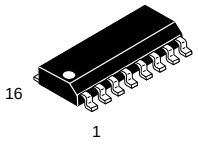


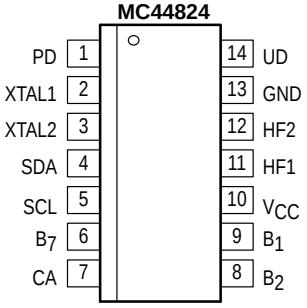
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

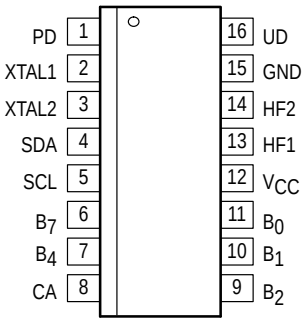
PIN CONNECTIONS

MC44824



(Top View)

MC44825

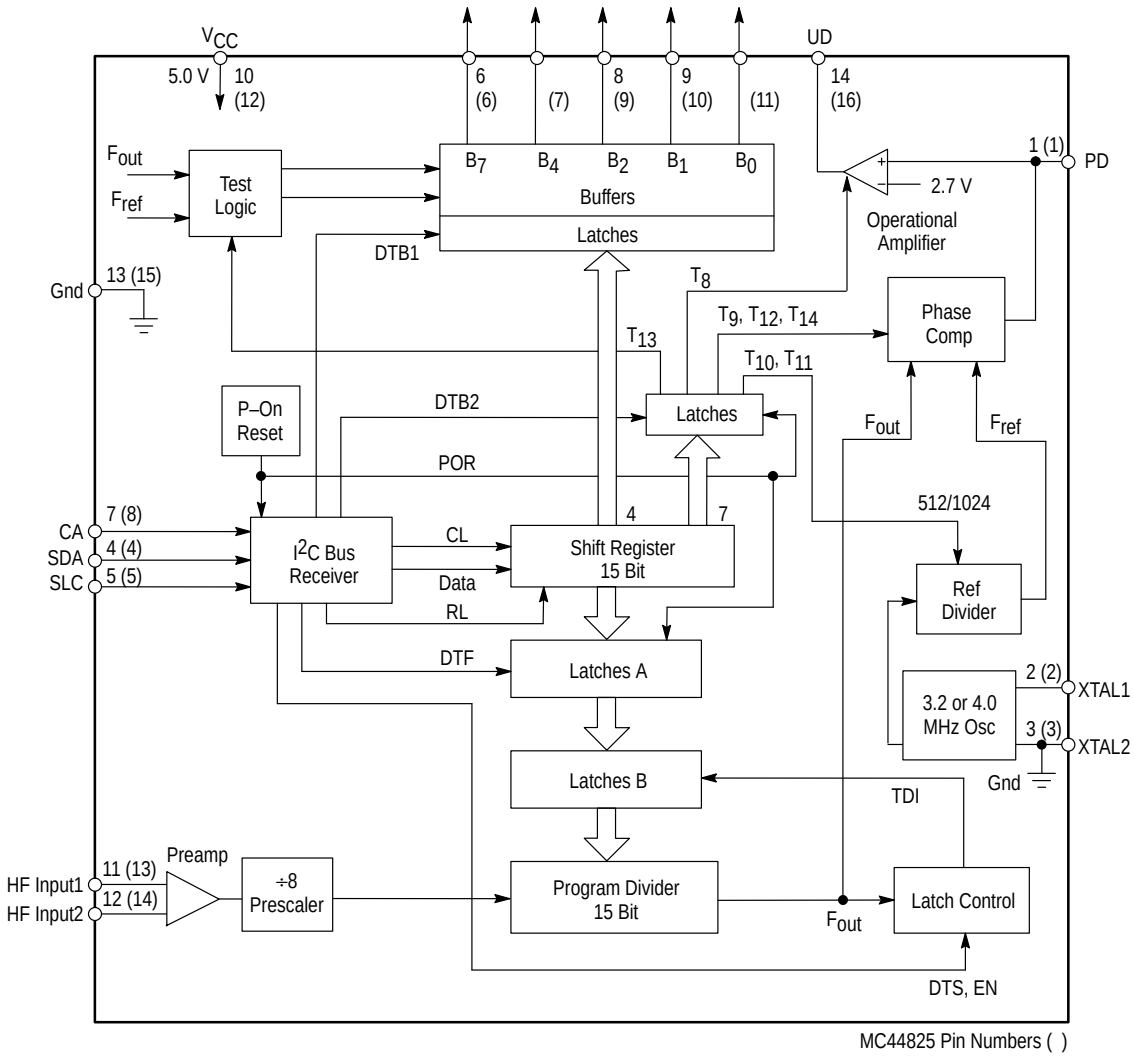


(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44824D	T_A = –20° to +80°C	SO–14
MC44825D		SO–16

Representative Block Diagram



This device contains 3,204 active transistors.

PIN FUNCTION DESCRIPTION

Pin		Symbol	Description
MC44824	MC44825		
1	1	PD	Input of tuning voltage amplifier
2	2	XTAL1	First crystal input is the active pin at the oscillators
3	3	XTAL2	Second crystal input is the internal ground
4	4	SDA	Data input
5	5	SCL	Clock input of the I^2C bus
6, 8, 9	–	B_7, B_2, B_1	Band buffer (open collector) outputs for up to 10 mA
–	6, 7, 9, 10, 11	B_7, B_4, B_2, B_1, B_0	Band buffer (open collector) outputs for up to 10 mA
7	8	CA	Chip address selection pin
10	12	V_{CC}	Supply voltage, typical 5.0 V
11, 12	13, 14	HF1/HF2	Symmetric HF inputs from local oscillator
13	15	GND	Ground
14	16	UD	Output of the tuning voltage amplifier. Needs an external NPN with pull–up resistor to drive the varicaps

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin		Value	Unit
	MC44824	MC44825		
Power Supply Voltage (V_{CC})	10	12	6.0	V
Band Buffer “Off” Voltage	6, 8, 9	6, 7, 9, 10, 11	15	V
Band Buffer “On” Current	6, 8, 9	6, 7, 9, 10, 11	15	mA
Storage Temperature	–	–	–65 to +150	°C
Operating Temperature Range	–	–	–20 to +80	°C
RF Input Level (10 MHz to 1.3 GHz)	11, 12	13, 14	1.5	Vrms

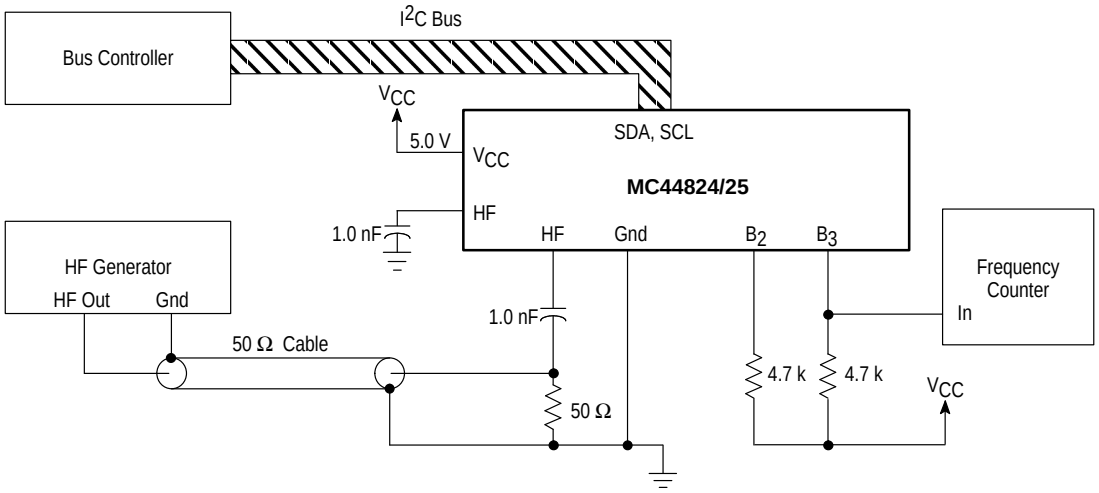
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin		Min	Typ	Max	Unit
	MC44824	MC44825				
V_{CC} Supply Voltage Range	10	12	4.5	5.0	5.5	V
V_{CC} Supply Current (V_{CC} = 5.0 V)	10	12	–	40	55	mA
Band Buffer Leakage Current when “Off” at 12 V	6, 8, 9	6, 7, 9, 10, 11	–	0.01	1.0	µA
Band Buffer Saturation Voltage when “On” at 10 mA	6, 8, 9	6, 7, 9, 10, 11	–	1.6	1.8	V
Data Saturation Voltage at 15 mA Acknowledge “On”	4	4	–	–	1.0	V
Data/Clock/Enable Current at 0 V	4, 5	4, 5	–10	–	0	µA
Data/Clock/Enable Current at 5.0 V	4, 5	4, 5	0	–	1.0	µA
Data/Clock/Enable Input Voltage Low	4, 5	4, 5	–	–	1.5	V
Data/Clock/Enable Input Voltage High	4, 5	4, 5	3.0	–	–	V
Clock Frequency Range	5	5	–	–	100	kHz
Oscillator Frequency Range	2, 3	2, 3	3.15	3.2	4.05	MHz
Operational Amplifier Input Current	1	1	–15	0	15	nA
Phase Detector Current in High Impedance State	1	1	–15	0	15	nA
Charge Pump Current of Phase Comparator, T_{14} = 0	1	1	30	40	60	µA
Charge Pump Current of Phase Comparator, T_{14} = 1	1	1	100	125	200	µA

HF CHARACTERISTICS (See Figure NO TAG)

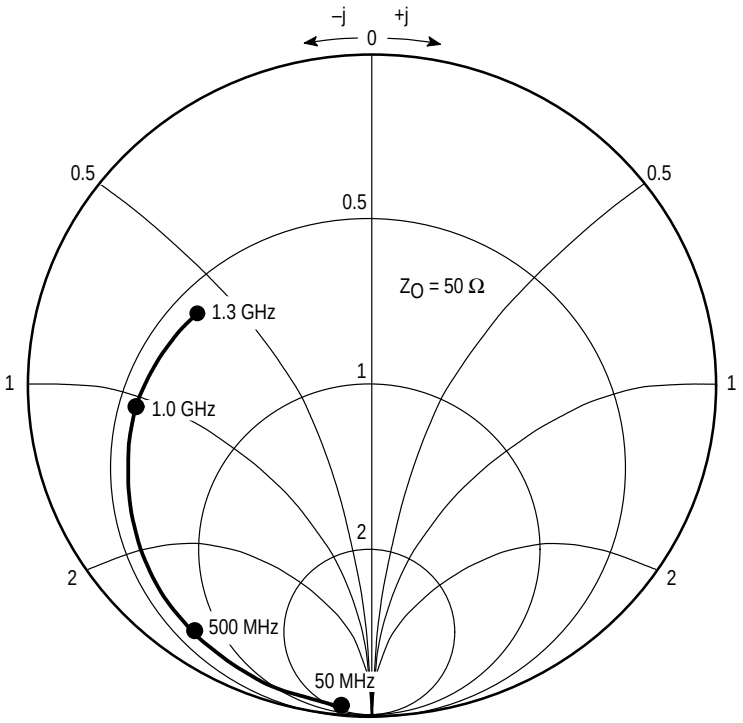
Characteristic	Pin		Min	Typ	Max	Unit
	MC44824	MC44825				
DC Bias	11, 12	13, 14	–	1.6	–	V
Input Voltage Range						mVrms
80–150 MHz	11, 12	13, 14	10	–	315	
150–600 MHz	11, 12	13, 14	5.0	–	315	
600–950 MHz	11, 12	13, 14	10	–	315	
950–1300 MHz	11, 12	13, 14	50	–	315	

Figure 1. HF Sensitivity Test Circuit



Device is in test mode. Sensitivity is level of HF generator on 50 Ω load.

Figure 2. Typical HF Input Impedance



Data Format and Bus Receiver

The circuit receives the information for tuning and control via the I2C bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I2C bus receiver. The definition of the permissible bus protocol is shown below:

1_STA	CA	CO	BA	STO		
2_STA	CA	FM	FL	STO		
3_STA	CA	CO	BA	FM	FL	STO
4_STA	CA	FM	FL	CO	BA	STO

STA = Start Condition
STO = Stop Condition
CA = Chip Address Byte
CO = Data Byte for Control Information
BA = Band Information
FM = Data Byte for Frequency Information (MSB's)
FL = Data Byte for Frequency Information (LSB's)

Figure 3. Complete Data Transfer Process

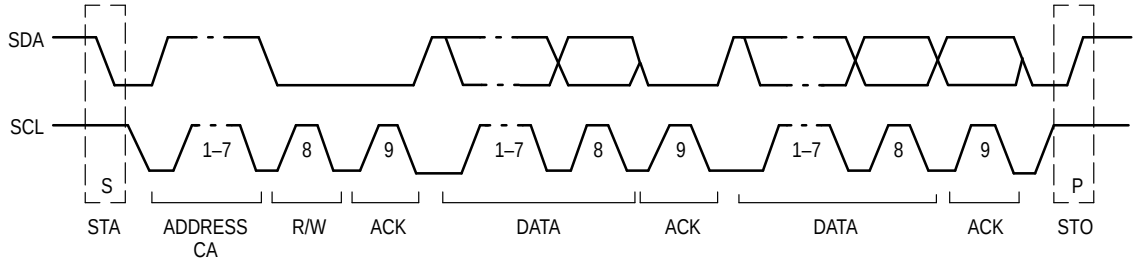


Figure 4 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received, the third data byte is ignored.

If five or more data bytes are received, the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allows the IC to distinguish between frequency information and control plus band information.

Frequency information is preceded by a Logic “0”. If the function bit is Logic “1” the two following bytes contain control and band information. The first data byte, shifted after the chip address, may be byte CO or byte FM.

The two permissible bus protocols with five bytes are shown in Figure 4.

Figure 4. Definition of Bytes

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	X	X	X	X	B_3	B_2	B_1	B_0	ACK
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	X	X	X	X	B_3	B_2	B_1	B_0	ACK

Chip Address

The chip address is programmable by Pin 7 (8), CA.

CA – Pin 7 (8)	Address (HEX.)
Gnd to 0.1 V_{CC1}	C0
Open or 0.2 V_{CC1} to 0.3 V_{CC1}	C2
0.4 V_{CC1} to 0.7 V_{CC1}	C4
0.8 V_{CC1} to 1.1 V_{CC1}	C6

Bits B_0, B_1, B_2, B_4, B_7: Control the Band Buffers

B_0, B_1, B_2, B_4, B_7 = 0	Buffer “Off”
= 1	Buffer “On”

Bit T_8: Controls the Output of the Operational Amplifier

T_8 = 0	Normal Operation Operational Amplifier Active
= 1	Output State of Operational Amplifier Switched “Off”, Output Pulls High Through an External Pull–Up Resistor

Bits T_9, T_{12}: Control the Phase Comparator

T_9	T_{12}	Function
1	0	Normal Operation
1	1	High Impedance
0	0	Upper Source “On” Only
0	1	Lower Source “On” Only

Bits T_{10}, T_{11}: Control the Reference Ratio

T_{10}	T_{11}	Division Ratio
0	0	512
0	1	1024
1	0	1024
1	1	512

Bit T_{13}: Switches the Internal Signals F_{ref} and F_{BY2} to the Band Buffer Outputs (Test)

T_{13} = 0	Normal Operation
= 1	Test Mode F_{ref} Output at B_7 F_{BY2} Output at B_2

Bits B_2 and B_7 have to be "Off", $B_2 = B_7 = 0$ in the test mode.
F_{ref} is the reference frequency.
F_{BY2} is the output frequency of the programmable divider, divided by two.

Bit T_{14}: Controls the Charge Pump Current of the Phase Comparator

T_{14} = 0	Pump Current 40 μA Typical
= 1	Pump Current 125 μA Typical

The Band Buffers

BA_Band Information
MC44824 14 Pin version

B_7	X	X	X	X	B_2	B_1	X	ACK

MC44825 16 Pin version

B_7	X	X	B_4	X	B_2	B_1	B_0	ACK

The band buffers are open collector buffers and are active "low" at Bn = 1. They are designed for 10 mA with a typical "On" resistance of 160 Ω. These buffers are designed to withstand relative high output voltage in the "Off" state.

B_2 and B_7 buffers may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for test purposes.

The bit B_2 and/or B_7 have to be zero if the buffers are used for these additional functions.

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N_{14} + 8192 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$

Maximum Ratio 32767

Minimum Ratio 17

Where N_0 … N_{14} are the different bits for frequency information.

The counter may be used for any ratio between 17 and 32767 and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the I^2C bus.

At power–on, the whole bus receiver is reset and the programmable divider is set to a counting ration of N = 256 or higher.

The first I^2C message must be sent only when the POWER ON RESET is completed.

The Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Tuning Voltage Amplifier

The amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The tuning voltage amplifier needs an external NPN with a pull–up resistor to generate the tuning voltage.

The amplifier can be switched "Off" through bit T_8. When bit T_8 is "One", the amplifier is "Off". The tuning voltage is then pulled high by the external pull–up resistor.

Figure 5 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

As a starting point for optimization, the component values in Figure 5 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

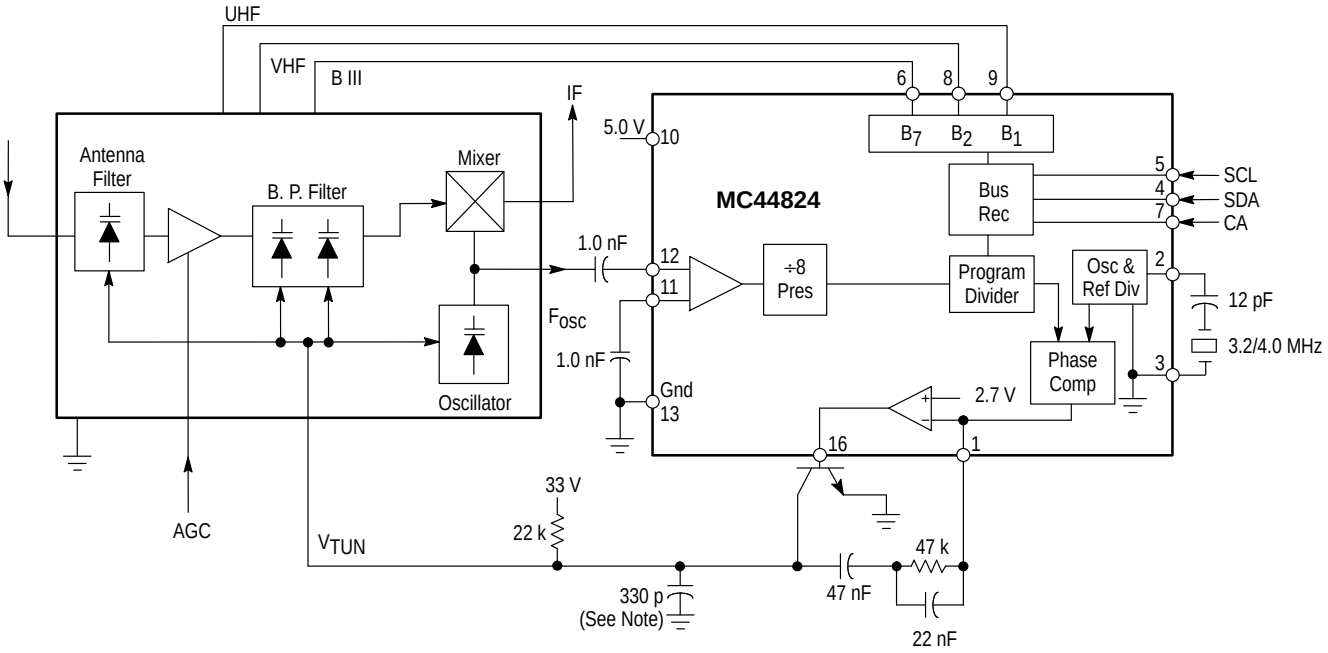
The Oscillator

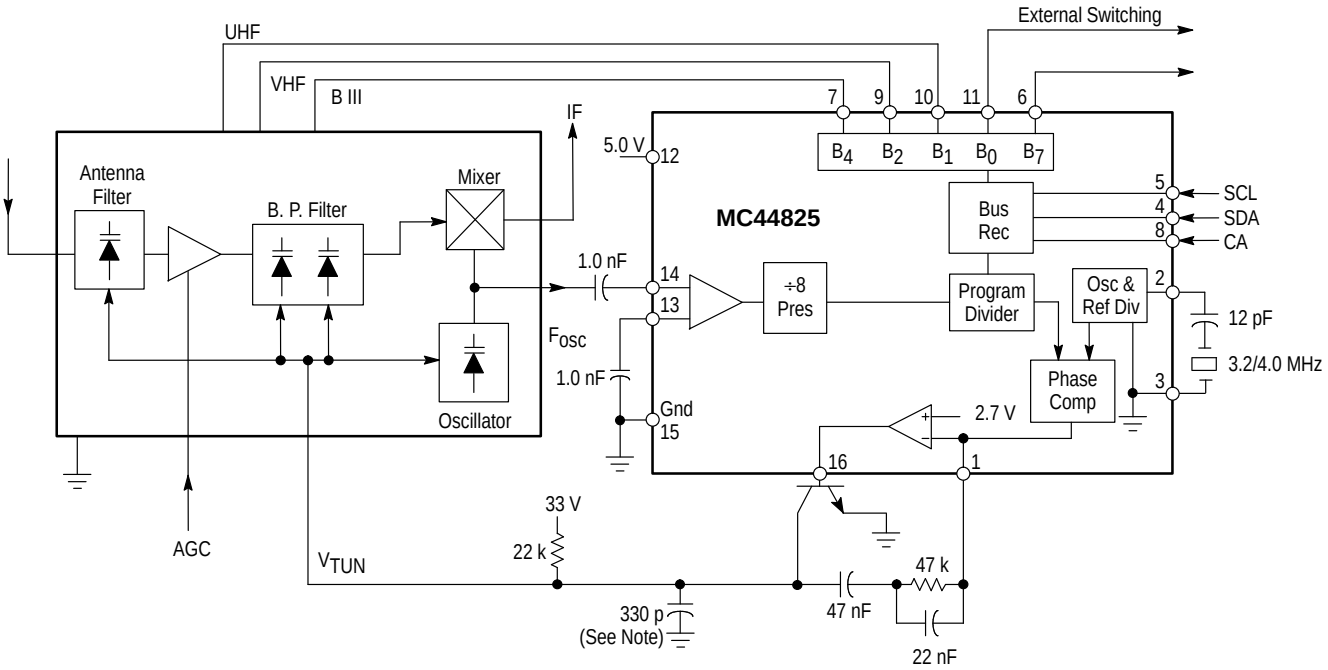
The oscillator uses a 4.0 MHz crystal tied to ground "or between Pins 2 and 3" through a series capacitor. The crystal oscillates in its series resonance mode.

The voltage at Pin 13 XTAL1, has low amplitude and low harmonic distortion.

Pin XTAL2 is the internal ground of the oscillator; it is connected internally to ground Pin 13 (15).

Figure 5. Typical Tuner Applications

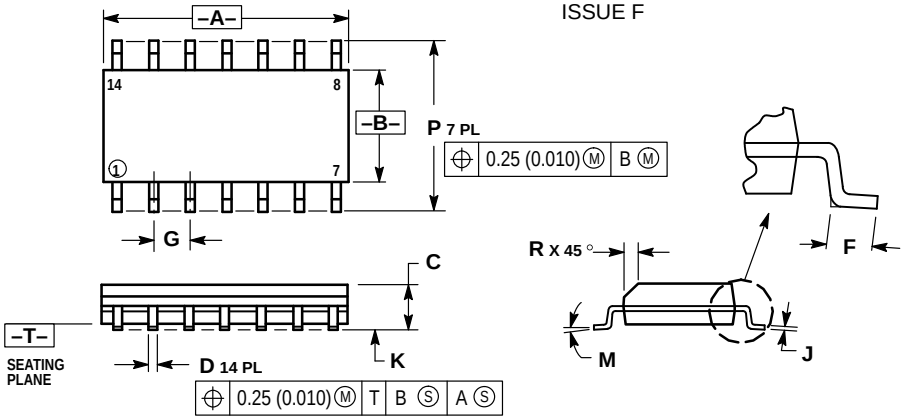




NOTE: C_2 = 330 pF minimum is required for stability.

OUTLINE DIMENSIONS

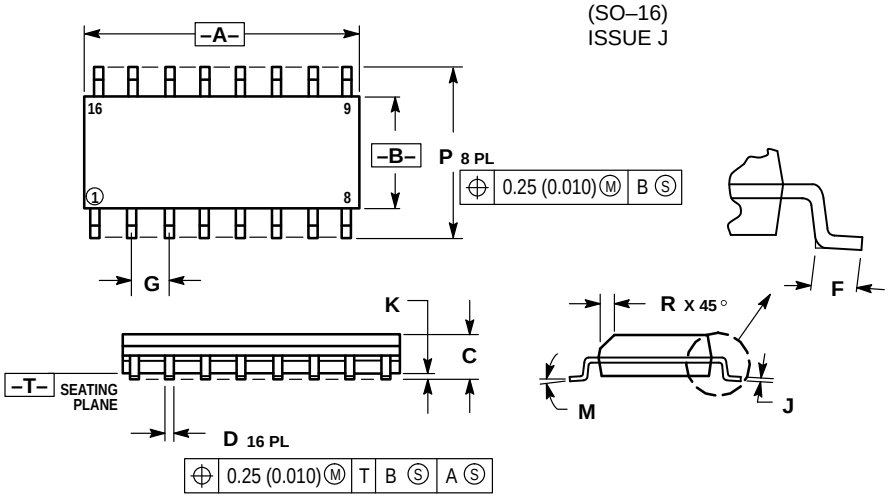
D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



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	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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