

Advance Information

1M x 4 CMOS Dynamic RAM

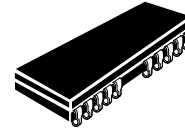
Fast Page Mode

The MCM44400C is a 0.8μ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM44400C requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil J-lead small outline package.

- Three-State Data Output
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- RAS-Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
 - MCM44400C = 16 ms
 - MCM4L4400C = 128 ms
- Fast Access Time (t_{RAC}):
 - MCM44400C-60 and MCM4L4400C-60 = 60 ns (Max)
 - MCM44400C-70 and MCM4L4400C-70 = 70 ns (Max)
 - MCM44400C-80 and MCM4L4400C-80 = 80 ns (Max)
- Low Active Power Dissipation:
 - MCM44400C-60 and MCM4L4400C-60 = 605 mW (Max)
 - MCM44400C-70 and MCM4L4400C-70 = 550 mW (Max)
 - MCM44400C-80 and MCM4L4400C-80 = 495 mW (Max)
- Low Standby Power Dissipation:
 - MCM44400C and MCM4L4400C = 11 mW (Max, TTL Levels)
 - MCM44400C = 5.5 mW (Max, CMOS Levels)
 - MCM4L4400C = 1.1 mW (Max, CMOS Levels)

MCM44400C MCM4L4400C



N PACKAGE
300 MIL SOJ
CASE
822B-01

PIN NAMES

A0 – A9	Address Inputs
DQ0 – DQ3	Data Input/Output
<u>G</u>	Output Enable
<u>W</u>	Read/Write Enable
<u>RAS</u>	Row Address Strobe
<u>CAS</u>	Column Address Strobe
VCC	Power Supply (+ 5 V)
VSS	Ground

PIN ASSIGNMENTS

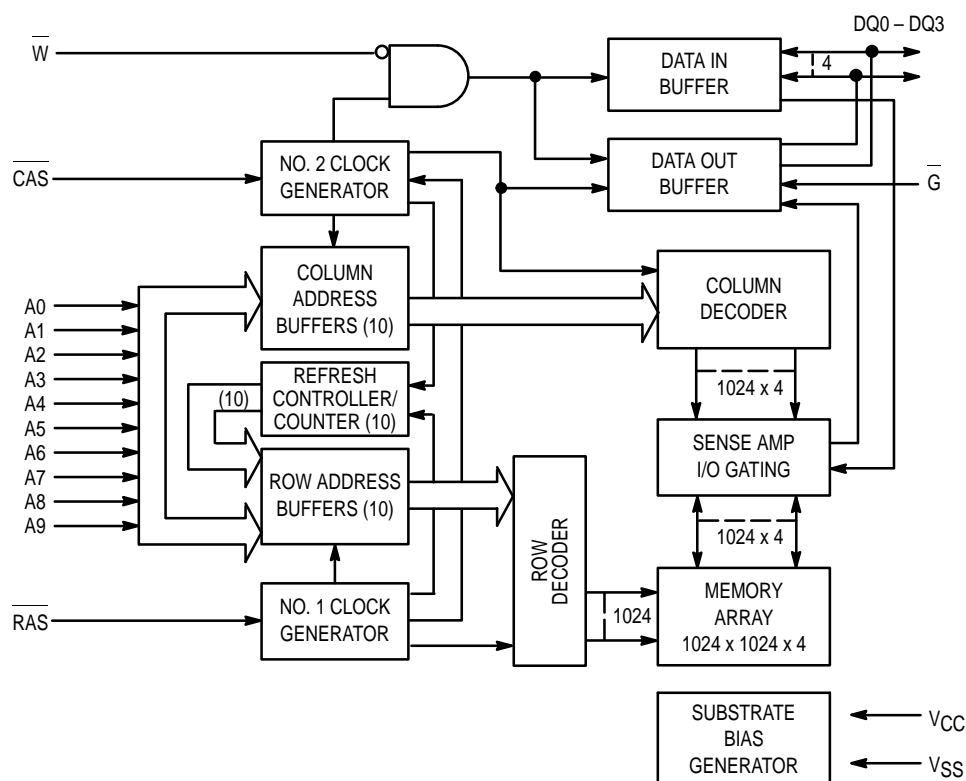
300 MIL SOJ

DQ0	1	26	VSS
DQ1	2	25	DQ3
<u>W</u>	3	24	DQ2
<u>RAS</u>	4	23	<u>CAS</u>
A9	5	22	<u>G</u>
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
VCC	13	14	A4

This document contains information on a new product. Specifications and information herein are subject to change without notice.



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	- 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	- 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_A = 0 \text{ to } 70^\circ\text{C}$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM44400C–60 and MCM4L4400C–60, $t_{RC} = 110 \text{ ns}$ MCM44400C–70 and MCM4L4400C–70, $t_{RC} = 130 \text{ ns}$ MCM44400C–80 and MCM4L4400C–80, $t_{RC} = 150 \text{ ns}$	I_{CC1}	— — —	110 100 90	mA	1, 2
V_{CC} Power Supply Current (Standby) ($RAS = CAS = V_{IH}$)	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During RAS–Only Refresh Cycles ($CAS = V_{IH}$) MCM44400C–60 and MCM4L4400C–60, $t_{RC} = 110 \text{ ns}$ MCM44400C–70 and MCM4L4400C–70, $t_{RC} = 130 \text{ ns}$ MCM44400C–80 and MCM4L4400C–80, $t_{RC} = 150 \text{ ns}$	I_{CC3}	— — —	110 100 90	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($RAS = V_{IL}$) MCM44400C–60 and MCM4L4400C–60, $t_{PC} = 40 \text{ ns}$ MCM44400C–70 and MCM4L4400C–70, $t_{PC} = 45 \text{ ns}$ MCM44400C–80 and MCM4L4400C–80, $t_{PC} = 50 \text{ ns}$	I_{CC4}	— — —	110 100 90	mA	1, 3
V_{CC} Power Supply Current (Standby) ($RAS = CAS = V_{CC} - 0.2 \text{ V}$) MCM44400C MCM4L4400C	I_{CC5}	— —	1.0 200	mA μA	
V_{CC} Power Supply Current During CAS Before RAS Refresh Cycle MCM44400C–60 and MCM4L4400C–60, $t_{RC} = 110 \text{ ns}$ MCM44400C–70 and MCM4L4400C–70, $t_{RC} = 130 \text{ ns}$ MCM44400C–80 and MCM4L4400C–80, $t_{RC} = 150 \text{ ns}$	I_{CC6}	— — —	110 100 90	mA	1
V_{CC} Power Supply Current, Battery Backup Mode — MCM4L4400C Only ($t_{RC} = 125 \mu\text{s}$; $CAS = CAS$ Before RAS Cycling or 0.2 V ; $G, W = V_{CC} - 0.2 \text{ V}$; $A0 - A9 = V_{CC} - 0.2 \text{ V}$ or 0.2 V ; $DQ0 - DQ3 = V_{CC} - 0.2 \text{ V}$ or 0.2 V or OPEN; $t_{RAS} = \text{Min to } 1 \mu\text{s}$)	I_{CC7}	—	300	μA	1, 4
Standby Current $RAS = V_{IH}$ $CAS = V_{IL}$ $Q = \text{Enable}$	I_{CC8}	—	5	mA	1
Input Leakage Current ($0 \text{ V} \leq V_{in} \leq 6.5 \text{ V}$)	$I_{lkg(I)}$	– 10	10	μA	
Output Leakage Current ($CAS = V_{IH}$, $0 \text{ V} \leq V_{out} \leq 5.5 \text{ V}$)	$I_{lkg(O)}$	– 10	10	μA	
Output High Voltage ($I_{OH} = -5 \text{ mA}$)	V_{OH}	2.4	V_{CC}	V	
Output Low Voltage ($I_{OL} = 4.2 \text{ mA}$)	V_{OL}	0	0.4	V	

NOTES:

- Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
- Column address can be changed once or less while $RAS = V_{IL}$.
- Column address can be changed once or less while $CAS = V_{IH}$.
- $t_{RAS}(\text{max}) = 1 \mu\text{s}$ is only applied to refresh of battery-back up. $t_{RAS}(\text{max}) = 10 \mu\text{s}$ is applied to functional operating.

CAPACITANCE ($f = 1.0 \text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{CC} = 5 \text{ V}$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Input Capacitance — $A0 - A9$ G, RAS, CAS, W	C_{in}	5 7	pF
Output Capacitance ($CAS = V_{IH}$ to Disable Output) $DQ0 - DQ3$	C_{out}	10	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I \Delta t / \Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM44400C-60 MCM4L4400C-60		MCM44400C-70 MCM4L4400C-70		MCM44400C-80 MCM4L4400C-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RELREL}	t _{RC}	110	—	130	—	150	—	ns	6
Read-Write Cycle Time	t _{RELREL}	t _{RWC}	150	—	180	—	200	—	ns	6
Fast Page Mode Cycle Time	t _{CELCEL}	t _{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t _{CELCEL}	t _{PRWC}	80	—	95	—	100	—	ns	
Access Time from RAS	t _{RELQV}	t _{RAC}	—	60	—	70	—	80	ns	7,8,9
Access Time from CAS	t _{CELQV}	t _{CAC}	—	15	—	20	—	20	ns	7,9,10,11
Access Time from Column Address	t _{AVQV}	t _{AA}	—	30	—	35	—	40	ns	7,9,11,12
Access Time from Precharge CAS	t _{CEHQV}	t _{CPA}	—	35	—	40	—	45	ns	7,9,11
Output Buffer and Turn-Off Delay	t _{CEHQZ}	t _{OFF}	0	15	0	15	0	15	ns	13
Transition Time (Rise and Fall)	t _T	t _T	3	50	3	50	3	50	ns	1
RAS Precharge Time	t _{REHREL}	t _{RP}	40	—	50	—	60	—	ns	
RAS Pulse Width	t _{RELREH}	t _{RAS}	60	10 k	70	10 k	80	10 k	ns	
RAS Pulse Width (Fast Page Mode)	t _{RELREH}	t _{RASP}	—	100 k	—	100 k	—	100 k	ns	
RAS Hold Time	t _{CELREH}	t _{RSH}	15	—	20	—	20	—	ns	
CAS Hold Time	t _{RELCEH}	t _{CSH}	60	—	70	—	80	—	ns	
CAS Precharge to RAS Hold Time	t _{CEHREH}	t _{RHCP}	35	—	40	—	45	—	ns	
CAS Pulse Width	t _{CELCEH}	t _{CAS}	15	10 k	20	10 k	20	10 k	ns	
RAS to CAS Delay Time	t _{RELCEL}	t _{RCD}	20	45	20	50	20	60	ns	14
RAS to Column Address Delay Time	t _{RELAV}	t _{RAD}	15	30	15	35	15	40	ns	15

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 μs is required after power-up followed by 8 initialization cycles (RAS only refresh cycle or CAS before RAS refresh cycle) before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements assume t_T = 5.0 ns.
5. In delayed write or read modify write cycles, must disable output buffer prior to applying data to the device.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
7. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that t_{RCD} ≤ t_{RCD} (max) and t_{RAD} ≤ t_{RAD} (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, and t_{CPA} is delayed for 2 ns to 5 ns for the specified value. These parameters should be in the test mode cycles by adding the above value to the specified value in the data sheet.
10. Assumes that t_{RCD} ≥ t_{RCD} (max) and t_{RAD} ≤ t_{RAD} (max).
11. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
12. Assumes that t_{RCD} ≤ t_{RCD} (max) and t_{RAD} ≥ t_{RAD} (max).
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM44400C-60 MCM4L4400C-60		MCM44400C-70 MCM4L4400C-70		MCM44400C-80 MCM4L4400C-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
CAS to RAS Precharge Time	t _{CEHREL}	t _{CRP}	10	—	10	—	10	—	ns	
CAS Precharge Time	t _{CEHCEL}	t _{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t _{AVREL}	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RELAX}	t _{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t _{AVCEL}	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CELAX}	t _{CAH}	15	—	15	—	15	—	ns	
Column Address to RAS Lead Time	t _{AVREH}	t _{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t _{WHCEL}	t _{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to CAS	t _{CEHWX}	t _{RCH}	0	—	0	—	0	—	ns	16
Read Command Hold Time Referenced to RAS	t _{REHWX}	t _{RRH}	0	—	0	—	0	—	ns	16
Write Command Hold Time Referenced to CAS	t _{CELWH}	t _{WCH}	15	—	15	—	15	—	ns	
Write Command Pulse Width	t _{WLWH}	t _{WP}	10	—	10	—	10	—	ns	
Write Command to RAS Lead Time	t _{WLREH}	t _{RWL}	15	—	20	—	20	—	ns	
Write Command to CAS Lead Time	t _{WLCEH}	t _{CWL}	15	—	20	—	20	—	ns	
Data in Setup Time	t _{DVCEL}	t _{DS}	0	—	0	—	0	—	ns	17
Data in Hold Time	t _{CELDX}	t _{DH}	15	—	15	—	15	—	ns	17
Refresh Period MCM44400C MCM4L4400C	t _{RVRV}	t _{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t _{WLCEL}	t _{WCS}	0	—	0	—	0	—	ns	18
CAS to Write Delay	t _{CELWL}	t _{CWD}	35	—	45	—	45	—	ns	18
RAS to Write Delay	t _{RELWL}	t _{RWD}	80	—	95	—	105	—	ns	18
Column Address to Write Delay Time	t _{AVWL}	t _{AWD}	50	—	60	—	65	—	ns	18
CAS Precharge to Write Delay Time (Page Mode)	t _{CEHWL}	t _{CPWD}	55	—	65	—	70	—	ns	18
CAS Setup Time for CAS Before RAS Refresh	t _{RELCEL}	t _{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t _{RELCEH}	t _{CHR}	10	—	10	—	10	—	ns	
RAS Precharge to CAS Active Time	t _{REHCEL}	t _{RPC}	10	—	10	—	10	—	ns	
CAS Precharge Time for CAS Before RAS Counter Time	t _{CEHCEL}	t _{CPT}	40	—	40	—	40	—	ns	
G Access Time	t _{GLQV}	t _{GA}	—	15	—	20	—	20	ns	7, 9
G to Data Delay	t _{GLHDX}	t _{GD}	15	—	20	—	20	—	ns	

(continued)

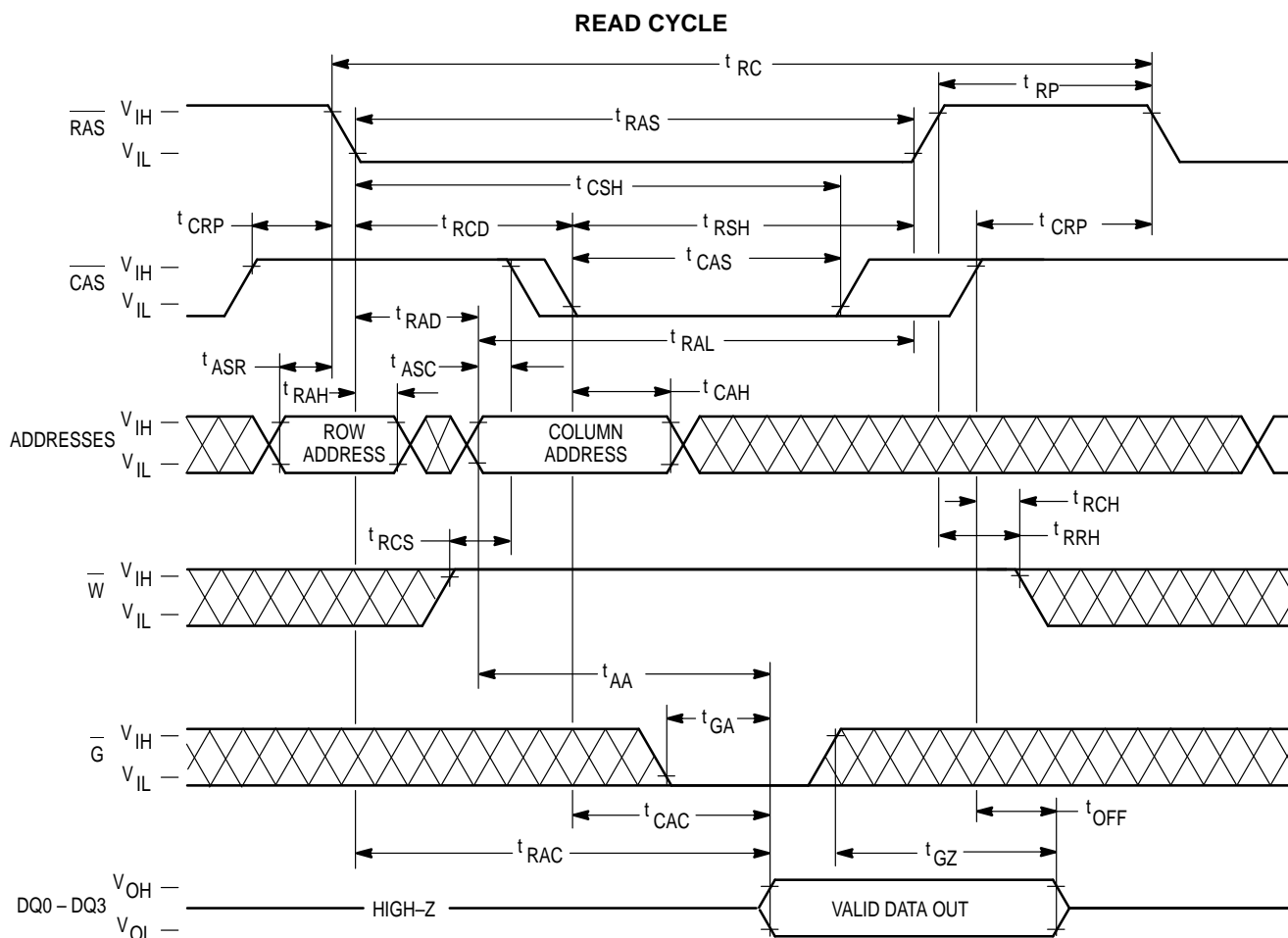
 16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

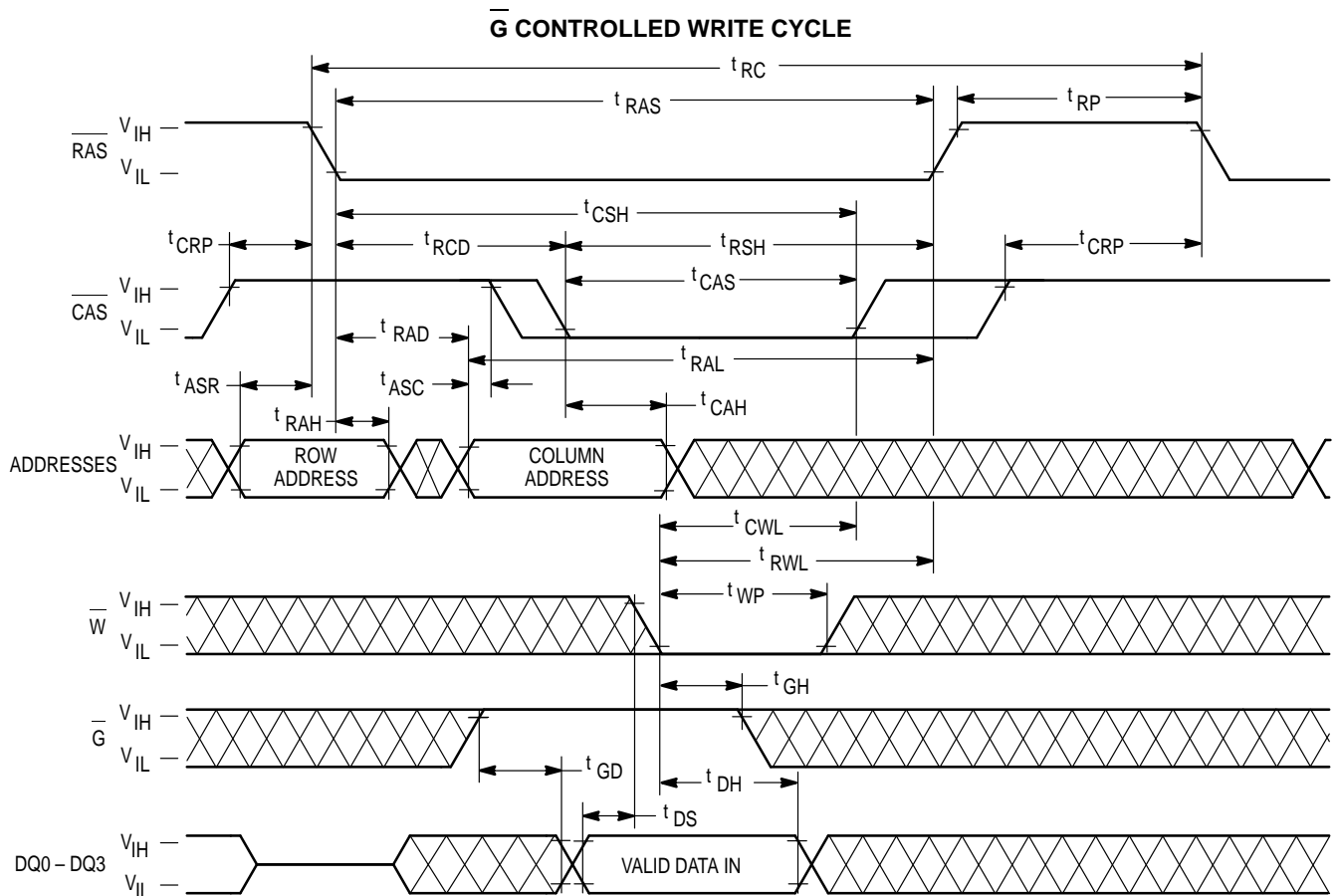
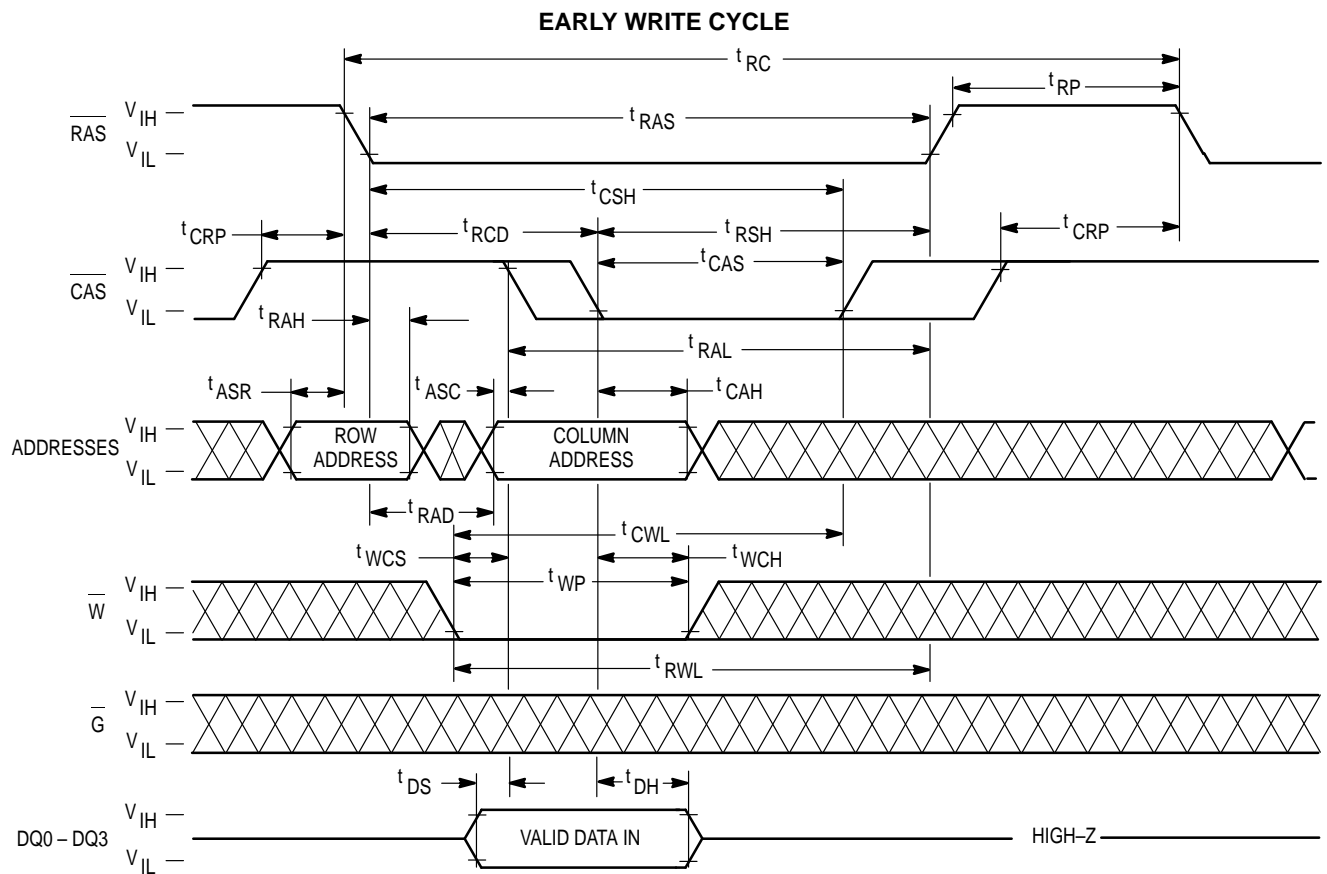
17. These parameters are referenced to CAS leading edge in early write cycles and to W leading edge in read-write cycles.

 18. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{CWD} ≥ t_{CWD} (min), t_{RWD} ≥ t_{RWD} (min), t_{AWD} ≥ t_{AWD} (min), and t_{CPWD} ≥ t_{CPWD} (min) (page mode) the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

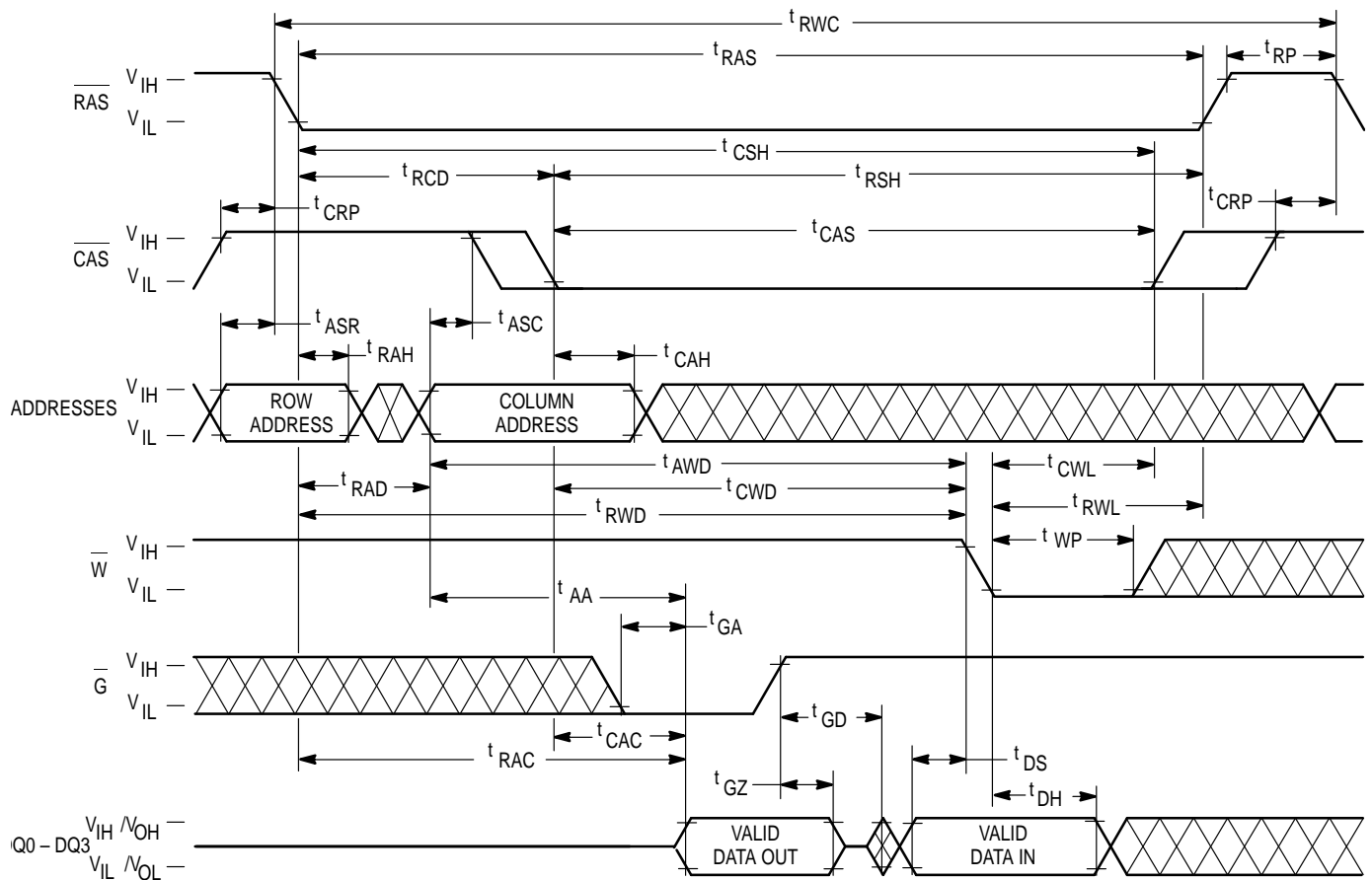
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM44400C-60 MCM4L4400C-60		MCM44400C-70 MCM4L4400C-70		MCM44400C-80 MCM4L4400C-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write to RAS Precharge Time (CAS Before RAS Refresh)	t_{WHREL}	t_{WRP}	0	—	0	—	0	—	ns	
Write to RAS Hold Time (CAS Before RAS Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	
Output Buffer Turn-Off Delay Time from G	t_{GHQZ}	t_{GZ}	0	15	0	15	0	15	ns	13
G Command Hold Time	t_{WLGL}	t_{GH}	15	—	20	—	20	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	0	—	0	—	0	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	





READ-WRITE CYCLE



The diagram illustrates the timing relationships for a memory device. The signals shown are:

- RAS**: Row Address Strobe, with high (V_{IH}) and low (V_{IL}) levels.
- CAS**: Column Address Strobe, with high (V_{IH}) and low (V_{IL}) levels.
- ADDRESSES**: Data bus for addresses, with high (V_{IH}) and low (V_{IL}) levels. It shows **ROW ADDRESS** and **COLUMN ADDRESS** periods.
- W**: Write Enable, with high (V_{IH}) and low (V_{IL}) levels.
- G**: Gate, with high (V_{IH}) and low (V_{IL}) levels.
- DQ0-DQ3**: Data bus, with high (V_{OH}) and low (V_{OL}) levels. It shows **VALID DATA OUT** periods.

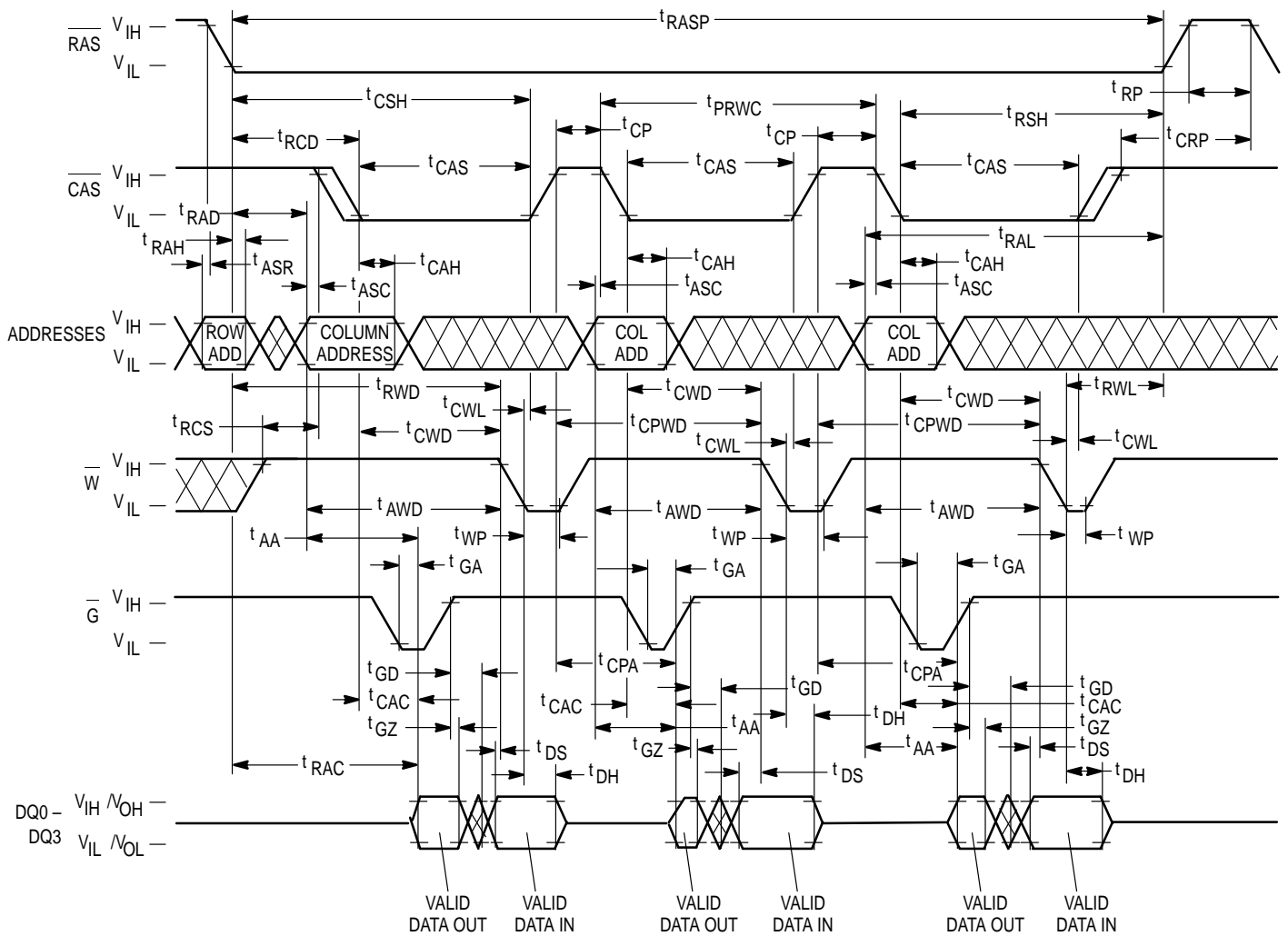
Key timing parameters are indicated by arrows:

- t_{RASP} : RAS pulse width.
- t_{CRP} : RAS to CAS delay.
- t_{RCD} : RAS to CAS delay.
- t_{CAS} : CAS pulse width.
- t_{CP} : CAS to RAS delay.
- t_{PC} : CAS to RAS delay.
- t_{RSH} : RAS to SH (Sense Amplifier) delay.
- t_{CAS} : CAS to SH delay.
- t_{CRP} : RAS to CAS delay.
- t_{RAH} : RAS to Address Hold delay.
- t_{CSH} : CAS to SH delay.
- t_{CAH} : CAS to Address Hold delay.
- t_{ASC} : Address to SH delay.
- t_{RCS} : RAS to SH delay.
- t_{RCH} : RAS to SH delay.
- t_{AA} : Address to SH delay.
- t_{GA} : Gate to SH delay.
- t_{CAC} : CAS to SH delay.
- t_{RAC} : RAS to SH delay.
- t_{OFF} : SH to SH delay.
- t_{GZ} : Gate to SH delay.
- t_{RRH} : RAS to SH delay.
- t_{RP} : RAS to SH delay.

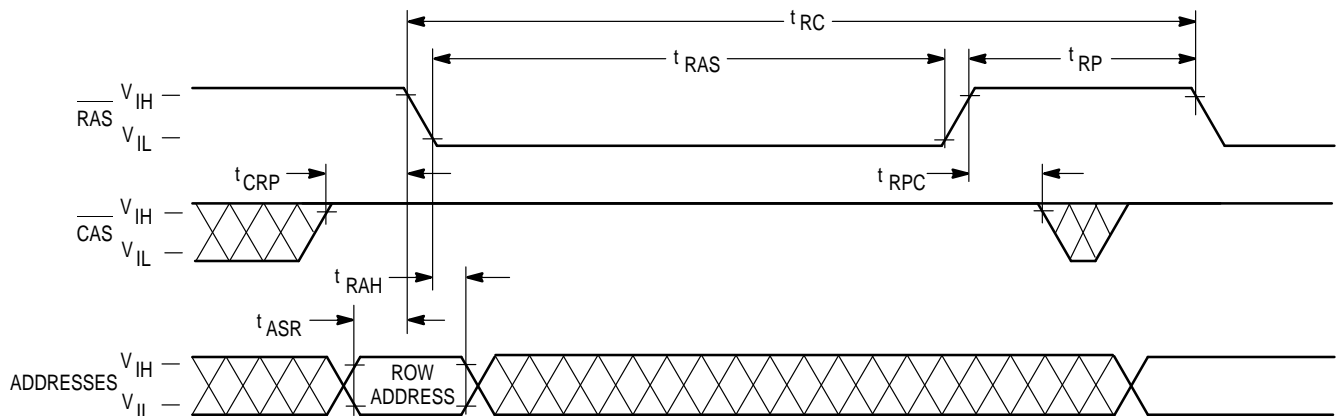
The diagram illustrates the timing relationships for a 2D array memory device. It shows the following signals and their timing parameters:

- RAS:** Row Address Strobe. Timing parameters include t_{RAS} (pulse width), t_{RHCP} (hold time after pulse), and t_{RP} (return time to high level).
- CAS:** Column Address Strobe. Timing parameters include t_{CRP} (pulse width), t_{RCD} (row-to-column delay), t_{CAS} (pulse width), t_{CP} (hold time after pulse), t_{PC} (period), t_{RSH} (row-to-strobe hold time), and t_{ASR} (address-to-strobe rise time).
- ADDRESSES:** Row and Column addresses. Timing parameters include t_{RAH} (row address hold time), t_{ASH} (address-to-strobe hold time), t_{ASC} (address-to-column delay), t_{CAH} (column address hold time), t_{RAD} (row address delay), t_{CWL} (column word line delay), t_{WCS} (word column strobe delay), t_{RHL} (row hold time), and t_{CAH} (column address hold time).
- W:** Write Enable. Timing parameters include t_{WP} (pulse width), t_{WCH} (word column hold time), and t_{WCS} (word column strobe delay).
- G:** Ground reference signal.
- DQ0-DQ3:** Data bus. Timing parameters include t_{DS} (data strobe delay) and t_{DH} (data hold time).

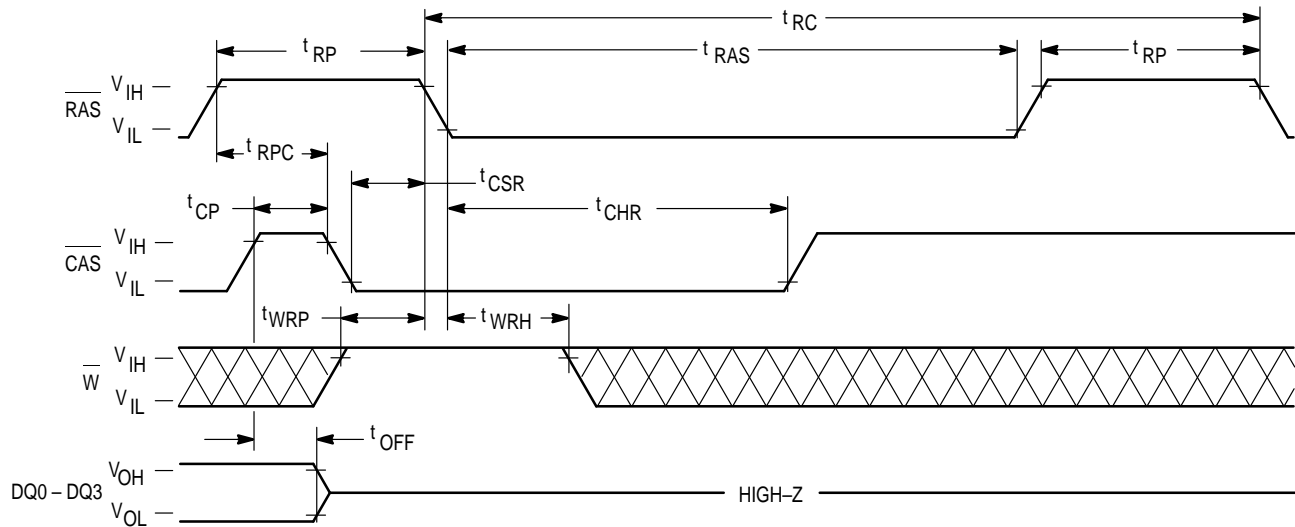
FAST PAGE MODE READ-WRITE CYCLE



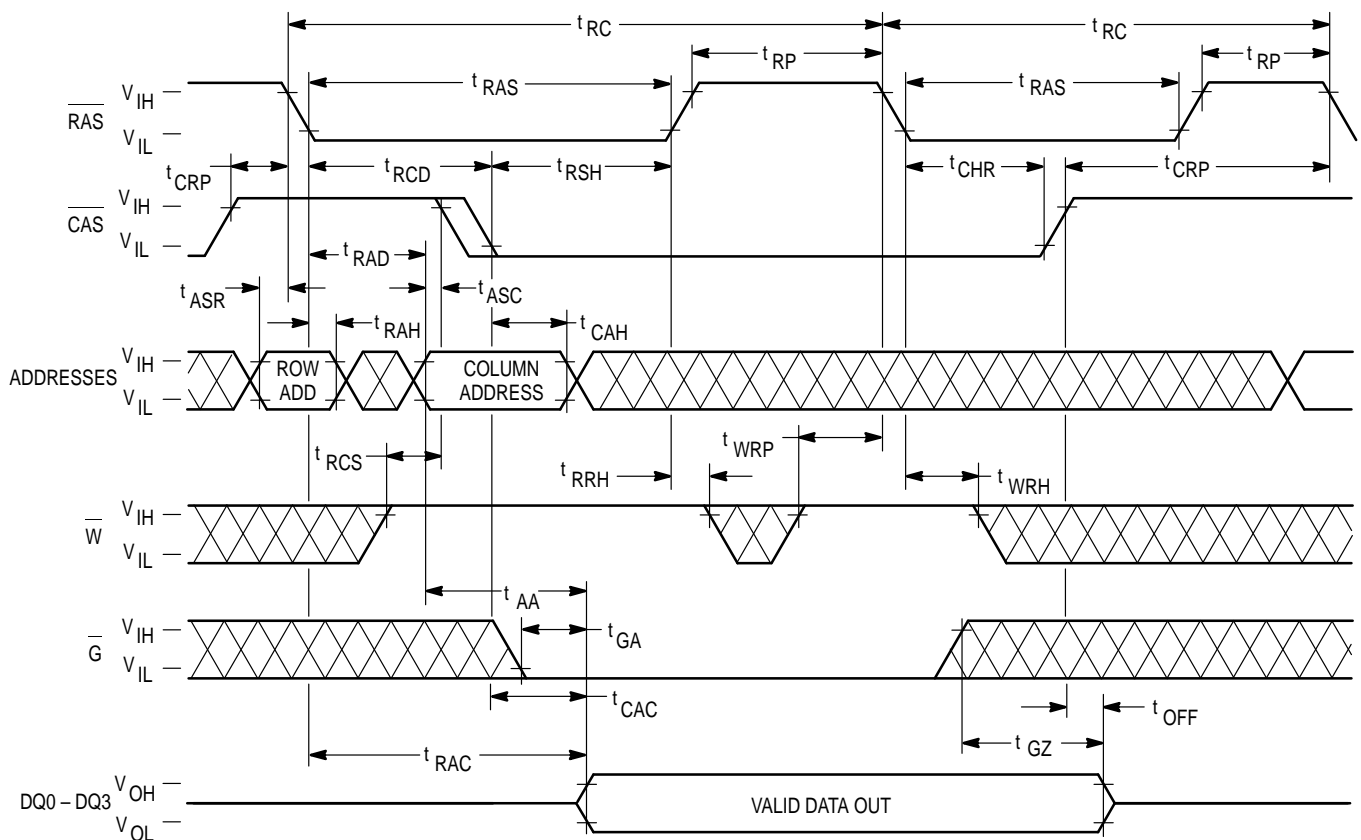
RAS-ONLY REFRESH CYCLE (W and G are Don't Care)



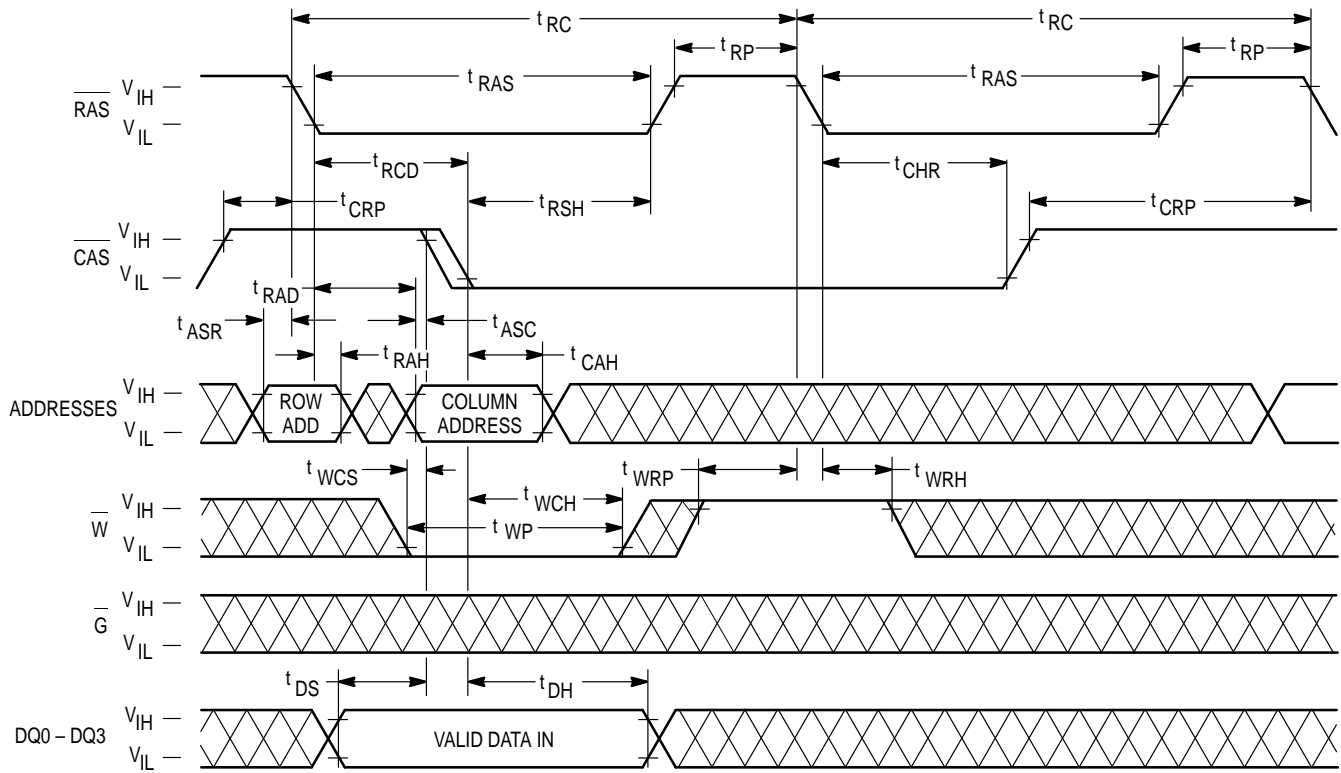
CAS BEFORE RAS REFRESH CYCLE
(G and A0 – A9 are Don't Care)



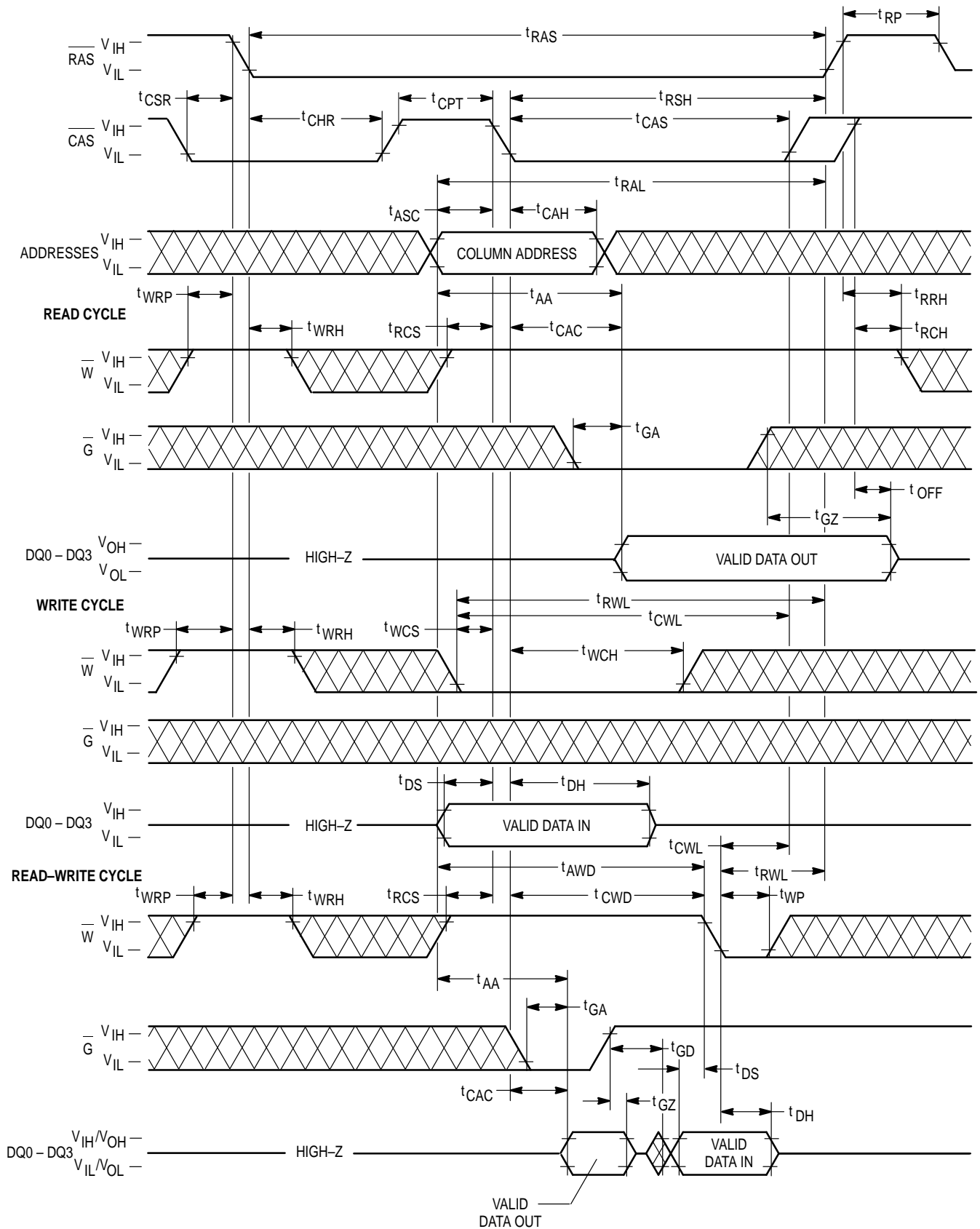
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up, an initial pause of 100 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. RAS active transition is followed by CAS active transition (active = V_{IL} , t_{RCD} minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the 1M x 4 RAM: **RAS-only refresh cycle**, **CAS before RAS refresh cycle**, and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (\overline{W}) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both CAS and output enable (\overline{G}) control read access time: CAS must be active before or at t_{RCD} maximum and \overline{G} must be active $t_{RAC} - t_{GA}$ (both minimum) after RAS active transition to guarantee valid data out (Q) at t_{RAC} (access time from RAS active transition). If the t_{RCD} maximum is exceeded and/or \overline{G} active transition does not occur in time, read access time is determined by either the CAS or \overline{G} clock active transition (t_{CAC} or t_{GA}).

The RAS and CAS clocks must remain active for minimum times of t_{RAS} and t_{CAS} , respectively, to complete the read cycle. \overline{W} must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after RAS or CAS inactive transition,

respectively, to maintain the data at that bit location. Once RAS transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the CAS and \overline{G} clocks are active. When either the CAS or \overline{G} clock transitions to inactive, the output will switch to High-Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of \overline{W} to active (V_{IL}). Early and late write modes are distinguished by the active transition of \overline{W} , with respect to CAS. Minimum active time t_{RAS} and t_{CAS} , and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by \overline{W} active transition at minimum time t_{WCS} before CAS active transition. Data in (\overline{D}) is referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL} , respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because \overline{W} active transition precedes or coincides with CAS active transition, keeping data-out buffers and \overline{G} disabled.

A late write cycle (referred to as \overline{G} -controlled write) occurs when \overline{W} active transition is made after CAS active transition. \overline{W} active transition could be delayed for almost 10 microseconds after CAS active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T \leq t_{RAS}$, if other timing minimums (t_{RCD} , t_{RWL} , and t_T) are maintained. \overline{D} is referenced to \overline{W} active transition in a late write cycle. Output buffers are enabled by CAS active transition but outputs are switched off by \overline{G} inactive transition, which is required to write to the device. Q may be indeterminate (see note 18 of the AC Operating Conditions table). RAS and CAS must remain active for t_{RWL} and t_{CWL} , respectively, after \overline{W} active transition to complete the write cycle. \overline{G} must remain inactive for t_{GH} after \overline{W} active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except \overline{W} must remain high for t_{CWD} minimum after the CAS active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the 1M x 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC} . Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL} . The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP} , while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read–write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP} . Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM44400C require refresh every 16 milliseconds, while refresh time for the MCM4L4400C is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM44400C, and 124.8 microseconds for the MCM4L4400C. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM44400C and 128 milliseconds on the MCM4L4400C.

A normal read, write, or read–write operation to the RAM will refresh all the bits (4096) associated with the particular row decodes. Three other methods of refresh, **RAS–only refresh**, **CAS before RAS refresh**, and **hidden refresh** are available on this device for greater system flexibility.

RAS–Only Refresh

RAS–only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a test mode cycle.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight CAS before RAS initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 1024 times.
3. Read the 1s which were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 1024 times.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one to five using complement data.

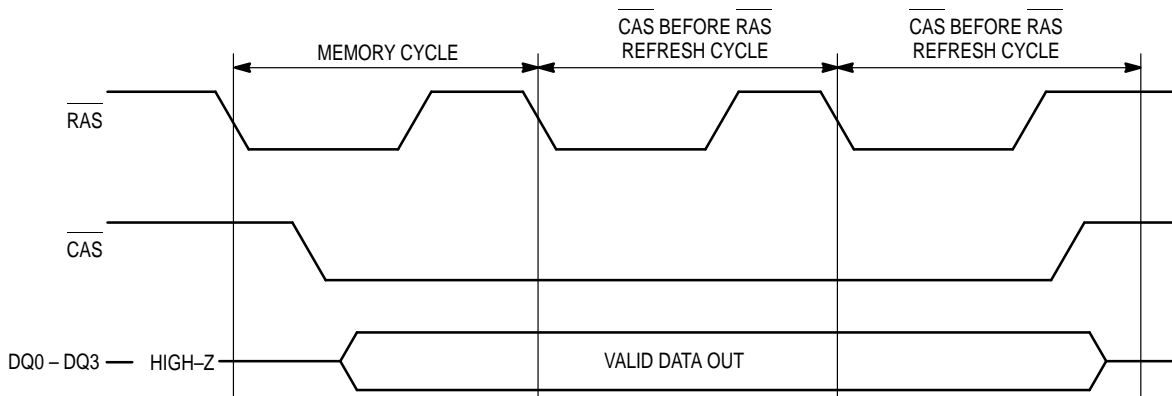


Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 4 DRAM. Nineteen of the twenty addresses are used when operating the device in test mode. Column address A0 is ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of

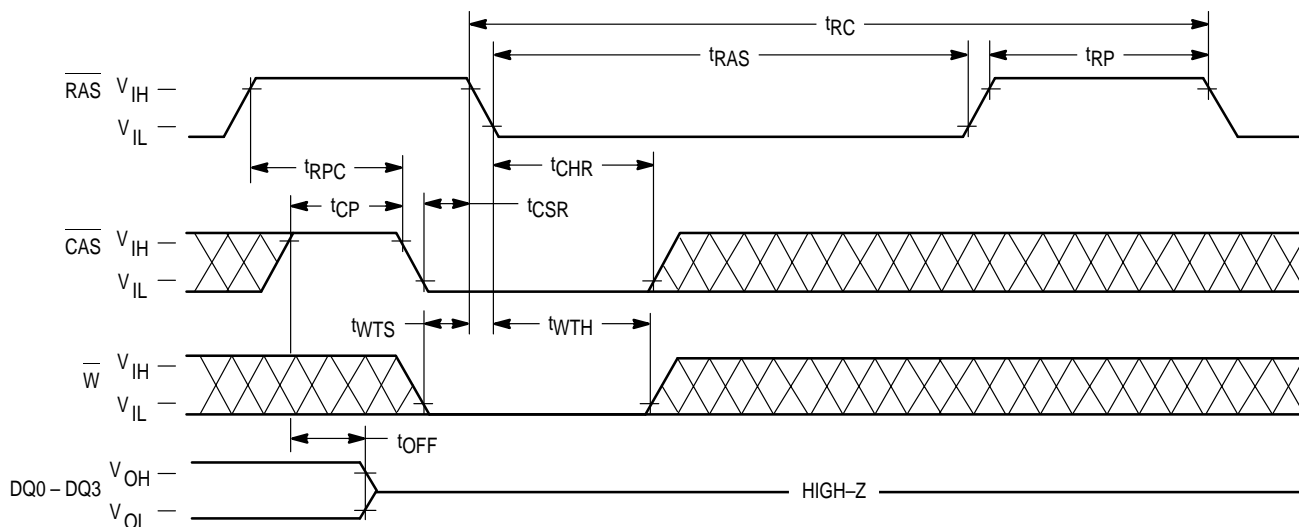
the device. See following truth table and test mode block diagram.

\overline{W} , CAS before RAS timing puts the device in **Test Mode** as shown in the test mode timing diagram. A **CAS before RAS** or a **RAS-only refresh cycle** puts the device back into normal mode. Refresh is performed in test mode by using a **W, CAS before RAS refresh cycle** which uses internal refresh address counter.

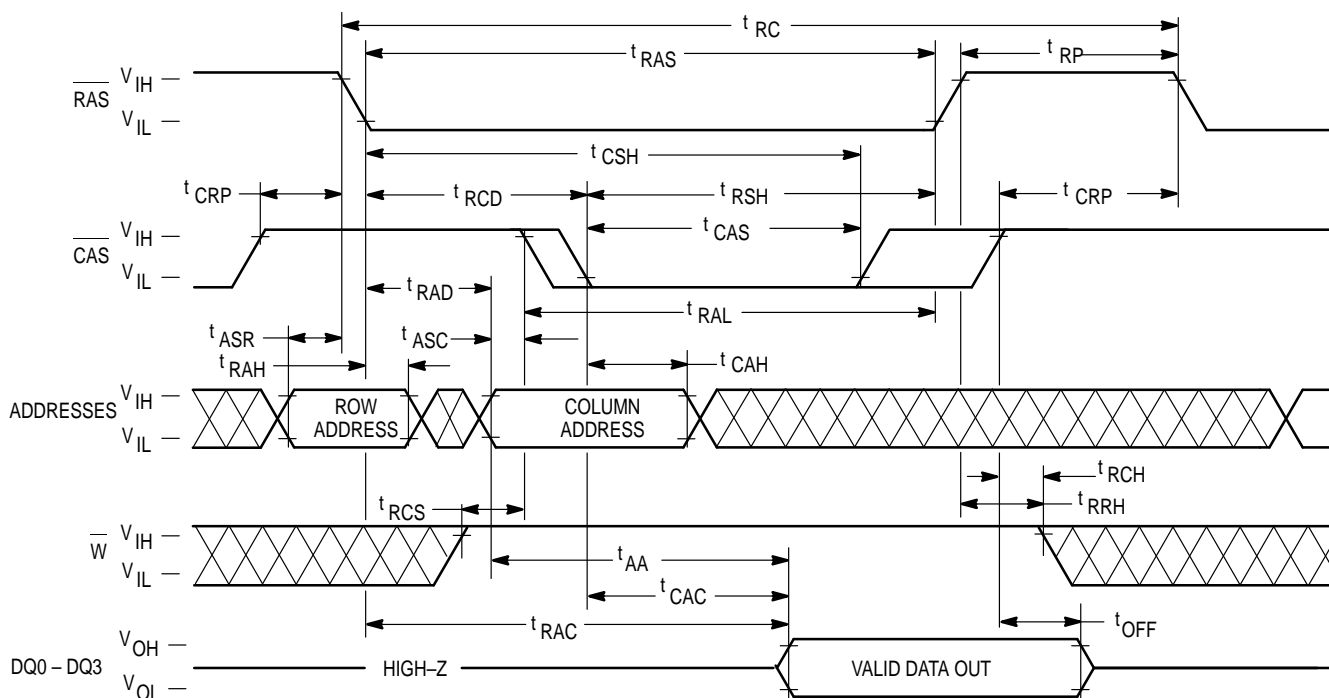
TEST MODE TRUTH TABLE

D	B0, B1	B2, B3	B4, B5	B6, B7	Q
0	0	0	0	0	1
1	1	1	1	1	1
—	Any Other				0

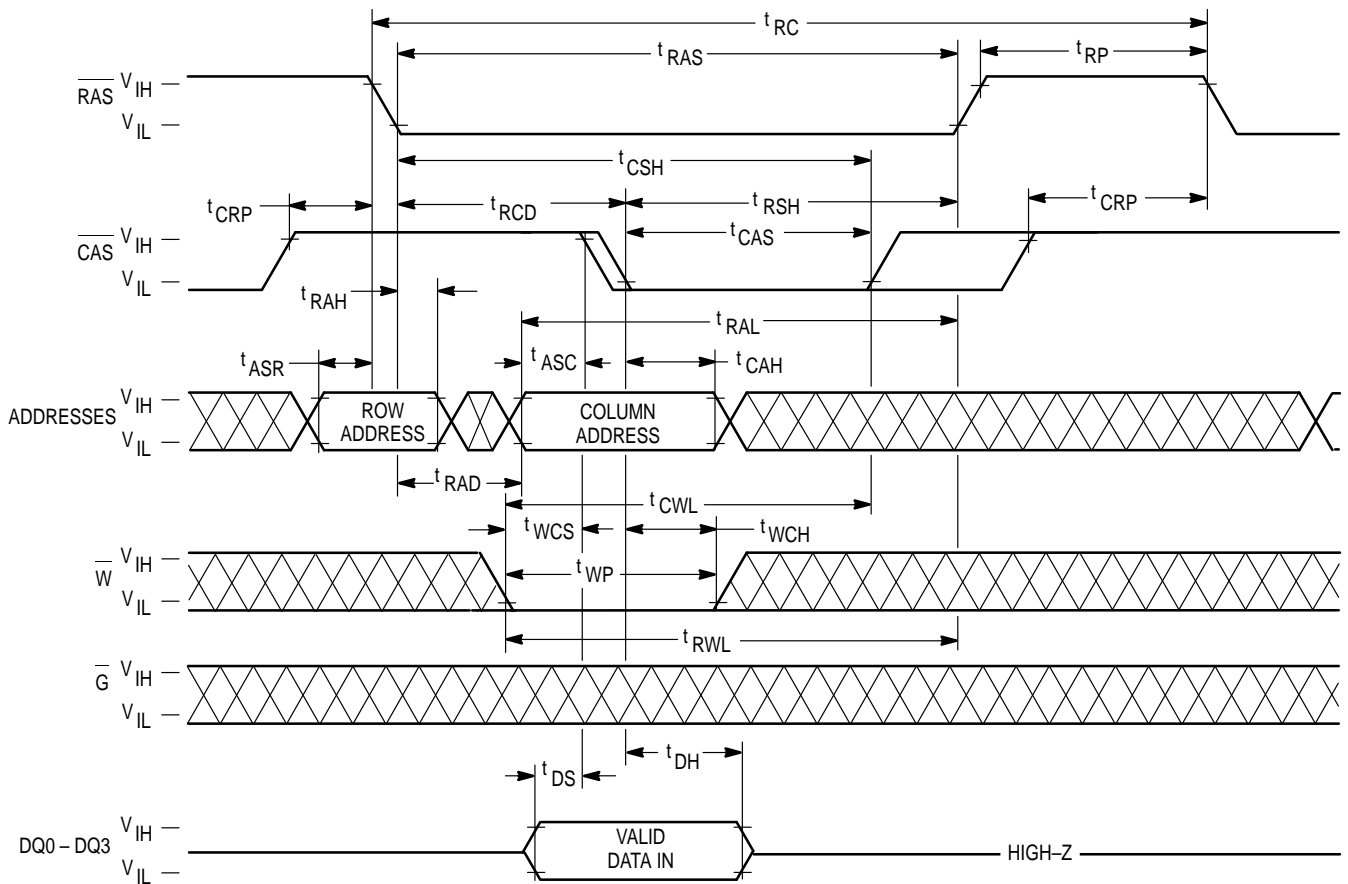
W, CAS BEFORE RAS REFRESH CYCLE (TEST MODE ENTRY)
(G and A0 – A9 are Don't Care)



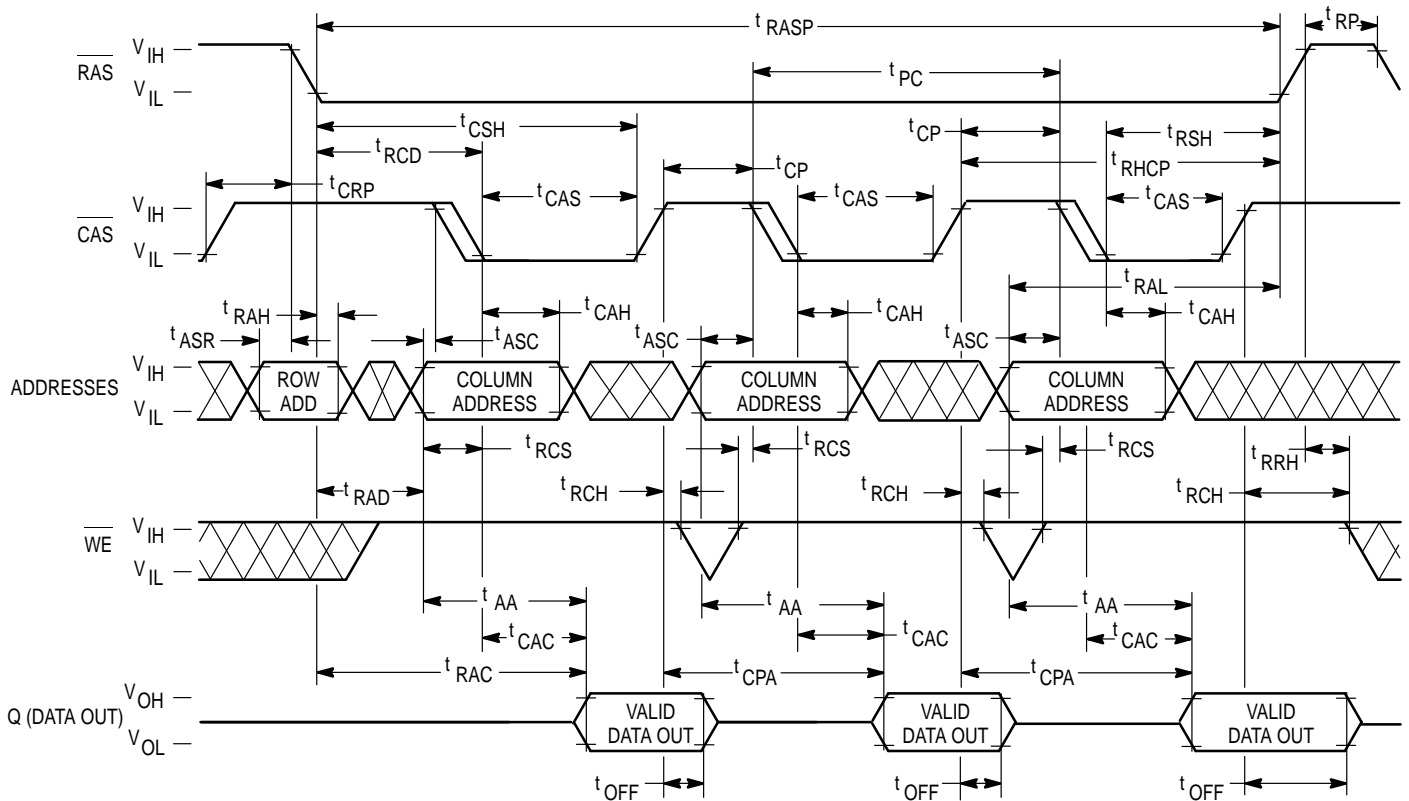
TEST MODE — READ CYCLE



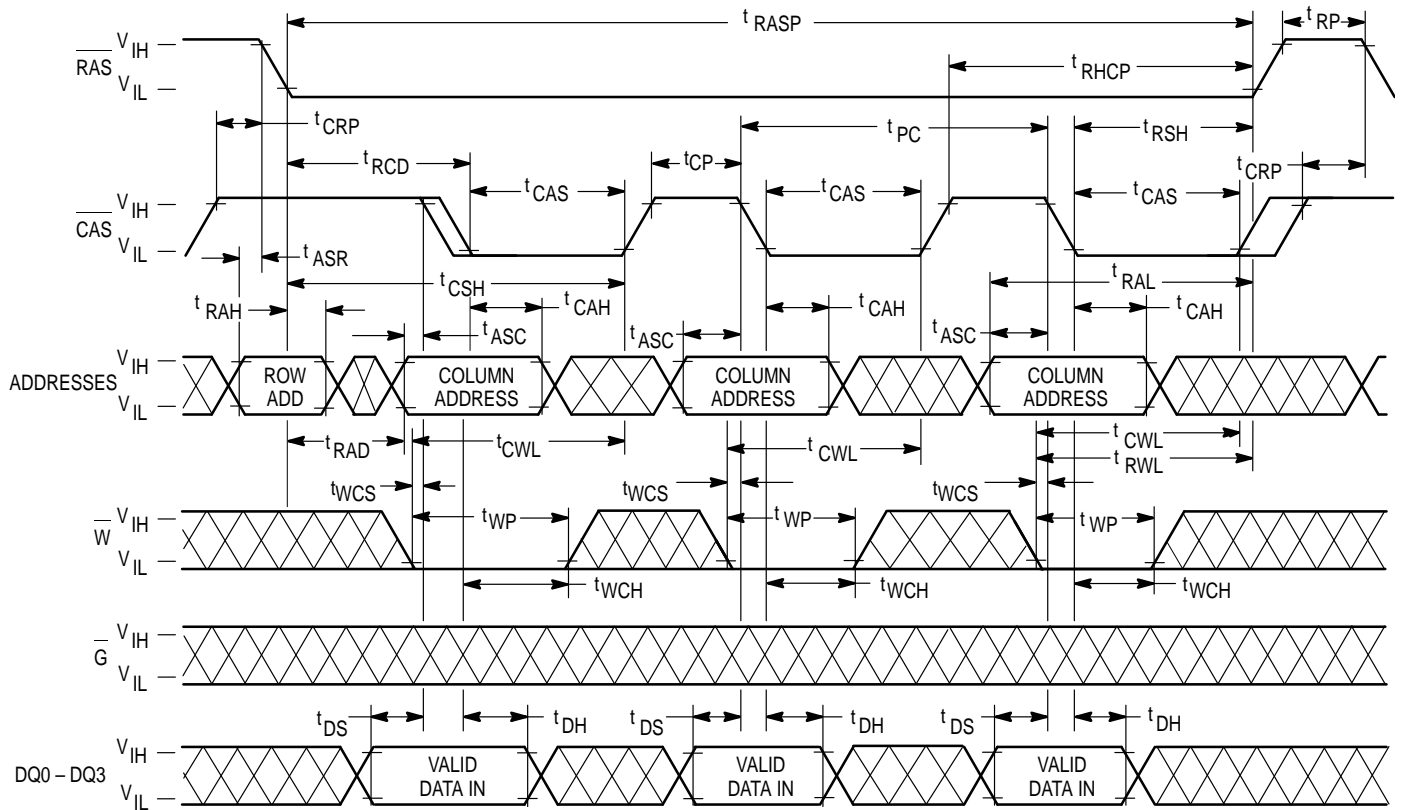
TEST MODE — EARLY WRITE CYCLE



TEST MODE — FAST PAGE MODE READ CYCLE (G = Low)



TEST MODE — FAST PAGE MODE EARLY WRITE CYCLE

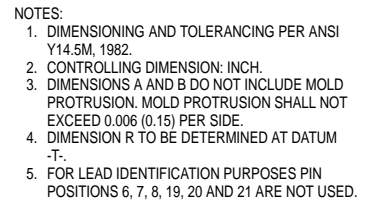


ORDERING INFORMATION (Order by Full Part Number)

MCM 44400C or 4L4400C X XX XX
 Motorola Memory Prefix —
 Part Number —
 Shipping Method (R2 = Tape and Reel, Blank = Rails)
 Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns)
 Package (N = 300 mil SOJ)

Full Part Numbers — MCM44400CN60 MCM44400CN60R2
 MCM44400CN70 MCM44400CN70R2
 MCM44400CN80 MCM44400CN80R2
 MCM4L4400CN60 MCM4L4400CN60R2
 MCM4L4400CN70 MCM4L4400CN70R2
 MCM4L4400CN80 MCM4L4400CN80R2

**N PACKAGE
300 MIL SOJ
CASE 822B-01**



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.661	0.680	16.79	17.27
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.25	3.76
D	0.015	0.021	0.38	0.53
E	0.085	0.103	2.16	2.61
F	0.026	0.032	0.66	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.025	0.045	0.63	1.14
L	0.100 BSC		2.54 BSC	
M	0 °	20 °	0 °	20 °
N	0.035	0.059	0.89	1.50
P	0.330	0.340	8.39	8.63
R	0.260	0.275	6.60	6.98
S	0.027	0.040	0.69	1.02

19

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