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MOTOROLA

MC44301

Advance Information

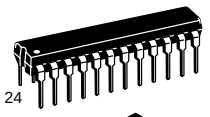
High Performance Color TV IF

HIGH PERFORMANCE COLOR TV IF

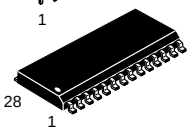
SEMICONDUCTOR TECHNICAL DATA

The MC44301 is a single channel TV IF and PLL detector system for all standard transmission systems. This device enables the designer to produce a high quality IF system with white spot inversion, AFT and AGC. The MC44301 was designed with an emphasis on linearity to minimize sound/picture intermodulation.

- Single Coil Adjustment for AFT and PLL
- VCO at 1/2 IF for Minimum Beats
- Simple Circuitry for Low System Cost
- White Spot Inversion
- Symmetrical ± 2.0 MHz Pull–in
- User Selectable Positive or Negative Modulation
- Auxiliary AM Detector for AM Sound
- Simple Alignment Procedure



P SUFFIX
PLASTIC PACKAGE
CASE 724

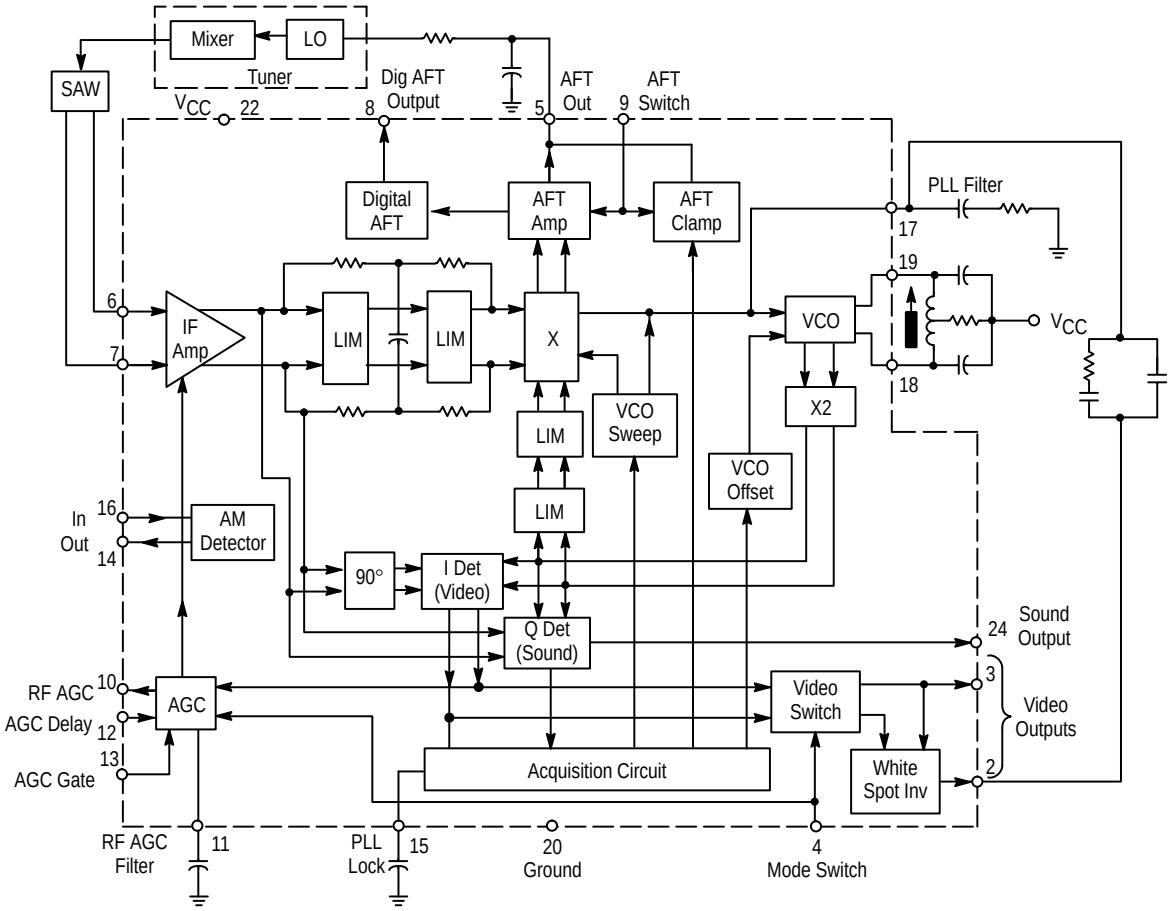


DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO–28L)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44301P	T_A = 0° to 70°C	Plastic DIP
MC44301DW		SO–28L

Figure 1. Representative Block Diagram



NOTE: Pin numbers shown are for DIP package only. Refer to Table 1 for pin assignments.

MAXIMUM OPERATING CONDITIONS

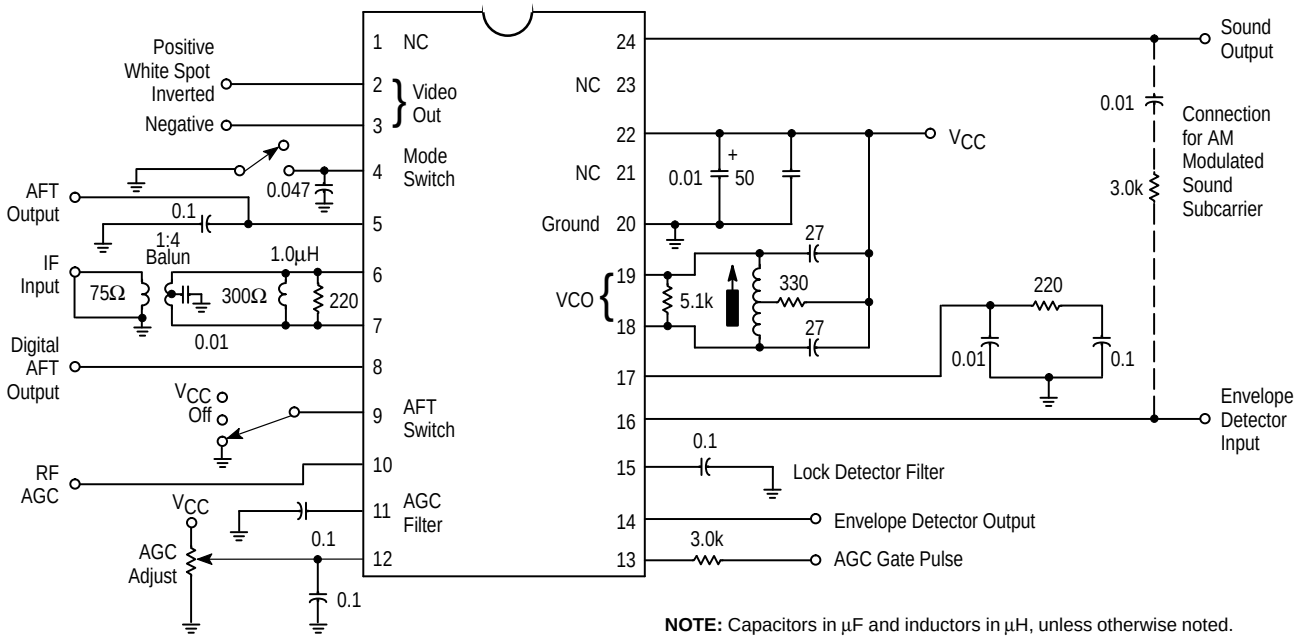
Characteristics	Symbol	Rating	Unit
Power Supply Voltage – Pin 22	V_{CC}	7.0	V
Gating Pulse Amplitude	–	±500	μA pk
Ambient Operating Temperature (Note 1)	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_{Jmax}	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C, unless noted.)

Characteristics	Pin (DIP)	Pin (SOIC)	Min	Typ	Max	Unit
Operating Supply Voltage Range Supply Current	22	27	4.5 –	– 70	5.5 –	Vdc mAdc
Differential Input Sensitivity for Full Output	6,7	7,8	–	30	–	μV_{rms}
Bandwidth Video Bandwidth	2,3	2,3	– –	120 8.0	– –	MHz
AGC Range Noise Figure (R_S = 300 Ω)			– –	80 7.0	– –	dB
Lock–up Time			–	5.0	–	ms
Video Amplitude (100% mod depth)	2,3	2,3	–	2.2	–	Vpp
Tuner AGC Current (10 Vdc; R_{pullup} = 10 k)	10	12	0.6	0.95	–	mAdc
Differential Gain Distortion Differential Phase Distortion (Uncorrected – refer to text description)	2	2	– –	2.0 1.0	5.0 5.0	% Degrees
Sound Subcarrier Output	24	28	–	0.1	–	V_{rms}
AGC Gate Pulse (R_{pin} ≈ 5.0 k)	13	15	–	±0.3	–	mA pk
Differential Input Impedance R_{in} C_{in}	6,7	7,8	– –	3.4 3.0	– –	kΩ pF

NOTE: 1. At 0°C the device only tolerates a 5% change in minimum supply voltage (i.e. 4.75 Vdc is the minimum supply voltage at which the device will function).

Figure 2. Test Circuit



NOTE: Capacitors in μF and inductors in μH, unless otherwise noted.

TYPICAL CURVES

Figure 3. AFT Open Loop Error versus Closed Loop Error

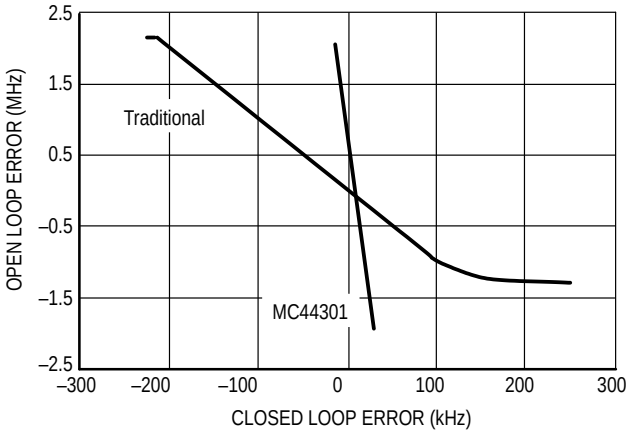


Figure 4. AGC Voltage versus Antenna Input Signal

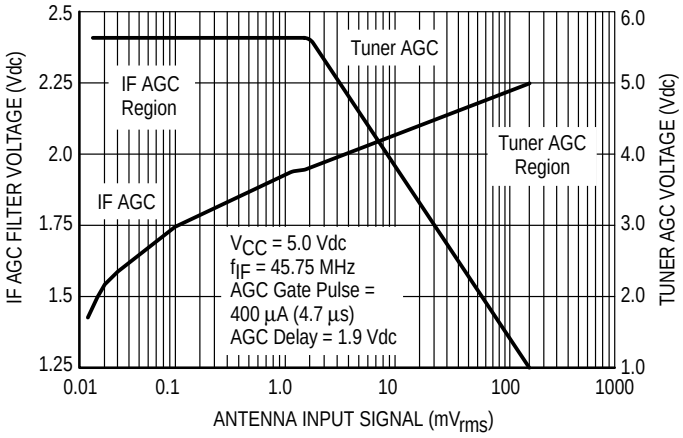


Figure 5. IF Noise Figure versus IF Input

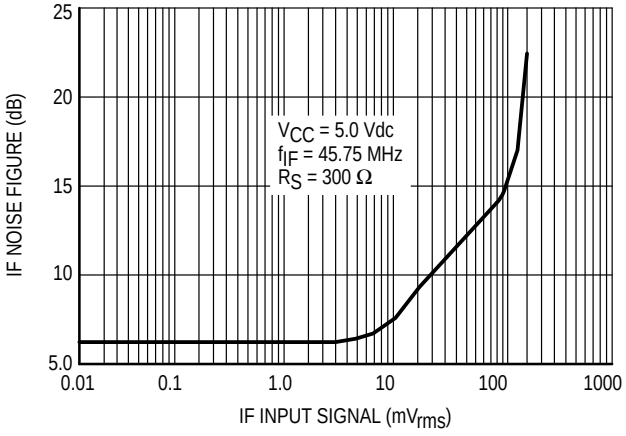
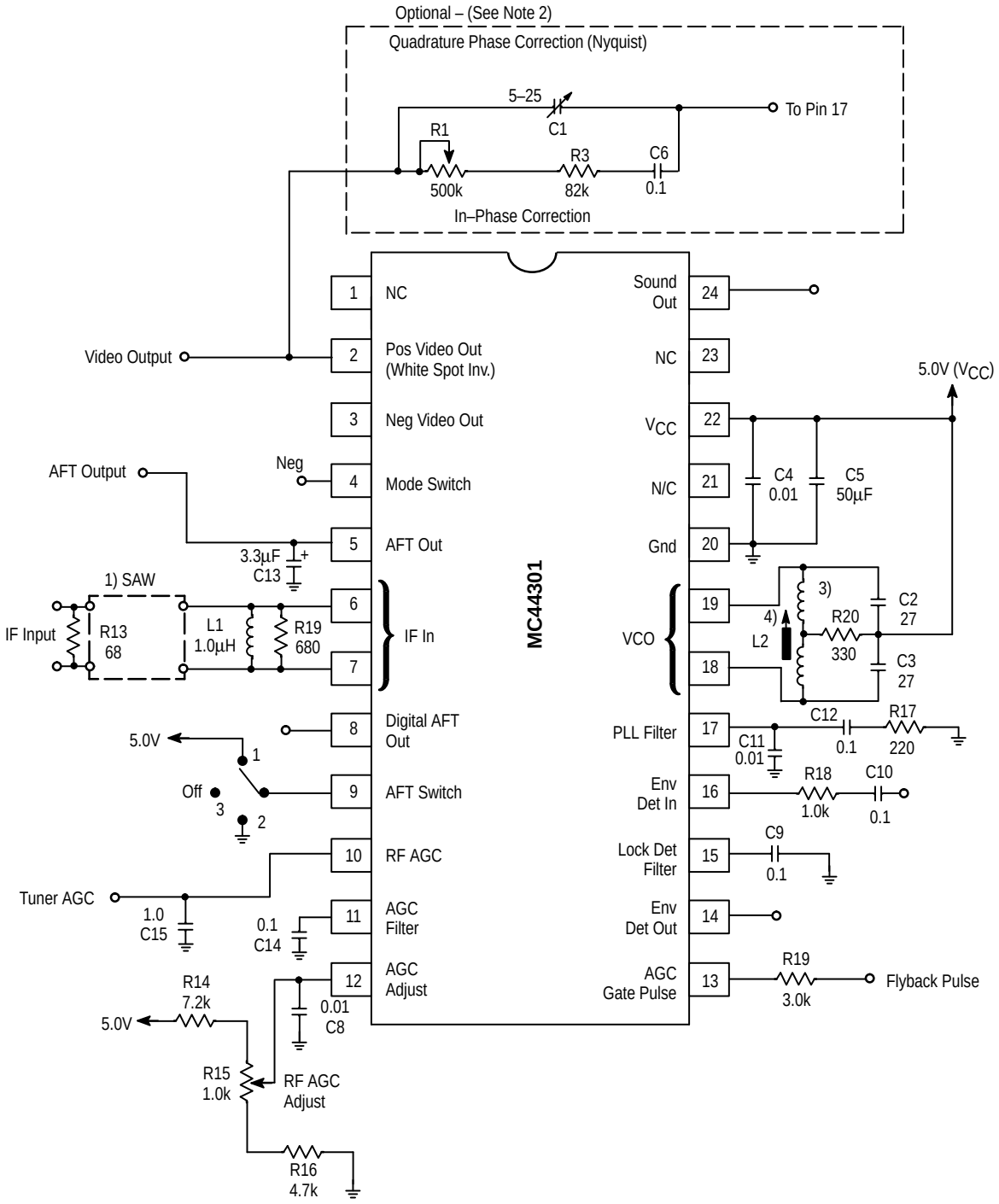


Table 1. Package/Pin Assignments

Description	24 Pin (DIP)	28 Pin (SOIC)
No Connection	1	1
Positive Video Output	2	2
Negative Video Output	3	3
No Connection		4
Mode Switch	4	5
AFT Output	5	6
IF Input (Pos)	6	7
IF Input (Neg)	7	8
Digital AFT Output	8	9
AFT Switch	9	10
No Connection		11
RF AGC	10	12
AGC Filter	11	13
AGC Adjust or Delay	12	14
AGC Gate Pulse	13	15
Envelope Detector Out	14	16
Lock Detector Filter	15	17
No Connection		18
Envelope Detector In	16	19
PLL Filter	17	20
VCO	18	21
VCO	19	22
Ground	20	23
No Connection	21	24
No Connection		25,26
V_{CC}	22	27
No Connection	23	
Sound Output	24	28

Figure 6. Typical 5.0 V Color TV Application



NOTES: 1. IF input assumes 75 Ω output from tuner. The SAW filter should be low loss (<20 dB) with good triple transit response. The Murata 80Z series resin mold SIP type filter has low loss and good TT response. The PCB enclosed in the evaluation kit accommodates these filters and SAF45MA80Z and Siemens M1963. The Zenith SAW filter is packaged in a metal can filter.
2. Optional circuitry to improve sound performance by providing additional quadrature and in–phase corrections.
3. The VCO coil is a shielded 10 mm center–tapped inductor, bifiliar wound. See details in Figure 17.
4. See Figure 17 for coil details.

CIRCUIT DESCRIPTION

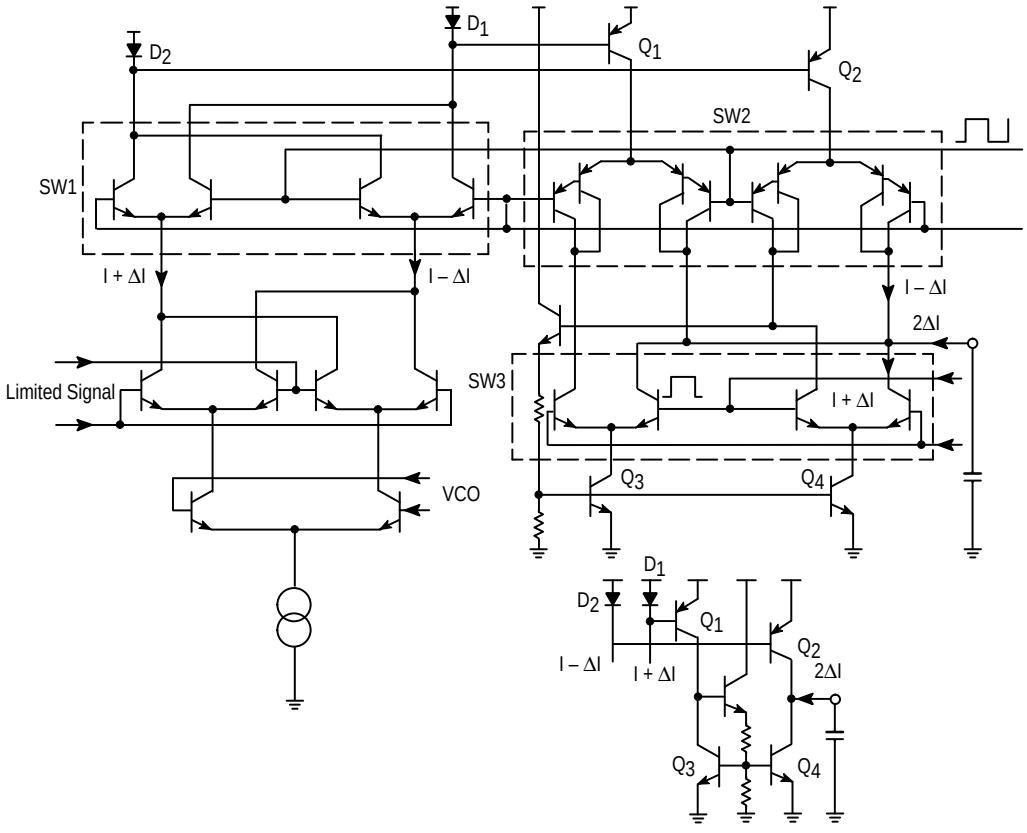
IF Amplifier and AGC

The IF amplifier is a four stage ac coupled amplifier having a sensitivity of 30 μV, thus removing the need for a SAW preamplifier when used with a suitable SAW filter and tuner. The first three stages are gain controlled, giving an extended AGC range of 80 dB with improved signal handling. The AGC to the first stage is delayed as normal so as to preserve the amplifier's noise figure. Reverse AGC is supplied to the tuner and provision is made for the usual tuner RF delay adjustment. The AGC system is gated with a positive or negative pulse. Flyback gating is used for negative modulation and the video is maintained constant by the sync tip being kept equal to an internal voltage reference. When positive modulation is selected, via the mode switch, back porch sampling pulse is used and the internal reference is altered such that the video amplitude remains unchanged. Both polarities of video are provided, and the same sense is kept at the video outputs by means of the video switches.

PLL and Demodulation

Following the IF amplifier and preceding the PLL phase detector is a two stage limiter with a gain of 100 and overall dc feedback. This contrasts with the usual single stage of limiting with no dc feedback and diodes with possibly a tuned circuit at its output. With two stages of limiting, the minimum gain required to remove amplitude modulation can be designed–in without the large voltage swings of a single stage with the same gain. Large voltage swings lead to poor differential phase performance, hence the need for diodes and a tuned circuit as used in previous designs. The dc feedback removes the effects of input offsets which are another source of differential phase. The combination of low swing per stage and dc feedback removes the need for having a tuned circuit at the limiter output and reduces the danger of IF instability and radiation. The only problem in using this technique is the potential for extra static phase shift with resultant errors in the demodulating angles at the video and sound demodulators. However, by putting a similar two stage limiter, with a matching phase shift on the oscillator side of the phase detector, the demodulating angles can be restored to the correct phases (0°, 90°). Phase errors and hence quadrature video distortion can also be caused by dc errors in the phase detector and AFT amplifier (Figure 1). Most of the dc offsets are caused by mismatches in the current mirrors of the push–pull output stage (see simplified stage Figure 7). Switches S_1, S_2 and S_3 are driven by an accurate 1:1 mark/space ratio 1.0 MHz square wave. Switches S_1 and S_2 maintain the same sense of error signal, while S_2 ensures errors due to the top PNP current mirrors average to zero on the external loop filter capacitor. In a similar way, S_3 by interchanging Q_3 and Q_4 cancels errors due to the bottom NPN mirror. With phase errors reduced to a minimum, there is no need for external phase adjustments. The output of the phase detector is filtered and controls the VCO to lock at 90°C phase to the incoming IF signal. The

Figure 7. Phase Detector

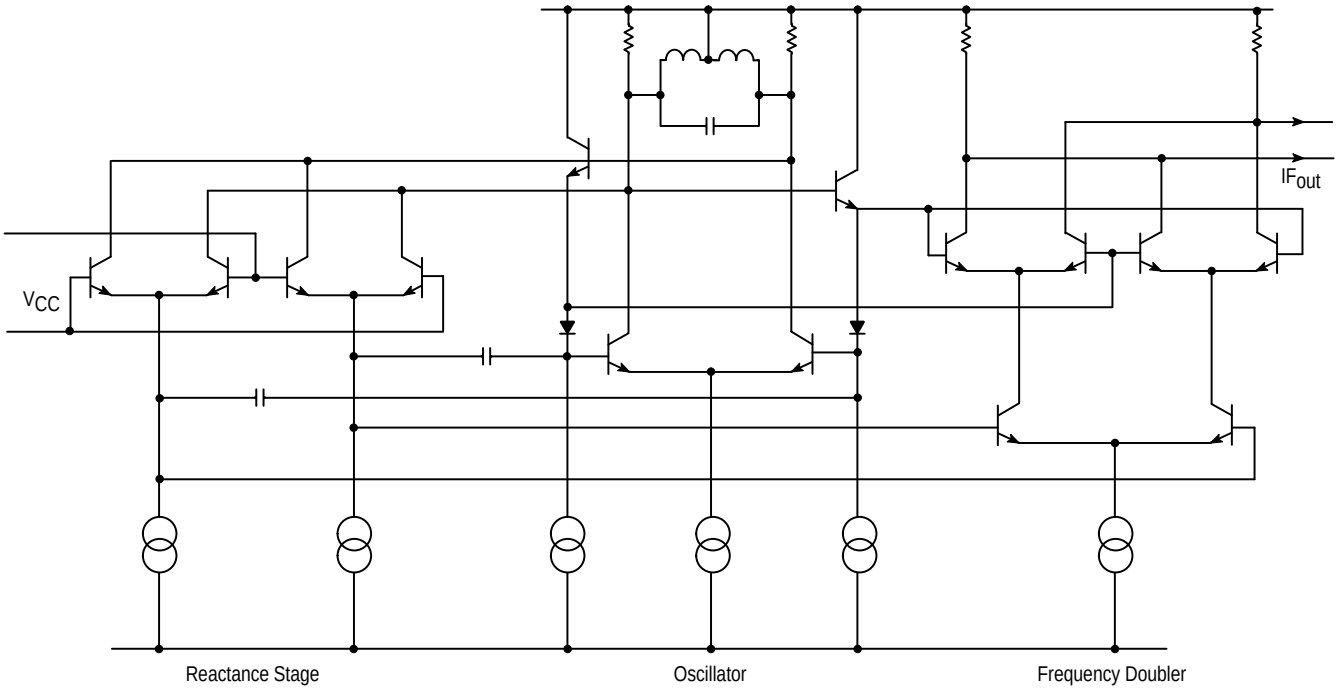


VCO, as shown in Figure 8, is a reactance tuned oscillator at “half IF”. The frequency is doubled by a balanced multiplier, and signals to the multiplier’s input ports are at 90° to each other. Reactance tuning enables a higher Q to be used in the oscillator tank circuit as opposed to a phase shift type of oscillator with the same tuning range. The oscillator being at “half IF” means that radiation from the external frequency–determining components will be at half frequency and so will not desensitize the system even if picked up by the amplifier input leads (PLL push–off). Running the oscillator at twice IF and dividing down, which is another way of solving this problem, has several disadvantages. First and foremost, radiation into the antenna at twice IF produces channel 6 problems in the U.S.A. and possibly channel 8 due to harmonics. It is also much more difficult to produce a stable oscillator at twice the IF frequency than at one–half IF frequency. After attaining phase lock, demodulation of the video is achieved by multiplying the 90° phase shifted signal (nonlimited) with the regenerated vision carrier (VCO) in a double balanced multiplier. The sound FM intercarrier signal is recovered in a similar way by multiplication, but in this case, the phase relationship of signal and VCO is 90° and not 0° as for the video.

Differential Phase Suppression

Even with all the care taken in this design, some residual differential phase still remains. Although low, it would degrade stereo sound performance. In addition, there is the quadrature differential phase produced by the IF filter to be considered. Both produce currents in the output of the phase detector which in turn phase modulates the VCO. This phase modulation is transferred to the sound intercarrier and hence produces video related sound interference. With the correct phase of demodulated video, these currents can be eliminated at the output of the phase detector, as shown in Figure 6, by the network connected to the PLL filter. The phase detector current, due to the in–phase differential gain, is cancelled by the resistor current, while the capacitive current cancels the quadrature component induced by the IF filter. This technique enables the level of performance to be taken to the point where the use of the parallel sound IF is now unnecessary. Here it should be pointed out that in many cases the *improved sound quality* of a parallel sound system has proved to be illusive. The gain in quality accrued by removing IF filter phase modulation is often more than offset by imperfections in the regeneration of the vision carrier (VCO).

Figure 8. VCO and Frequency Doubler



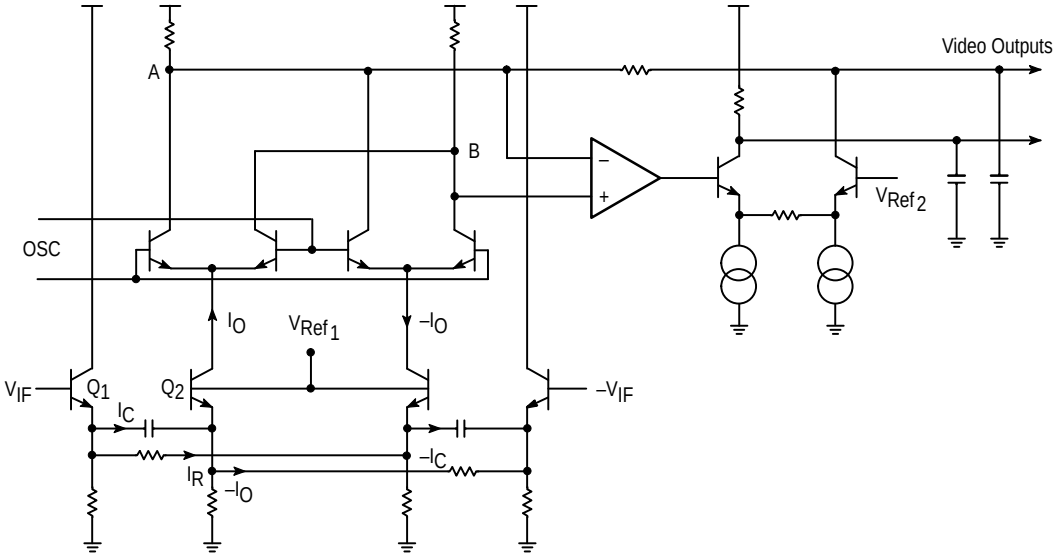
Video Demodulator and Amplifier

The video demodulator and amplifier are shown in simplified form in Figure 9. The 90° phase shift of the signal is obtained by replacing the usual emitter resistors in the differential amplifier feeding the demodulator by capacitors. The output currents are 90° with respect to the input voltage over a wide range of frequencies and small phase errors, caused by transistor small signal emitter resistances, are corrected by the cross coupled resistors. This arrangement leads to a simpler design, the ability to adjust the demodulation angle, and lower distortion than is normal at the IF amplifier/demodulator interface. The dynamic emitter resistances are now in quadrature with the capacitive reactance and therefore contribute very little to the resultant output. Although the current outputs of the demodulator are in antiphase, the voltages at A and B are forced by the feedback loop to be in phase. Level shifting from the top supply to the bottom rail is within the feedback loop, and RF components are filtered internally. The advantages of this configuration are improved linearity with lower sound/chroma beat products; differential to single–ended conversion of the demodulator output; accurate control of the peak white video level, and low levels of high frequencies at the video outputs. The positive video output is intended to be used as the actual video and is acted upon by a white spot noise inverter. This effectively removes the “whiter than white” noise produced by a true synchronous demodulator and prevents the CRT from being overdriven and defocused. The negative video output is not acted upon by a white spot noise inverter and, of course, the noise output from a synchronous detector does not contain a dc component. Hence, this drive should be used as the sync separator drive because a simple preseparator low pass noise filter will give optimum sync performance.

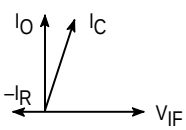
Sound Output

A separate quadrature demodulator is used to recover the intercarrier sound signal. The IF signal and VCO have a 90° phase relationship at the detector’s input ports instead of the 0° required at the video demodulator. This ensures that the only video components appearing at the output will be high frequency components. A consequence of the quadrature relationship of the demodulator signals is that the low distortion capacitive input stage used in the video demodulator cannot be used. Instead, a new linear wideband differential stage has been designed where the distortion in the output currents, caused by emitter/base diode nonlinearities, is cancelled by the current through the R_2 resistor. A reduction in THD of 20 dB is obtained, compared to a simple differential amplifier even at 120 MHz. The combination of a linear input stage and a post demodulation feedback amplifier results in quadrature intercarrier sound demodulation having lower video interference than sound recovered in the normal way from the video channel.

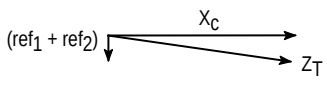
Figure 9. Video Demodulator and Amplifier



Vector Diagram

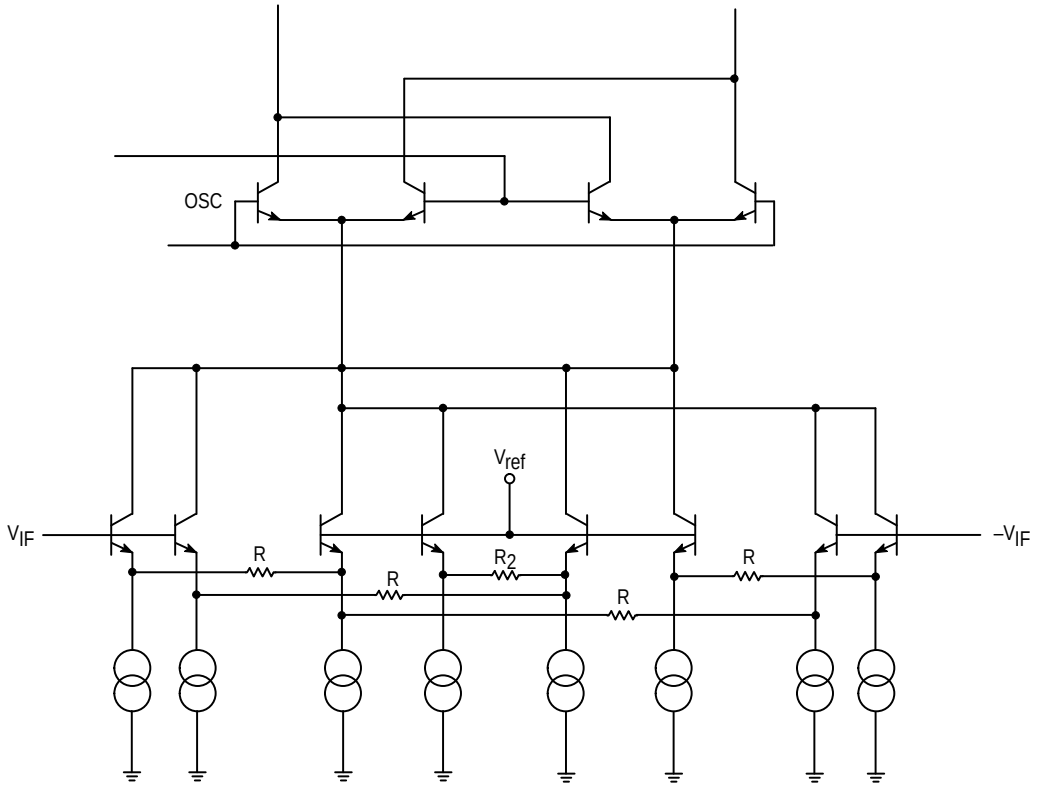


Impedance Diagram



$$Z_T = \sqrt{X_C^2 + (ref_1 + ref_2)^2}$$

Figure 10. Sound Demodulator



AFT

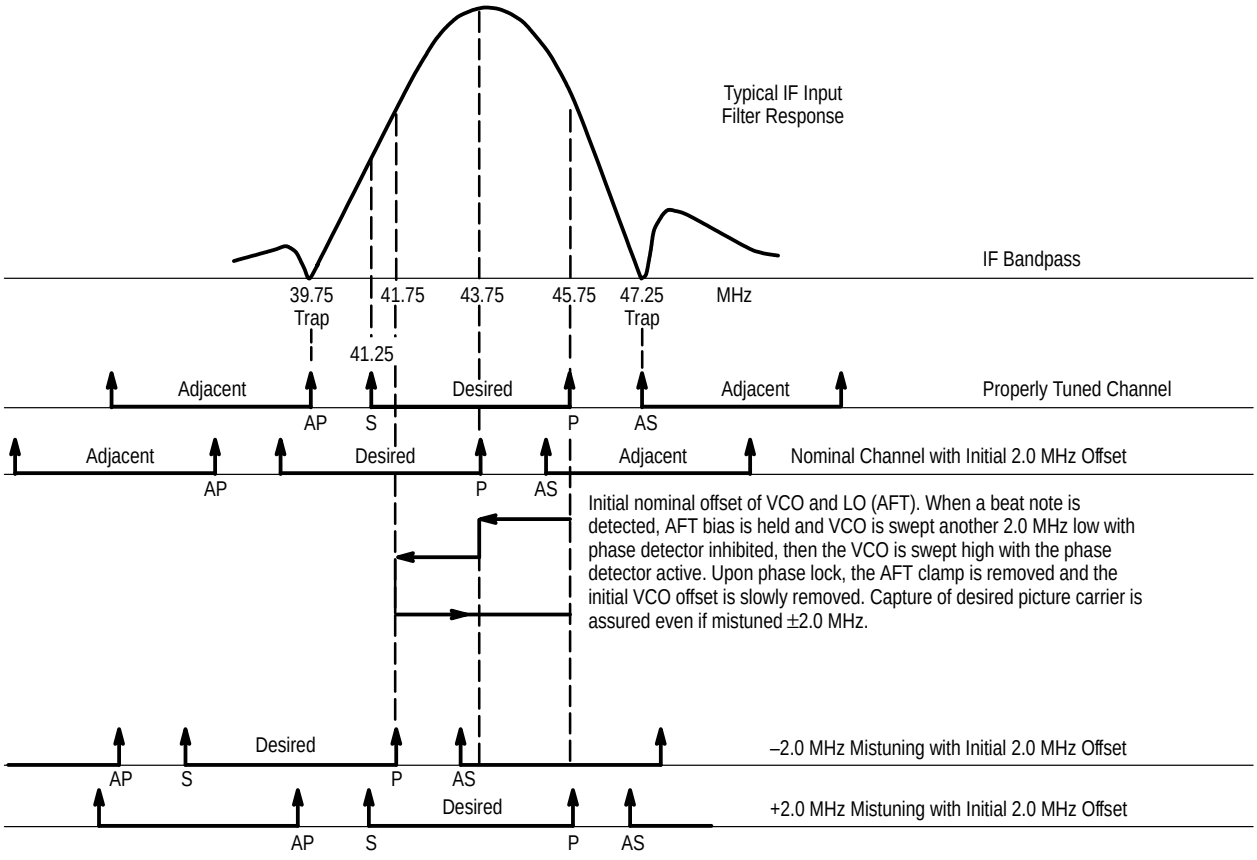
The AFT portion of the circuit is the most unconventional in form. Essentially, AFT is derived by amplifying the error signal and applying this to the local oscillator in the tuner, thus eliminating a coil and a potential IF instability problem. After acquisition (phase lock) when the circuit has reached its steady state condition, due to the much higher gain in the LO loop, the VCO will have moved a small amount (Δfv) from its nominal frequency, and almost all the original IF error (Δfe) will have been corrected by a change in the LO frequency (Δfl). In this way, provided the local VCO loop can initially be phase locked to the incoming IF signal, the VCO can be used as the frequency reference for the AFT system. It follows from the above, therefore, because the system is phase locked, that Δfe = (Δfl +Δfv). The combination of local VCO loop and the loop produced by feedback to the local oscillator forms a double–loop PLL. Analysis shows that overall system stability can be assured by treating the VCO as a stand alone PLL, provided the bandwidth is much wider than the LO loop. The VCO loop therefore is a low gain wideband loop which guarantees initial capture, while the LO loop is basically a high gain dc loop used to keep frequency and phase offsets to a minimum.

The AFT system is designed to acquire the vision carrier, without false locking to the sound or adjacent sound carriers, with an initial error of ±2.0 MHz being reduced to 10 kHz to 20 kHz when locked (U.S.A.). This contrasts with the discriminator type of AFT which has highly asymmetric lock characteristics (–2.0 MHz + 1.0 MHz), because of the effects of the IF filter, and large closed loop errors caused by limited loop gain (see Figure 3). To achieve this level of performance without encountering the normal AFT problems associated with high loop gain (large dc offsets, etc.), a novel approach has been taken to locking up the PLL. In the absence of an IF signal, the acquisition circuitry examines the state of the video (I) and sound (Q) demodulators and detects the lack of a signal. The filtered output of the lock detector then sits at approximately 2.7 V. Under these circumstances the LO drive is clamped to a reference voltage and an offset applied to the VCO. This is done in such a way that the IF signal (should a signal appear) and the VCO are sitting in the center of the IF filter passband. Therefore, even if the LO drifts high by as much as 2.0 MHz, the signal will not be significantly attenuated by the filter. On the arrival of a signal, beat notes appear at the outputs of the demodulators, the output of the lock detector goes low and a sweep generator is switched on. The generator immediately sweeps the VCO an additional –2.0 MHz from its out of lock mid–band nominal frequency. During this negative sweep, the PLL phase detector is switched off so phase lock cannot be obtained. The VCO is then swept positive from –2.0 MHz to +2.0 MHz of the nominal out of lock frequency with the phase detector switched on. The PLL will therefore lock to the first carrier it encounters. This in fact must be the vision carrier because the sound carrier is more than 2.0 MHz below the nominal frequency and the adjacent sound carrier is higher than the vision carrier. On achieving lock, the lock detector output goes high. When this happens, the AFT clamp is released, the VCO offset is slowly removed, the sweep generator is inhibited and the phase detector remains permanently enabled. With the AFT clamp removed, a large error voltage appears at the AFT output, driving the system back to the correct frequency. Since the LO loop is slow and the VCO loop is fast, the IF changes slowly and the VCO tracks it, maintaining phase lock until the final static conditions are reached. For large frequency errors during this period, the slew rate of the LO loop is increased but not to the extent where it would cause any VCO tracking problems. This technique allows the acquisition time of the circuit to be

considerably shortened while still using a larger than normal time constant in the LO loop. In this way, any possibility of phase modulating the LO with video is removed. Figure 11 illustrates the AFT system in action.

To accommodate all types of tuners the LOs, positive or negative LO drive can be selected externally by operation of the AFT switch. The AFT switch also has a third position which disconnects the drive to the tuner. Under this condition, the TV set can be tuned in the normal manner and so appears to have a conventional type of AFT. Other PLL systems cannot be tuned manually in this way, having an abrupt capture characteristic, and because of this, have not gained general acceptance.

Figure 11. The AFT System in Action



APPLICATIONS INFORMATION

Alignment

The alignment of the MC44301 is very simple and inexpensive compared to other IF amplifier circuits, especially those using PLL demodulators. With a CW input signal of correct picture carrier frequency, the LO side of the 8.2 kΩ resistor in series with the loop is connected to a dc supply of approximately 2.5 V. The dc supply is adjusted until the output of the tuner is 45.75 MHz. The VCO coil is adjusted until lock is obtained and the voltage across the 8.2 kΩ resistor is zero. The dc supply is then removed (refer to Figure 12).

Component Selection

The IF input assumes 75 Ω output from the tuner. A SAW bandpass filter is used which has a low insertion loss while maintaining good triple transit response. Recommended sources for this filter include Murata 80Z series, SAF45MA80Z and Siemens M1963, which are packaged in a 5–pin SIP plastic package. Pinouts are identical, but the interface matching to IF will need to be modified for best performance. The evaluation PC board is laid out to accept either the SIP or a more expensive metal can filter.

The VCO coil is a bifiliar wound, center–tapped, 10 mm size shielded inductor, Figure 17 shows the construction details. Recommended sources for the (45.75 MHz IF) coil are TOKO TKANAS–T1390ADP, and Coilcraft M1300–A. For a higher IF frequency, the coil inductance must be decreased. In this case, the coil may be a custom having windings similar to the specified coil in Figure 17. Note that this coil has the same number of turns on both sides of the center–tap.

Evaluation PC Board

The evaluation PC board schematic in Figure 13 and the layout in Figures 14, 15, and 16 show a double sided board which is designed to accommodate additional external components and circuitry intended for use in 12 V systems and various tuner systems and applications. An optional sync separator circuit is recommended where a flyback pulse is not available, such as in set–top converters. Other optional circuitry is shown which helps to further improve the sound performance through additional quadrature and phase corrections. This is shown in the schematic for the Rev B evaluation PC board (Figure 13).

PCB Layout Considerations

The typical 5.0 V application circuit shown in Figure 6 uses a single sided PC board with very few external components. To maintain optimum performance, the placement and interconnection of some components such as the SAW filter and VCO tank are critical. These components are placed close to the IC to enable short trace lengths which are symmetrically placed and equal in length to avoid differential offsets and noise. In a single sided PC board layout the ground should flow around the device, and around the V_{CC} trace and other circuit traces as a continuous “sea of ground”. Since the IF is very stable and immune to radiation, the device can be mounted on a single sided PC board without the customary and necessary shielding required in other IF systems. **However, do not use prototype and wire wrap construction techniques.**

Figure 12. Alignment Configuration

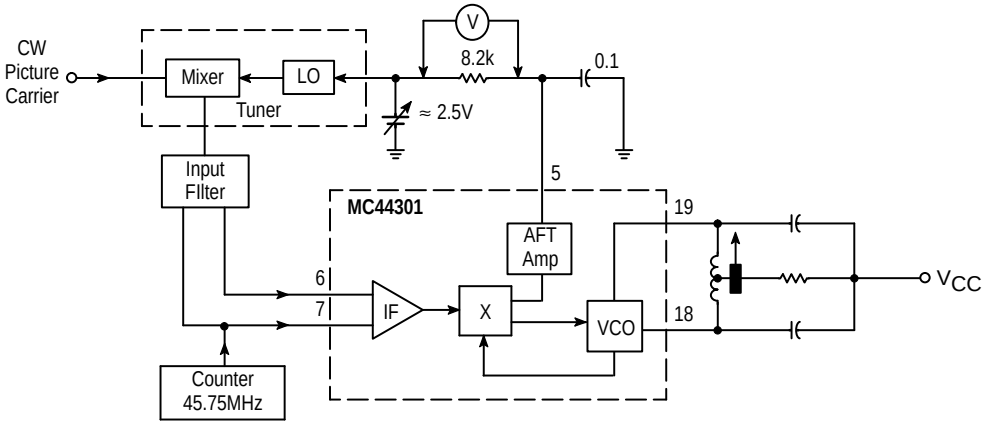
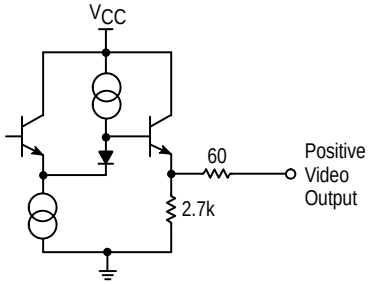
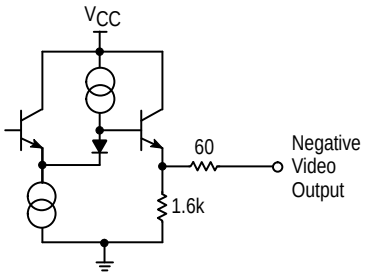
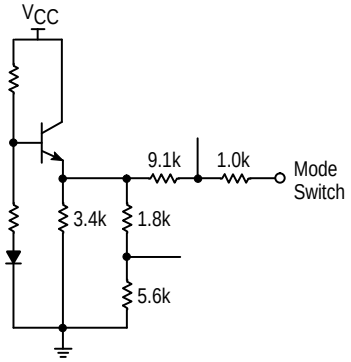
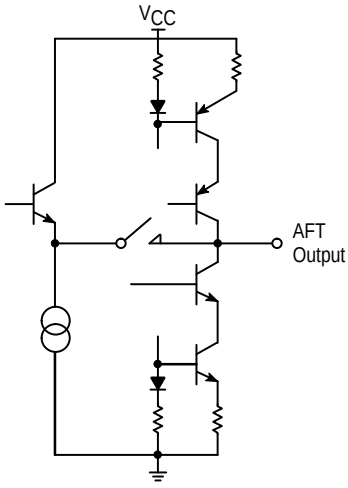
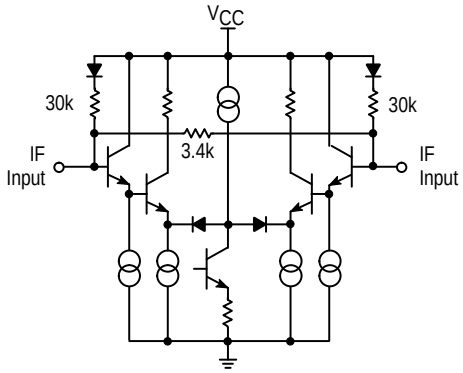
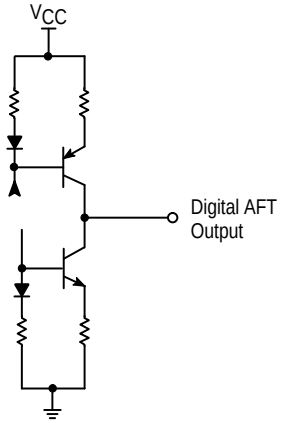
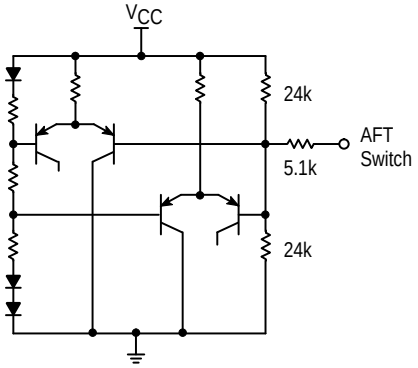
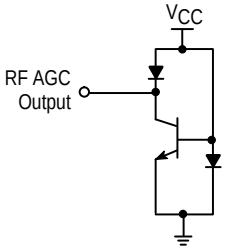


Table 2. Pin Function Desription

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
1, 21, 23	1, 4, 11, 18, 24, 25, 26		**No Connection.**
2	2		**Positive Video Output With White Spot Noise Inversion** In the evaluation PCB a discrete external buffer (2N4402) is used to provide interface – this is not needed in the actual application.
3	3		**Negative Video Output Without White Spot Noise Inversion** Intended for sync separator use.
4	5		**Mode Switch** Selects positive or negative modulation. The pin is open for negative going video and grounded for positive going video.
5	6		**AFT Output** High output impedance push–pull current drive. Intended to give high AFT loop gain when used with high load impedances (i.e. direct connection to the tuner varactor diode). Drive is greatly increased for large frequency error to minimize pull–in time and clamped when PLL is not locked. External circuitry is provided in the evaluation PCB to allow adjustment of the drive to the tuner. This will not be needed in the actual application where the tuner is compatible with the IC. Polarity is controlled externally by the AFT switch.

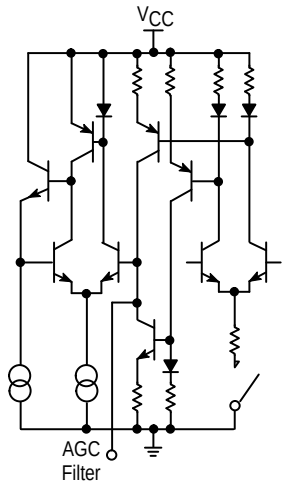
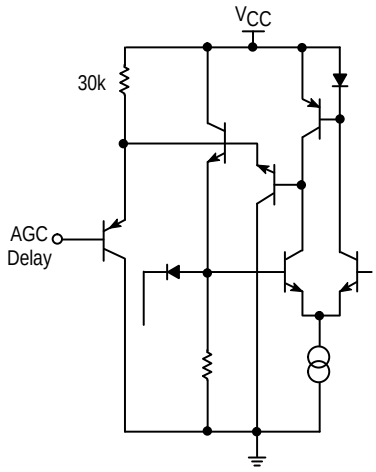
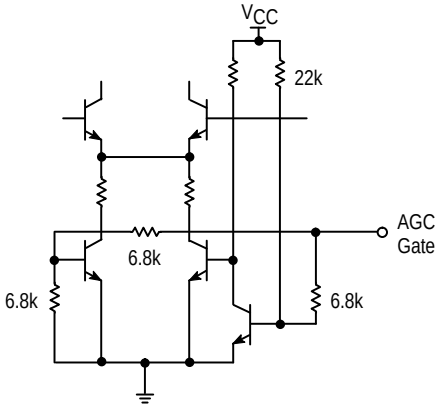
(continued)

Table 2. Pin Function Desription

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
6, 7	7, 8		**IF Inputs** Input leads should be kept short and symmetrical to avoid instability problems. The performance of the IF is greatly dependent upon the characteristics of the IF filter and upon the proper matching of the filter to the IF input. Refer to the evaluation circuit for recommended filters.
8	9		**Digital AFT Output** This is a tristate output having a ±300 kHz dead zone. Polarity is controlled externally by the AFT switch.
9	10		**AFT Switch** AFT is designed to accommodate all types of tuners and LOs. On the evaluation PCB, a jumper matrix provides three positions: 1) AFT switch pin to V_{CC} for positive LO drive, 2) AFT switch pin to ground for negative LO drive and 3) AFT switch pin to open which disconnects drive to the tuner.
10	12		**RF AGC Output** The output is designed for a reverse AGC tuner and will only sink about 0.8 mA maximum. At 5.0 Vdc V_{CC}, the maximum voltage on this pin is 5.8 Vdc, due to an internal clamping diode. In an application in which the tuner does not have a pull–up resistor, one must be added to the external circuit. With a tuner supply voltage at 8.0 Vdc, the load resistor should be at least 10 kΩ or greater.

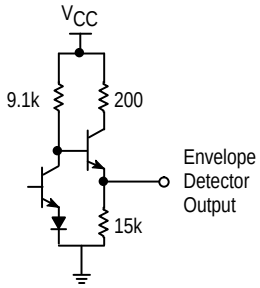
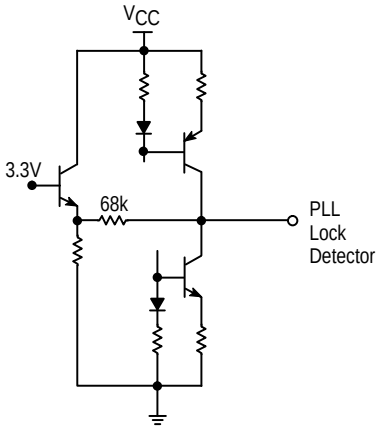
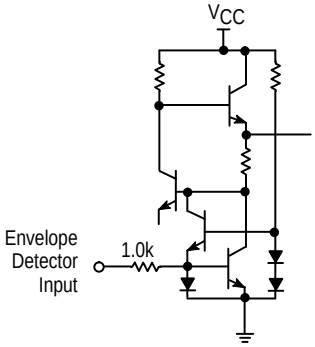
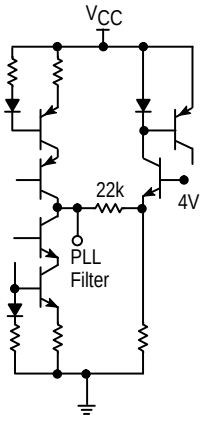
(continued)

Table 2. Pin Function Desription

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
11	13		**AGC Filter, AGC Control Voltage** Voltage level at this pin indicates AGC action by three gain control ranges. Increasing voltage at this pin gain reduces the tuner or IF. 0 Vdc to 2.5 Vdc is the IF initial control range, 2.5 Vdc to 4.0 Vdc is the nominal tuner RF control range, 4.0 Vdc to 5.0 Vdc further gain reduces the IF for very large signal level at the antenna.
12	14		**RF Tuner AGC Delay Adjustment** Below the potential set at this pin, the IF AGC is active and the tuner AGC is non–active. Above the potential set the IF amplifier gain is held constant while the tuner is gain reduced. The tuner takeover point normally corresponds to a 1.0 mVrms to 2.0 mVrms signal into the antenna. Thus, as the input increases beyond this level, the tuner AGC will activate, clamping the input drive into the IF at the associated 1.0 mVrms to 2.0 mVrms antenna threshold. The external AGC adjust network shown in Figure 13 provides 2.0 Vdc ± 0.2 Vdc at the AGC Adjust pin. This network may be modified for the desired range and resolution.
13	15		**AGC & Lock Gating Input** A 300 μA current pulse is required at this pin to gate on the AGC and lock systems. In most TV applications where negative modulation is used, the flyback pulse can be used to gate the AGC through a resistor. In applications where flyback is not available, the gate pulse can be acquired via a sync separator from the video output at Pin 2. The circuit shown in Figure 13 insures that the gate will be acquired in the proper time and level from the sync pulse.

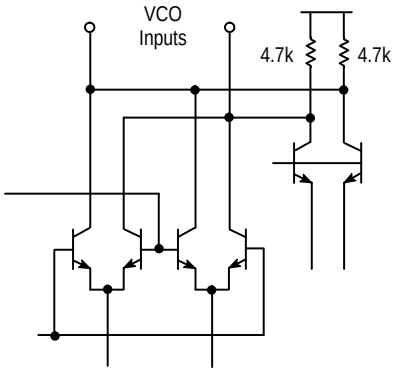
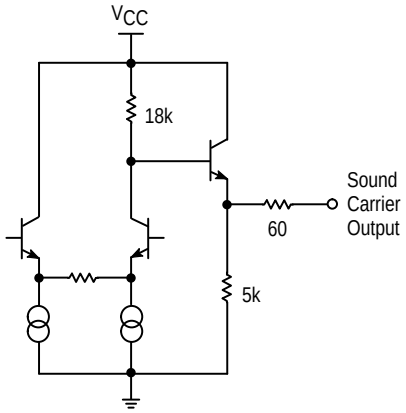
(continued)

Table 2. Pin Function Desription

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
14	16		**Envelope Detector Output** Detector for AM sound modulation (SECAM or descrambler signal).
15	17		**PLL Lock Detector** With 5.0 Vdc V_{CC}, lock is indicated by approximately 4.3 Vdc and zero signal is indicated by approximately 2.7 Vdc on this pin.
16	19		**Envelope Detector Input** AM sound subcarrier input.
17	20		**PLL Filter** The phase detector output after filtering produces a voltage which controls the frequency of the VCO. With 5.0 Vdc V_{CC}, there is approximately 3.2 Vdc present when VCO is locked and 3.1 Vdc when unlocked.

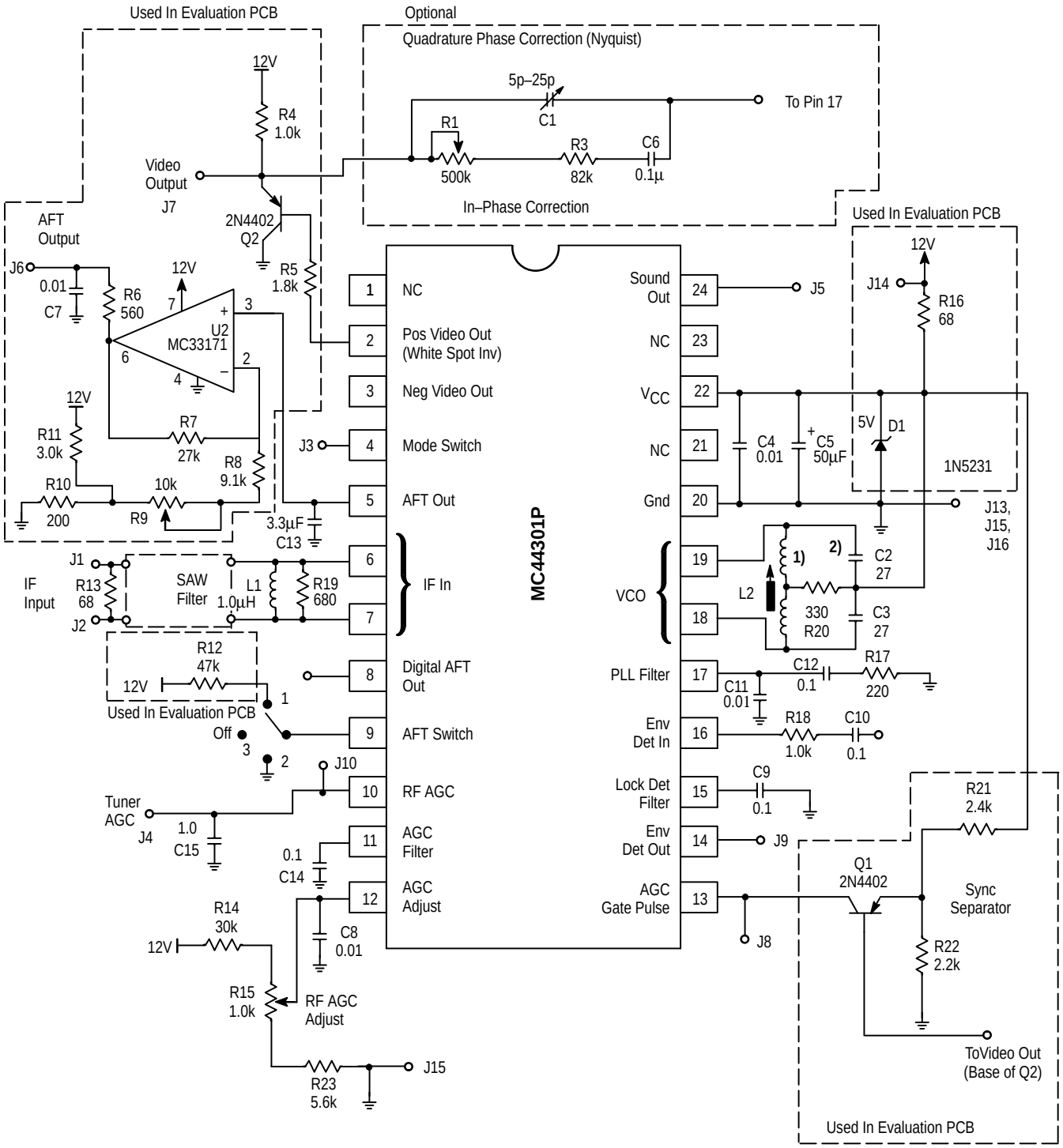
(continued)

Table 2. Pin Function Desription

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
18, 19	21, 22		**VCO Inputs** Care should be taken in layout by placing the VCO tank close to the IC pins with symmetrical traces to the shielded inductor. A center–tapped, bifiliar wound coil, previously defined, provides symmetrical tuning about the VCO frequency. The external VCO operates at half the IF frequency and is doubled on the IC chip.
20	23		**Supply Ground** Care should be taken to provide a continuous sea of ground or fill of the ground around the part, and traces in a single–sided PCB layout or a full ground plane on the component side of a double–sided layout.
22	27		**Supply Voltage (V_{CC})** Good RF decoupling must be provided close to this pin. At 25°C, maintain between 4.5 Vdc to 5.5 Vdc. At 0°C do not use less than 4.75 Vdc.
24	28		**Sound Carrier Output** Due to quadrature demodulation, the video components are suppressed at this output. However, with a vestigial sideband signal, high frequency video components will be present.

NOTE: Most pins on the IC have electrostatic protection diodes to V_{CC} and to ground. It is therefore *imperative* that no pin is taken below ground or above V_{CC} by more than one diode drop without current limiting.

Figure 13. MC44301P Universal Evaluation Circuit Schematic
Rev B – PCB



NOTES: 1. See Figure 17 for coil details.
2. Capacitors should be close tolerance, high Q components, such as silver mica – to insure dynamic frequency response and minimum bandwidth.

Figure 14. Component Placement and Silk Screen View

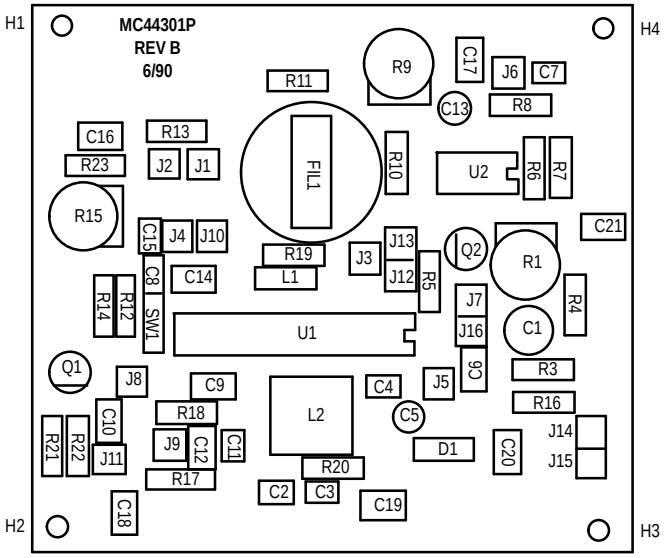


Figure 15. Component Side of PCB

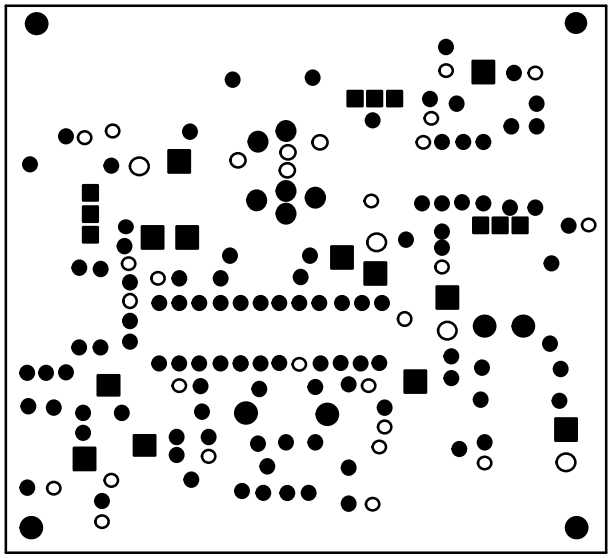
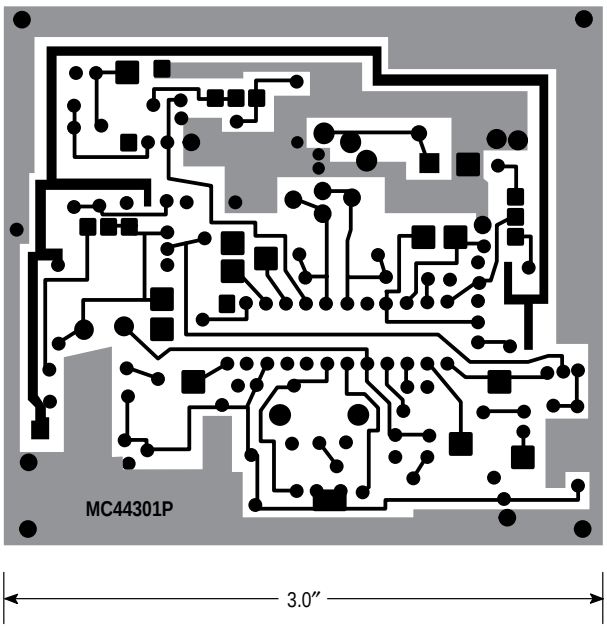


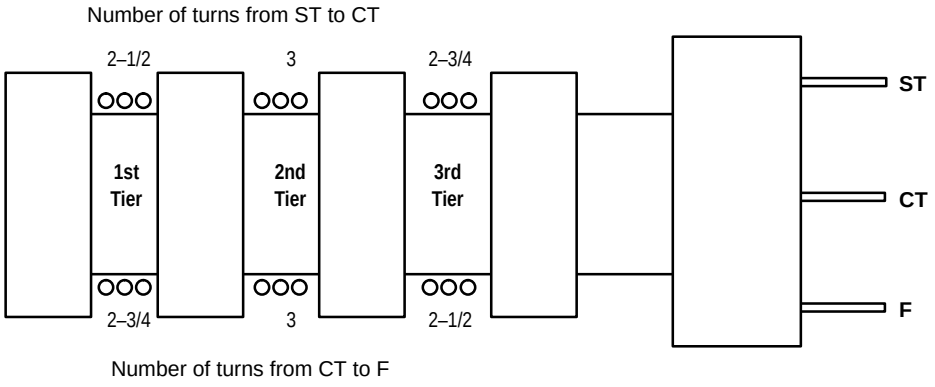
Figure 16. Circuit Side of PCB



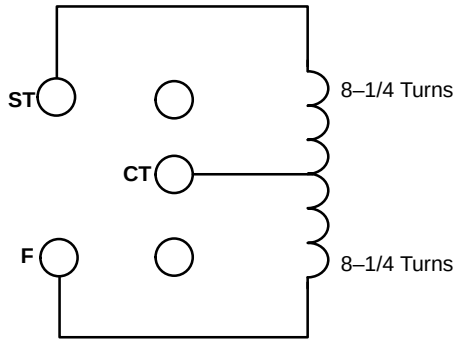
Winding Instructions

Use 38 AWG enameled wire. Start at “ST” pin, go to the top of the bobbin: wind 2–1/2 turns on the first tier; 3 turns on the second tier; 2–3/4 turns on the third tier, then go to the center tap “CT” pin. From the CT wind 2–3/4, 3 and 2–1/2 turns on the first, second and third tiers respectively, then finish the windings at the “F” pin. Wind the wire in the same direction, making sure it is wound tightly around the bobbin. The wire must be tinned to obtain the necesary solder connections. Application of solder directly to the enameled wire will remove the enamel and adequately tin it.

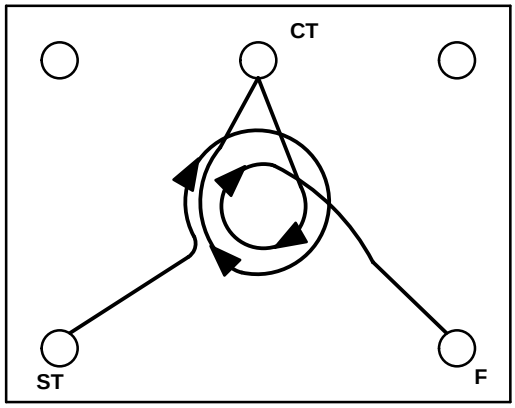
Figure 17. Winding Details for the VCO Coil



Bifiliar Wound 16–1/2 Turns



(Schematic)

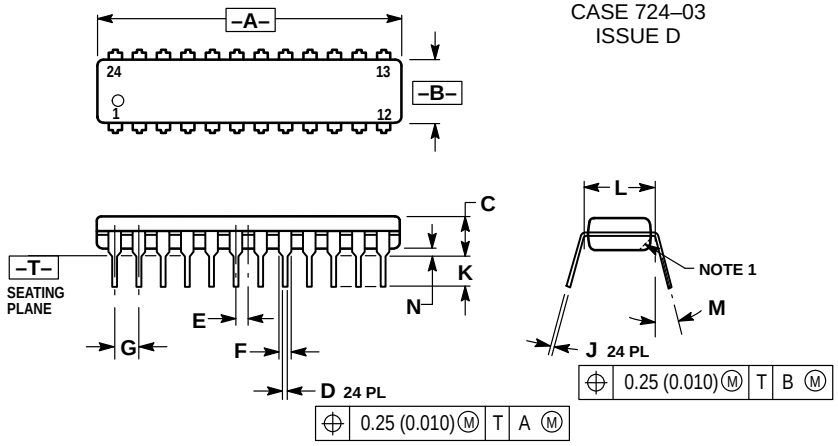


(Bottom View)

(TOKO Type 10 k Series or Coilcraft *Slot 10* Series Bobbin. Recommended sources for the coil are TOKO TKANAS–T1390ADP and the Coilcraft M1300–A)

OUTLINE DIMENSIONS

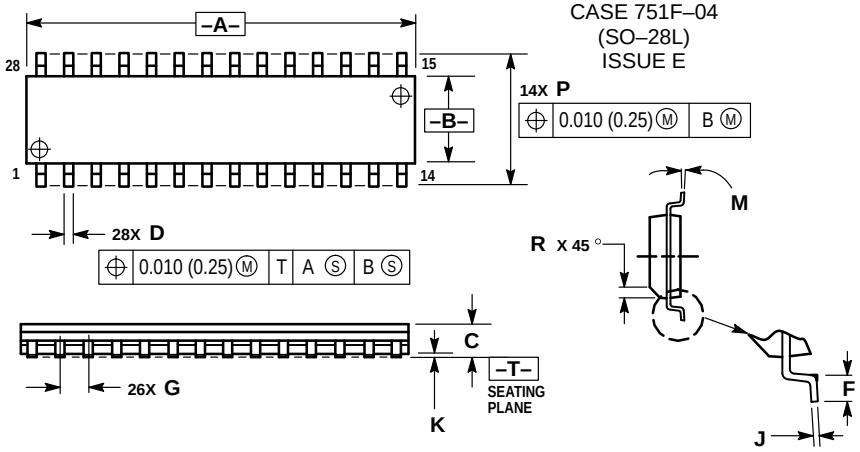
P SUFFIX
PLASTIC PACKAGE
CASE 724–03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC PACKAGE
CASE 751F–04
(SO–28L)
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.01	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

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