Order this document by MC44145/D

MOTOROLA

MC44145

Product Preview

Sync Separator/ Pixel Clock Generator

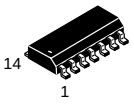
The MC44145 Pixel Clock Generator is a component of the MC44000 family, and a spin–off of the PLL2 function of the MC44011, Digital Multistandard Video Processor.

The MC44145 contains a sync separator with horizontal and vertical outputs, and clock generation circuitry for the digitalization of any video signal along with the necessary circuitry for clock generation, such as a phase comparator and a divide–by–2 to provide a 50% duty cycle.

The MC44145 is available in a 14 pin package and is fabricated using Motorola's high density, low voltage, bipolar MOSAIC 1.5® process.

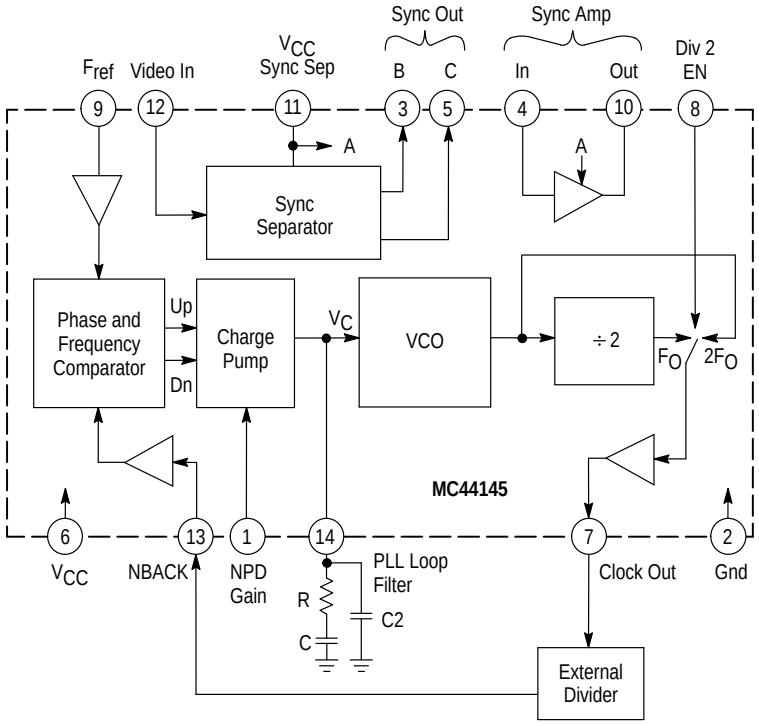
SYNC SEPARATOR/ PIXEL CLOCK GENERATOR

SEMICONDUCTOR TECHNICAL DATA

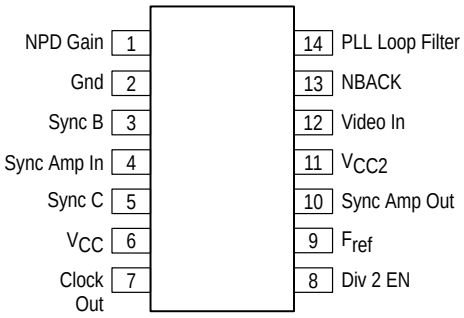


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

Representative Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44145D	T_A = 0° to +70°C	SO–14

CIRCUIT DESCRIPTION

Composite Sync Separator

The composite sync separation section comprises two blocks, a sync slicer and a sync amplifier, that can be used to extract the vertical sync information from a video signal.

The sync separator is an adaptive slicer in which the video signal is slightly integrated and then sliced at a ratio of 4.7 to 64 which corresponds to the sync to horizontal ratio. Two outputs are given, one of high impedance and the other low impedance.

A slicing sync inverting amplifier is also on–chip, allowing one output to be used for composite sync and the other output to be integrated and then sliced using the slicing amplifier to extract the vertical sync information.

Clock Generation

The clock generation is made up of a wide ranging emitter–coupled VCO followed by a switchable ÷ 2 to provide a 50% duty cycle wherever required, or twice the set frequency if an external divider is used. The clock generation is a PLL subsection. Its function is the generation of a high frequency, line–locked clock that is used for video sampling and digitizing.

The clock is output by a LSTTL–like buffer which has a limited drive capability of two LSTTL loads.

The VCO is driven from a charge pump circuit, with selectable current. The charge pump is driven from the phase comparator. The phase comparator is a type IV “phase and frequency comparator” sequential circuit.

The clock generator, the heart of a PLL, is to be closed by means of an external divider, thus setting the synthesized frequency. This divider could be implemented in discrete logic or be a part of an ASIC subsystem.

Phase and Frequency Comparator

The phase comparator is fed from two input buffers (F_{ref}) which expects a reference frequency at line rate and that is rising–edge sensitive, and NBACK which comes from the external divider and is falling–edge sensitive.

Charge pump current and output divider action are controlled by applying suitable voltage on the appropriate pins, respectively, NPD Gain and Div 2 EN.

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	NPD Gain	This pin sets the gain of the phase frequency detector by changing the current of the charge pump output (40 μA or 80 μA). Low current with this pin > 2.0 V, high current for < 0.5 V.
2	Ground	Ground connection common to the PLL and sync separator sections.
3	Sync B	High impedance sync output.
4	Sync Amp In	Sync amplifier input.
5	Sync C	Low impedance sync output.
6	V_{CC}	Power connection to the PLL section.
7	Clock Out	VCO clock output. Capable of limited LSTTL drive. It should not be used to drive high capacitive loads, such as long PCB traces or coaxial lines.
8	Div 2 EN	The divider is switched–in with this pin > 2.0 V; switched–out for < 0.5 V.
9	F_{ref}	Reference frequency input to the phase and frequency comparator. Typically, this will be a 15625 (15475) Hz signal. It is rising–edge sensitive. Due to the nature of the phase and frequency comparator, no missing pulse is tolerable on this input. In a typical setup, this signal can be provided by the MC44011.
10	Sync Amp Out	Sync amplifier output.
11	V_{CC2}	Power connection to the sync separator and amplifier.
12	Video In	Video signal input to the sync separator.
13	NBACK	Fed by the external clock divider. Sets the multiplication ratio of the loop in multiples of the F_{ref} frequency. Negative–edge sensitive.
14	PLL Loop Filter	Values for the loop filter components should be the same as for the MC44011.

NOTE: The two V_{CC} pins are not independent, as they are internally in relationship by means of the input protection diodes. They must always be connected to a suitable V_{CC} line.

CIRCUIT OPERATION

Composite Sync Separator

The sync separator is an adaptive slicer. It will output “raw” sync data. Two outputs are given, thus allowing one output to be used for composite sync and the other output to be integrated and then sliced using the inverting slicing amplifier provided. As the input of the slicing amplifier is external, the amplifier may be driven from either sync output, although normally the high output impedance (Sync B) would be recommended.

The positive video input signal required is nominally 1.0 V sync–to–white, but the circuit supports signals above and below this level and also is resistant to a degree of reflections on the signal. Coupling to the sync separator may be achieved by a simple capacitor of 100 nF, but better results may be obtained with a higher value in series with a resistance of 1.0 kΩ.

Clock Generator

The system is best put to use in a dual loop configuration. The first loop locks to line frequency by means of a type I phase detector (multiplier type) which is insensitive to missing pulses. This PLL is then followed by a second loop using the MC44145, performing frequency multiplication. The phase comparator of the MC44145 is frequency and phase sensitive. It is a type IV (sequential type) phase detector, which does not tolerate missing pulses. The dual loop structure makes up a noise insensitive frequency (and phase) locked loop.

The phase and frequency comparator provides two logical outputs, mutually exclusive – up or down – that are used to source or sink current to and from the loop filter. This current can be user–selected to be 40 μA or 80 μA (typical), thus providing some degree of loop gain control.

The VCO is an emitter–coupled multivibrator type, with an on–chip timing capacitor, and has been designed for low phase noise.

The divide–by–2 is included at the output of the VCO, thus allowing for a precise 50% duty cycle, hence the VCO is operating at twice the required frequency. The divider can be bypassed, bringing the VCO output directly to the output buffer.

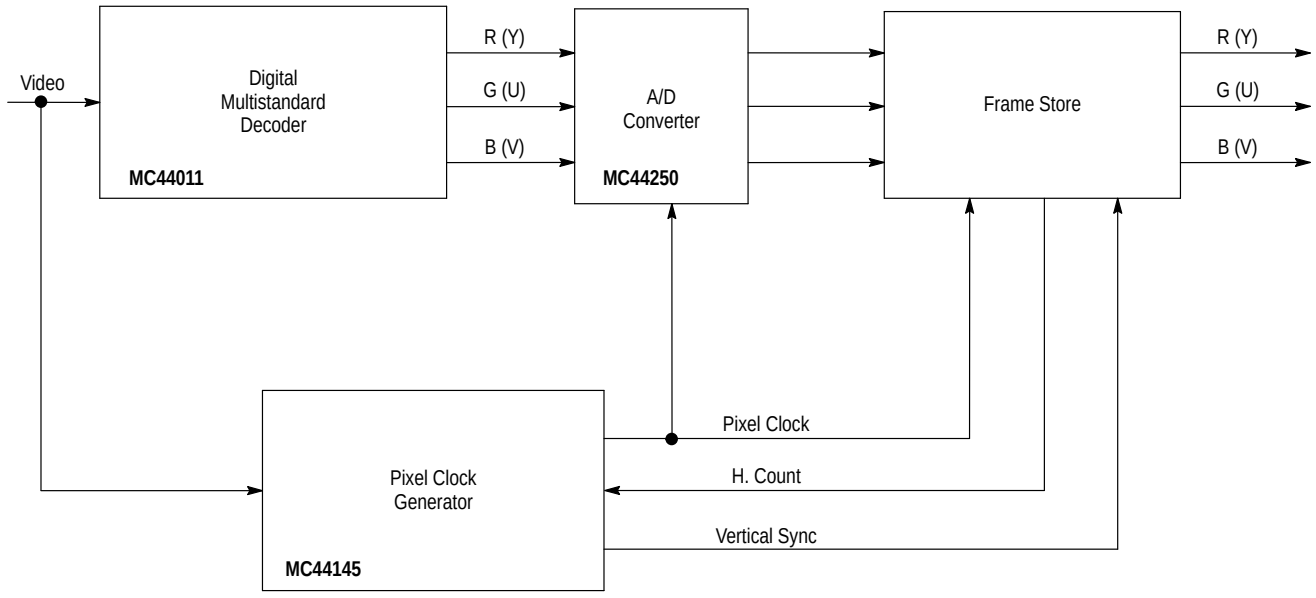
The external divider must provide a feedback pulse to close the loop. The falling edge of this pulse will be aligned (when the loop is in lock) with the rising edge of the pulse applied to the F_{ref} input. Operation of the phase comparator is insensitive to the duty cycle of both its inputs. The feedback pulse should have a minimum width of 500 ns. This can be guaranteed if it has a length of at least 16 output clock cycles (highest output frequency with the divider disabled).

APPLICATION INFORMATION

Analog video signals out of the MC44011 are sampled and converted to 8–bit digital in the A/D converter (MC44250) by means of the pixel clock generator, provided by the MC44145 (see Figure 1).

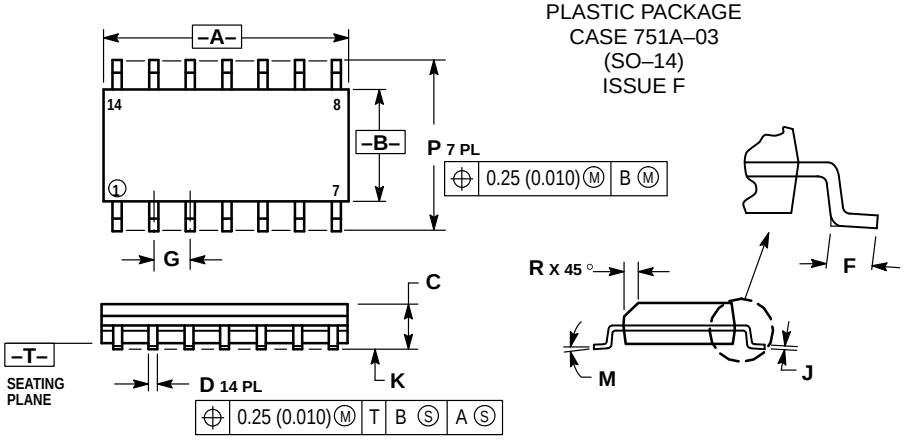
The frame store contains the memory, the necessary logic for the memory addressing, as well as the counter to set the frequency multiplication ratio of the line–locked clock generator (H. Count).

Figure 1. Application Block Diagram



OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298