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MOTOROLA

# MC44011

*Advance Information*

# Bus Controlled Multistandard Video Processor

**BUS CONTROLLED MULTISTANDARD VIDEO PROCESSOR**

**SEMICONDUCTOR TECHNICAL DATA**

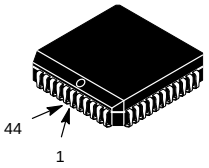
The Motorola MC44011, a member of the MC44000 Chroma 4 family, is designed to provide RGB or YUV outputs from a variety of inputs. The inputs can be composite video (two inputs), S–VHS, RGB, and color difference (R–Y, B–Y). The composite video can be PAL and/or NTSC as the MC44011 is capable of decoding both systems. Additionally, R–Y and B–Y outputs and inputs are provided for use with a delay line where needed. Sync separators are provided at all video inputs.

In addition, the MC44011 provides a sampling clock output for use by a subsequent triple A/D converter system which digitizes the RGB/YUV outputs. The sampling clock (6.0 to 40 MHz) is phase–locked to the horizontal frequency.

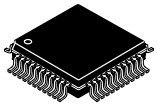
Additional outputs include composite sync, vertical sync, field identification, luma, burst gate, and horizontal frequency.

Control of the MC44011, and reading of status flags, is via an $I^2C$ bus.

- Accepts NTSC and PAL Composite Video, S–VHS, RGB, and R–Y, B–Y
- Includes Luma and Chroma Filters, Luma Delay Lines, and Sound Traps
- Digitally Controlled via $I^2C$ Bus
- R–Y, B–Y Inputs for Alternate Signal Source
- Line–Locked Sampling Clock for A/D Converters
- Burst Gate, Composite Sync, Vertical Sync and Field Identification Outputs
- RGB/YUV Outputs can provide 3.0 $V_{pp}$ for A/D Inputs
- Overlay Capability
- Single Power Supply: + 5.0 V, ± 5%, 550 mW (Typical)
- 44 Pin PLCC and QFP Packages




**FN SUFFIX**
PLASTIC PACKAGE
CASE 777
(PLCC)

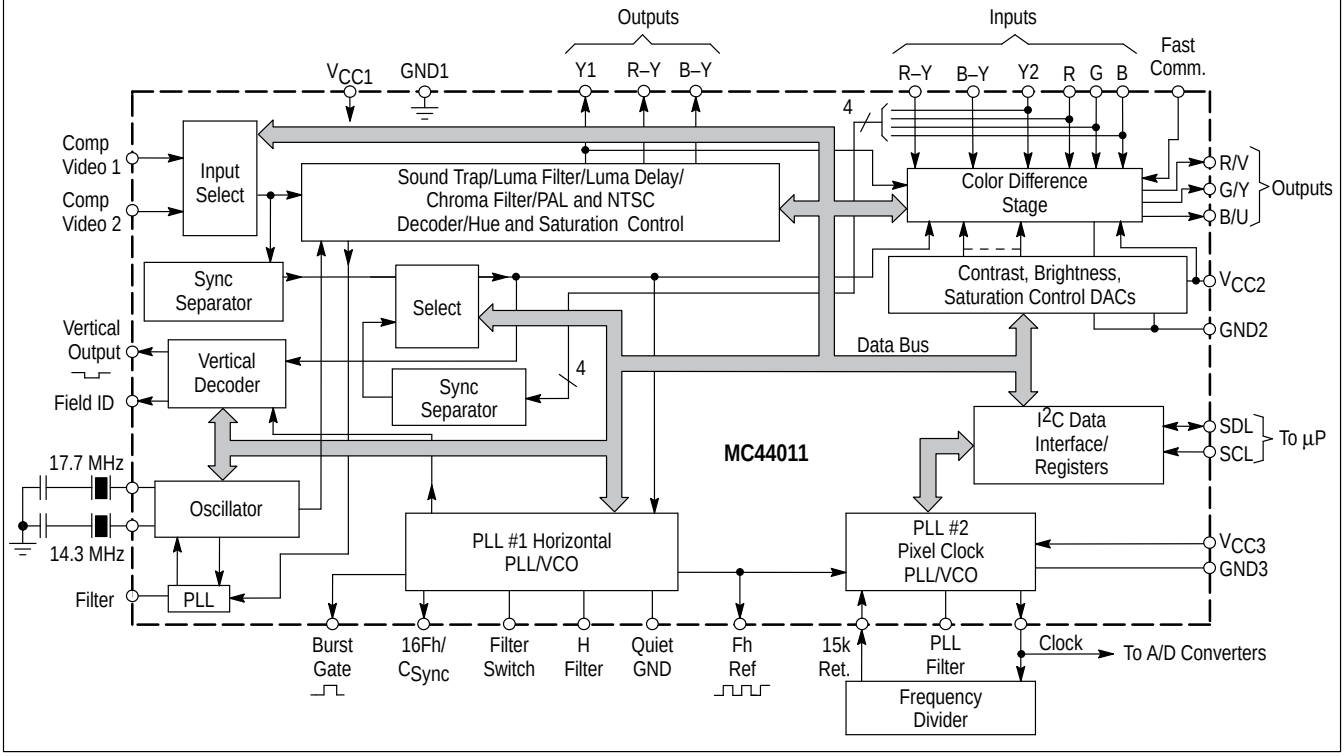


**FB SUFFIX**
PLASTIC PACKAGE
CASE 824E
(QFP)

**ORDERING INFORMATION**

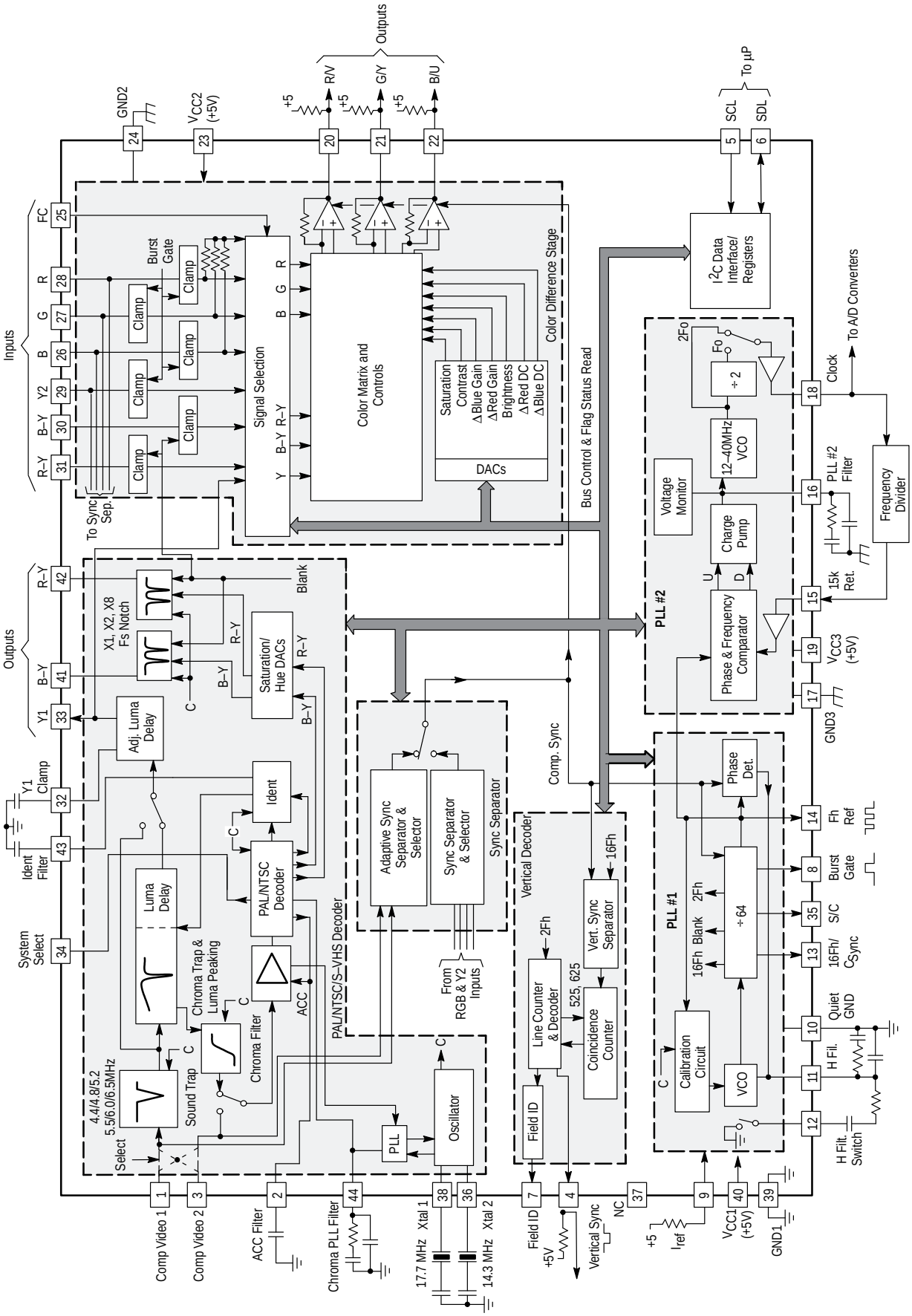
| Device | Operating Temperature Range | Package |
|---|---|---|
| MC44011FN | $T_A$ = 0° to +70°C | PLCC–44 |
| MC44011FB | | QFP |

**Representative Block Diagram**




This document contains information on a new product. Specifications and information herein are subject to change without notice.

**Figure 1. Representative Block Diagram**



**ELECTRICAL CHARACTERISTICS** (The tested electrical characteristics are based on the conditions shown in Table 1 and 2. Composite Video input signal = 1.0 $V_{pp}$, composed of: 0.7 $V_{pp}$ Black–to–White; 0.3 $V_{pp}$ Sync–to–Black; 0.3 $V_{pp}$ Color Burst. $V_{CC1} = V_{CC2} = V_{CC3} = +5.0$ V, $I_{ref} = 32$ µA (Pin 9), unless otherwise noted.)

**Table 1. Control Bit Test Settings**

| Control Bit | Name | Value | Function |
|---|---|---|---|
| $77–7 | S–VHS–Y | 0 | Composite Video input selected. |
| $77–6 | S–VHS–C | 0 | Composite Video input selected. |
| $77–5 | FSI | 0 | 50 Hz Field Rate selected. |
| $77–4 | $\overline{\text{L2 GATE}}$ | 0 | PLL #2 Gating enabled. |
| $77–3 | $\overline{\text{BLCP}}$ | 0 | Clamp Pulse Gating enabled. |
| $77–2 | $\overline{\text{L1 GATE}}$ | 0 | Vertical Gating enabled. |
| $77–1, 0 | CB1, CA1 | 1,1 | Vertical section Auto–Countdown mode |
| $78–7 | 36/68 µs | 0 | Time from beginning of Line 4 to Vertical Sync is 36 µs. |
| $78–6 | CalKill | 0 | Horizontal Calibration Loop enabled. |
| $79–7, 6 | HI, VI | 1,1 | Normal |
| $7A–7 | Xtal | → | 0 = 17.7 MHz crystal selected, 1 = 14.3 MHz crystal selected. |
| $7A–6 | SSD | 0 | Normal |
| $7B–7, 6 | T1, T2 | 1,1 | Sound Trap Notch filter set to 5.5 MHz (with 17.7 MHz crystal). |
| $7C–7 | SSC | 0 | Permits PAL and NTSC selection. |
| $7C–6, $7D–6 | SSA, SSB | → | 0, 1 = PAL decoding, 1,0 = NTSC decoding |
| $7D–7, $7E–7, 6 | P1, P3, P2 | 1, 1, 1 | Sets Luma Peaking at 0 dB. |
| $7F–7, 6, $80–6 | D3, D1, D2 | 0, 0, 0 | Set Luma Delay to minimum |
| $80–7 | $\overline{\text{RGB EN}}$ | 0 | Fast Commutate input can enable RGB inputs. |
| $81–7 | Y2 EN | 0 | Y2 input (Pin 29) deselected |
| $81–6 | Y1 EN | 1 | Y1 luma path from PAL/NTSC decoder selected. |
| $82–7 | YUV EN | 0 | RGB output mode selected |
| $82–6 | YX EN | 0 | Disable luma matrix from RGB inputs. |
| $83–7 | L2 Gain | 0 | Set PLL #2 Phase/Frequency detector gain high. |
| $83–6 | L1 Gain | 1 | Set PLL #1 Phase Detector gain high. |
| $84–7 | H Switch | 0 | Set Horizontal Phase Detector filter switch open. |
| $84–6 | 525/625 | → | 0= 625 lines (PAL), 1 = 525 lines (NTSC) |
| $85–7 | $F_{osc} \div 2$ | 0 | Select direct VCO output from PLL #2. |
| $85–6 | $C_{Sync}$ | 0 | 16 Fh output selected at Pin 13. |
| $86–7 | $V_{in}$ Sync | 1 | Composite Video inputs (Pin 1 or 3) Sync Source selected. |
| $86–6 | H EN | 0 | Enabled Horizontal Timebase. |
| $87–7 | Y2 Sync | 0 | Y2 sync source not selected. |
| $88–7 | V2/V1 | 1 | Select Video 1 input (Pin 1). |
| $88–6 | RGB Sync | 0 | RGB inputs Sync Source not selected. |

**Table 2. DAC Test Settings**

| DAC | Value | Function | DAC | Value | Function |
|---|---|---|---|---|---|
| $78 | 32 | R–Y/B–Y Gain | $82 | 32 | Red Contrast Trim |
| $79 | 32 | Sub Carrier Phase | $83 | 32 | Blue Brightness Trim |
| $7D | 00 | Blue Output DC Bias | $84 | 32 | Main Brightness |
| $7E | 00 | Red Output DC Bias | $85 | 32 | Red Brightness Trim |
| $7F | 63 | Pixel Clock VCO Gain | $86 | 32 | Saturation (Color Diff.) |
| $80 | 32 | Blue Contrast Trim | $87 | 16 | Saturation (Decoder) |
| $81 | 32 | Main Contrast | $88 | 32 | Hue |

Currents out of a pin are designated –, and those into a pin are designated +.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC1}$<br>$V_{CC2}$<br>$V_{CC3}$ | – 0.5 to + 6.0<br>– 0.5 to + 6.0<br>– 0.5 to + 6.0 | Vdc |
| Power Supply Difference (Between any two $V_{CC}$ pins) | | ± 0.5 | Vdc |
| Input Voltage: Video 1, 2, SCL, SDL<br>15 kHz Return<br>R–Y, B–Y, Y2, RGB, FC | $V_{in}$ | – 0.5, $V_{CC1}$ + 0.5<br>– 0.5, $V_{CC3}$ + 0.5<br>– 0.5, $V_{CC2}$ + 0.5 | Vdc |
| Junction Temperature (Storage and Operating) | $T_J$ | – 65 to +150 | °C |

Devices should not be operated at these limits. The “Recommended Operating Conditions” table provides for actual device operation.

## RECOMMENDED OPERATING CONDITIONS

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC1, 2, 3}$ | + 4.75 | + 5.0 | + 5.25 | Vdc |
| Power Supply Difference (Between any two $V_{CC}$ pins) | $\Delta V_{CC}$ | – 0.5 | 0 | + 0.5 | Vdc |
| Input Voltage: Video 1, 2 (Sync–White) | $V_{in}$ | 0.7 | 1.0 | 1.4 | $V_{pp}$ |
| Chroma (S–VHS Mode) | | – | – | 1.2 | |
| Y2 | | 0.7 | 1.0 | 1.4 | |
| RGB | | 0.5 | 0.7 | 1.0 | |
| R–Y, B–Y (Pins 30, 31) | | 0 | – | 1.8 | |
| 15 kHz Return | | 0 | – | $V_{CC3}$ | Vdc |
| SCL, SDL | | 0 | – | $V_{CC1}$ | |
| FC | | 0 | – | $V_{CC2}$ | |
| Burst Signal | | 30 | 280 | 560 | mVpp |
| Sync Amplitude | | 60 | 300 | $V_{CC1}$ | mVpp |
| Output Load Impedance to Ground: RGB (Pull–up = 390 Ω) | $RL_{RGB}$ | 1.0 | – | ∞ | kΩ |
| B–Y, R–Y | $RL_{CD}$ | 10 | – | ∞ | |
| Y1 | $RL_{Y1}$ | 1.0 | – | ∞ | |
| Pull–up Resistance at Vertical Sync (Pin 4) | $R_{VS}$ | 1.0 | 10 | – | kΩ |
| Source Impedance: Video 1, 2 | | 0 | – | 1.0 | kΩ |
| Pins 26 to 31 | | 0 | – | 1.0 | |
| Pixel Clock Frequency (Pin 18, see PLL #2 Electrical Characteristic) | $f_{px}$ | – | 2.0 to 45 | – | MHz |
| 15 kHz Return Pulse Width (Low Time) | $PW_{15k}$ | 0.2 | – | 45 | µs |
| $I^2C$ Clock Frequency | $f_{I^2C}$ | – | – | 100 | kHz |
| Reference Current (Pin 9) | $I_{ref}$ | – | 32 | – | µA |
| Operating Ambient Temperature | $T_A$ | 0 | – | 70 | °C |

All limits are not necessarily functional concurrently.

## ELECTRICAL CHARACTERISTICS ($T_A$ = + 25°C, $V_{CC1} = V_{CC2} = V_{CC3}$ = 5.0 V, unless otherwise noted.)

| Characteristics | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | |
| Power Supply Current ($V_{CC}$ = + 5.0 V) | Pin 40 | 75 | 95 | 115 | mA |
| | Pin 23 | 6.0 | 9.0 | 12 | |
| | Pin 19 | 3.5 | 6.0 | 8.0 | |
| | Total | 85 | 110 | 135 | |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = + 25°C, $V_{CC1} = V_{CC2} = V_{CC3}$ = 5.0 V, unless otherwise noted.)

| Characteristics | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **PAL/NTSC/S–VHS DECODER** | | | | |
| Video 1, 2 Inputs | | | | |
| Crosstalk Rejection, f = 1.0 MHz (Measured at Y1 output, Luma Peaking = 0 dB, $77–7 = 1) | 20 | 40 | – | dB |
| DC Level: @ Selected Input | – | 2.8 | – | Vdc |
| @ Unselected Input | – | 0.7 | – | |
| Clamp Current | – 30 | – 20 | –10 | µA |
| Sound Trap Rejection (See Figures 14 to 23) | | | | |
| With 17.7 MHz Crystal: @ 6.5 MHz (T1, T2 = 00) | 15 | 30 | – | dB |
| @ 6.0 MHz (T1, T2 = 10) | 15 | 30 | – | |
| @ 5.5 MHz (T1, T2 = 11) | 10 | 43 | – | |
| @ 5.74 MHz (T1, T2 = 01) | 15 | 26 | – | |
| With 14.3 MHz Crystal: @ 4.44 MHz (T1, T2 = 11) | – | 35 | – | |
| R–Y, B–Y Outputs (Pins 41, 42) | | | | |
| Output Amplitude (with 100% Saturated Color Bars) | | | | |
| Saturation (DAC 87) = 00 | – | <1.0 | – | mVpp |
| Saturation (DAC 87) = 16 | – | 1.6 | – | Vpp |
| Saturation (DAC 87) = 63 | 1.5 | 1.8 | – | |
| DC Level During Blanking | – | 2.4 | – | Vdc |
| Hue Control – Minimum Phase (DAC 88 = 00) | – 30 | – | – | Deg |
| – Maximum Phase (DAC 88 = 63) | + 30 | – | – | |
| Nominal Saturation (with respect to Y1 Output, Note 1) | – | 100 | – | % |
| B–Y/R–Y Ratio: Balance (DAC 78) = 63 | 1.35 | 1.69 | 2.06 | V/V |
| Balance (DAC 78) = 32 | 0.98 | 1.27 | 1.58 | |
| Balance (DAC 78) = 00 | 0.60 | 0.77 | 0.96 | |
| Output Amplitude Variation as Burst is varied from 80 mVpp to 600 mVpp | – | 3.0 | – | dB |
| Color Kill Attenuation ($7C–7, 6 and $7D–6 = 011) | – | 40 | – | dB |
| Crosstalk with respect to Y1 Output (@ 1.0 MHz) | – 27 | – 20 | – | |
| Chroma Subcarrier Residual | | | | |
| (Measured at Y1 Output, with 17.7 MHz Crystal) | | | | |
| f = Subcarrier | – | 25 | 60 | mVpp |
| 2nd Harmonic Residual | – | 4.0 | 12 | |
| 4th Harmonic Residual | – | 12 | 30 | |
| (Measured at R–Y, B–Y Outputs, with 17.7 or 14.3 MHz Crystal) | | | | |
| f = Subcarrier | – | 5.0 | 20 | |
| 2nd Harmonic Residual | – | 5.0 | 20 | |
| 4th Harmonic Residual | – | 15 | 50 | |
| Y1 Luma Output (Pin 33) | | | | |
| Clamp Level | 0.4 | 1.1 | 1.8 | Vdc |
| Output Impedance | – | 300 | – | Ω |
| Composite Video Mode ($77–6, 7 = 00) | | | | |
| Output Level versus Input Level | | | | |
| Delay = 000, Peaking = 111, f = 100 kHz | 1.0 | 1.1 | 1.2 | V/V |
| Delay = Min–to–Max, Peaking = Min–to–Max | – | 1.1 | – | |
| – 3 dB Bandwidth (17.7 MHz Crystal, PAL Decoding selected, Sound trap at 6.5 MHz, Peaking off) | – | 2.8 | – | MHz |
| Peaking Range ($7D–7, $7E–6/7 = 000 to 111, @ 3.0 MHz, with 17.7 MHz Crystal, Sound trap at 6.5 MHz) | 5 | 8 | 10 | dB |
| Overshoot with Minimum Peaking | – | 0 | – | % |
| Differential Non–linearity (Measured with Staircase) | – | 2.0 | – | % |
| Delay (Pin 1 or 3 to 33) | | | | |
| With 14.3 MHz Crystal: Minimum | – | 690 | – | ns |
| Maximum | – | 1040 | – | |
| With 17.7 MHz Crystal: Minimum | – | 594 | – | |
| Maximum | – | 876 | – | |

**NOTE:** 1. This spec indicates a correct output amplitude at Pins 41 and 42, with respect to Y1 output. For standard color bar inputs, the output amplitude is between 1.5 and 1.7 Vpp, with the settings in Tables 1 and 2.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = + 25°C, $V_{CC1}$ = $V_{CC2}$ = $V_{CC3}$ = 5.0 V, unless otherwise noted.)

| Characteristics | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **PAL/NTSC/S–VHS DECODER** | | | | |
| S–VHS Mode ($77–6, 7 = 11) | | | | |
| Output Level versus Input Level (Delay = Min–to–Max) | 1.0 | 1.1 | 1.2 | V/V |
| – 3 dB Bandwidth (17.7 MHz crystal, PAL Decoding selected, Sound trap at 6.5 MHz) | – | 4.5 | – | MHz |
| Y/C Crosstalk Rejection | 20 | 40 | – | dB |
| Delay (Luma input to Pin 33) | | | | |
| 14.3 MHz Crystal: Minimum | – | 395 | – | ns |
| Maximum | – | 745 | – | |
| 17.7 MHz Crystal: Minimum | – | 350 | – | |
| Maximum | – | 632 | – | |
| Crystal Oscillator | | | | |
| PLL Pull–in range with respect to Subcarrier Frequency | | | | |
| (Burst Level ≥ 30 mVpp): with 17.7 MHz Crystal | – | ± 350 | – | Hz |
| with 14.3 MHz Crystal | – | ± 300 | – | |
| $4f_{SC}$ Filter (Pin 44) DC Voltage | | | | |
| @ 14.3 MHz | – | 2.4 | – | Vdc |
| @ 17.7 MHz | – | 3.5 | – | |
| No Burst present | – | 1.3 | – | |
| DC Voltages | | | | Vdc |
| System Select (Pin 34) | | | | |
| NTSC Mode (SSA = 1, SSB = 0, SSC = 0, SSD = 0) | 1.5 | 1.75 | 2.0 | |
| PAL Mode (SSA = 0, SSB = 1, SSC = 0, SSD = 0) | 0 | 0.075 | 0.4 | |
| Color Kill Mode (SSA = 1, SSB = 1, SSC = 0, SSD = 0) | – | 0.075 | – | |
| External Mode (SSA = X, SSB = X, SSC = 1, SSD = 0) | 3.7 | 4.0 | 4.3 | |
| Ident Filter (Pin 43) | | | | |
| NTSC Mode | – | 1.6 | – | |
| PAL Mode | 1.2 | 1.5 | 1.8 | |
| No Burst present | – | 0.2 | – | |
| ACC Filter (Pin 2) | | | | |
| No Burst present | – | 0.25 | – | |
| Threshold for ACC Flag on | 0.8 | 1.2 | 1.6 | |
| Burst = 50 mVpp | – | 1.4 | – | |
| Burst = 280 mVpp | – | 1.7 | – | |
| System Select Output Impedance | – | 40 | 100 | kΩ |
| **COLOR DIFFERENCE SECTION** | | | | |
| RGB/YUV Outputs | | | | |
| Output Swing, Black–to–White (DAC $81 = 63) | 2.0 | 3.0 | – | Vpp |
| THD (RGB Inputs to RGB Outputs @ 1.0 MHz, 0.7 Vpp) | – | 0.5 | 2.0 | % |
| – 3 dB Bandwidth | – | 6.0 | – | MHz |
| Clamp Level | | | | |
| RGB Outputs ($7D, 7E = 00) | – | 1.4 | – | Vdc |
| UV Outputs ($7D, 7E = 32) | – | 2.3 | – | |
| Red, Blue Clamp Level Change (DACs $7D, 7E varied from 00 to 63) | 0.85 | 1.8 | 2.4 | |
| Crosstalk Rejection | | | | |
| Among RGB Outputs @ 1.0 MHz | 20 | 40 | – | dB |
| Y1 to Y2 | 20 | 40 | – | |
| From RGB Outputs to Y1 or Y2 | 20 | 40 | – | |
| Input Black Clamp Voltage at Y2, B–Y, R–Y, and RGB | 2.4 | 3.0 | 3.6 | Vdc |
| Fast Commutate Input (Pin 25) | | | | |
| Switching Threshold Voltage | – | 0.5 | – | Vdc |
| Input Current @ $V_{in}$ = 0 V | – | – 7.5 | – | μA |
| Input Current @ $V_{in}$ = + 5.0 V | – | 0 | – | |
| Timing: Input Low–to–High (RGB Enable) | – | 50 | – | ns |
| Input High–to–Low (RGB Disable) | – | 90 | – | |

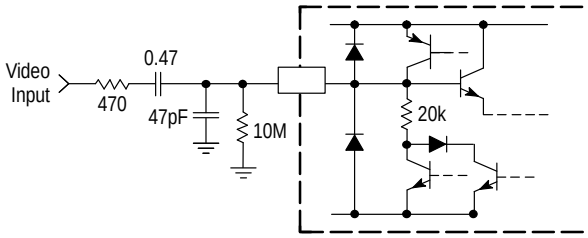
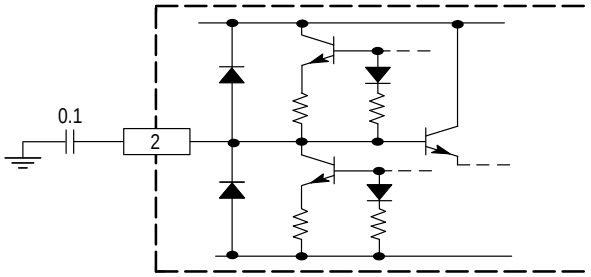
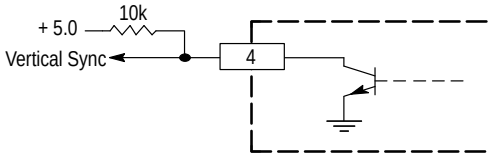
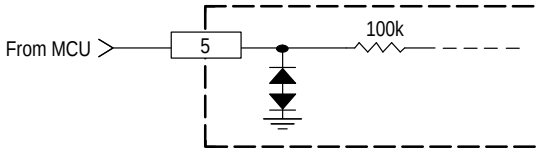
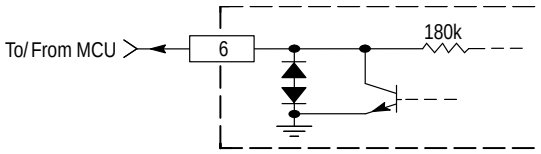
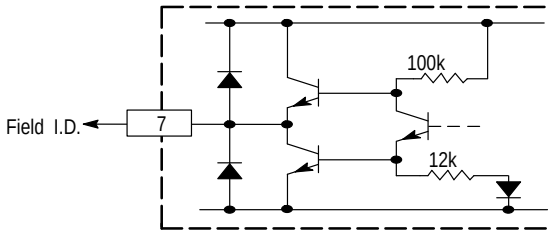
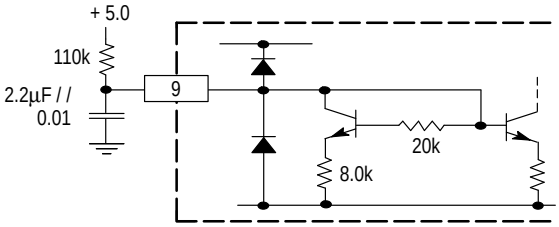
**ELECTRICAL CHARACTERISTICS** ($T_A$ = + 25°C, $V_{CC1}$ = $V_{CC2}$ = $V_{CC3}$ = 5.0 V, unless otherwise noted.)

| Characteristics | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **COLOR DIFFERENCE SECTION** | | | | |
| Contrast (Gain) | | | | V/V |
| Y1 to RGB (DAC $81 = 32, DAC $86 = 00) | 1.9 | 2.4 | 3.0 | |
| Y2 to RGB (DAC $81 = 32, DAC $86 = 00) | 1.8 | 2.3 | 2.8 | |
| Green In (Pin 27) to Green Out (Pin 21) with YX Enabled ($82–6 = 1, DAC $81 and DAC $86 = 32) | 1.8 | 2.3 | 2.4 | |
| Red–to–Green and Blue–to–Green Gain Ratio | 0.8 | 1.0 | 1.2 | |
| RGB Input to RGB Output with YX Not Enabled ($82–6 = 0, DAC $81 and DAC $86 = 32) | 2.0 | 2.6 | 3.2 | |
| Ratio (DAC $81 = 00 versus 32) | – | 0.2 | 0.4 | |
| Ratio (DAC $81 = 63 versus 32) | 1.5 | 2.0 | 2.5 | |
| Red and Blue Trim Control (DACs $80, 82 varied from 00 to 63) | ± 5 | ± 30 | ± 60 | % |
| Saturation (Average of R, G, B saturation levels with respect to Luma) | | | | |
| Inputs at Pins 29 to 31 (DAC $86 = 32) | 50 | 90 | 130 | % |
| Ratio (DAC $86 = 00 versus 32) | – | – | 5 | |
| Ratio (DAC $86 = 63 versus 32) | 150 | 170 | 190 | |
| Inputs at Pins 26 to 28 (DAC $86 = 32, $82–6 = 1) | 70 | 125 | 180 | |
| Brightness | | | | |
| Black Level Range (Brightness = 00 to 63 with respect to Brightness setting of 32) | ± 0.3 | ± 0.5 | ± 0.7 | Vdc |
| Red and Blue Trim Control (DACs $83, 85 varied from 00 to 63) | ± 0.05 | ± 0.3 | ± 0.6 | |
| Color Coefficients | | | | |
| G–Y Matrix Coefficient versus B–Y | – 0.21 | – 0.19 | – 0.17 | |
| G–Y Matrix Coefficient versus R–Y | – 0.56 | – 0.51 | – 0.46 | |
| YX Matrix (Inputs at Pins 26 to 28, $82–6 = 1): | | | | |
| Y versus R | 0.28 | 0.30 | 0.32 | |
| Y versus G | 0.57 | 0.59 | 0.61 | |
| Y versus B | 0.09 | 0.11 | 0.13 | |
| **HORIZONTAL TIME BASE SECTION (PLL #1)** | | | | |
| Free–Running Period (Calibration mode in effect, Bit $86–6 = 1) | | | | |
| 17.7 MHz Crystal selected ($84–6 = 0) | 62.5 | 64.0 | 65.5 | µs |
| 14.3 MHz Crystal selected ($84–6 = 1) | 62.5 | 63.5 | 65.5 | |
| VCO minimum period (Pin 11 Voltage at 1.2 V) | 56 | 59.5 | 62 | µs |
| VCO maximum period (Pin 11 Voltage at 2.8 V) | 66 | 69.5 | 72 | |
| VCO Control Gain factor | 5.0 | 8.5 | 12 | µs/V |
| Phase Detector Current | | | | |
| High Gain ($83–6 = 1) | 15 | 50 | 85 | µA |
| Low Gain–to–High Gain Current Ratio | 0.32 | 0.38 | 0.44 | µA/µA |
| Noise Gate Width ($77–2 = 0, Low Gain, see Figure 26) | – | 16 | – | µs |
| Horizontal Filter Switch (Pin 12) | | | | |
| Saturation Voltage ($I_{12}$ = 20 µA) | – | 10 | 100 | mV |
| Dynamic Impendance ($84–7 = 1) | – | < 5.0 | – | kΩ |
| Parallel Resistance ($84–7 = 0) | 0.6 | 1.0 | – | MΩ |
| Pins 8, 13, 14 Output Level | | | | |
| High ($I_O$ = – 40 µA) | 2.4 | 4.5 | – | Vdc |
| Low ($I_O$ = + 800 µA) | – | 0.1 | 0.8 | |
| Burst Gate (Pin 8) Timing (See Figures 25, 27) | | | | µs |
| Rising edge from Sync leading edge (Pins 1, 3) | 4.4 | 5.6 | 6.8 | |
| Rising edge from Sync center (Pins 26 to 29) | – | 2.5 | – | |
| Pulse Width | 3.0 | 3.5 | 4.0 | |
| 16 Fh Output (Pin 13) Timing (Bit $85–6 = 0) (See Figures 25, 27) | | | | |
| Rising edge from Fh rising edge | – | 1.3 | – | µs |
| Duty Cycle | – | 50 | – | % |
| Composite Sync Output (Pin 13) Timing (Bit $85–6 = 1) | | | | µs |
| Input Sync center to Output Sync center (Pins 1, 3) | – | 0.95 | – | |
| Input Sync center to Output Sync center (Pins 26 to 29) | – | 0.4 | – | |

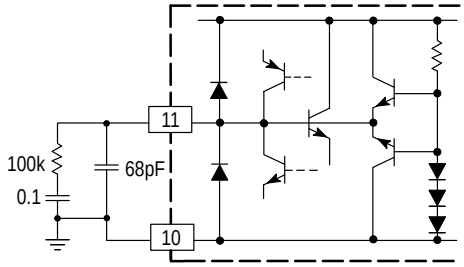
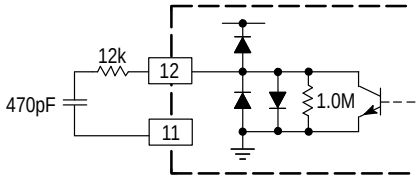
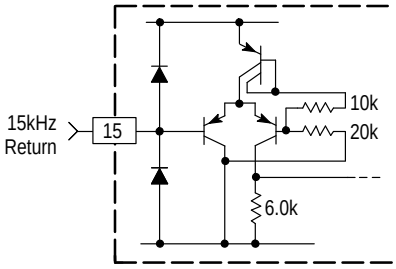
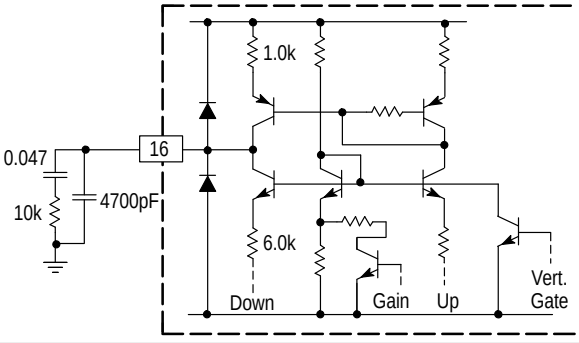
**ELECTRICAL CHARACTERISTICS** ($T_A$ = + 25°C, $V_{CC1} = V_{CC2} = V_{CC3}$ = 5.0 V, unless otherwise noted.)

| Characteristics | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **HORIZONTAL TIME BASE SECTION (PLL #1)** | | | | |
| Fh Reference (Pin 14) Timing (See Figures 25, 27) | | | | |
| Rising edge from Sync center (Pins 1, 3) | – | 1.3 | – | µs |
| Rising edge from Sync center (Pins 26 to 29) | – | 650 | – | ns |
| Duty cycle | – | 50 | – | % |
| Sandcastle Output (Pin 35, see Figures 25, 27) | | | | Vdc |
| Output Voltage – Level 1 | 3.7 | 4.0 | 4.3 | |
| Output Voltage – Level 2 | 2.8 | 3.0 | 3.2 | |
| Output Voltage – Level 3 | – | 1.55 | – | |
| Output Voltage – Level 4 | – | 0.07 | – | |
| Rising edge from Sync center (Pins 1, 3) | – | – 2.6 | – | µs |
| Rising edge from Sync center (Pins 26 to 29) | – | – 3.3 | – | |
| High Time | – | 6.0 | – | |
| Level 2 Time | – | 5.0 | – | |
| Reference Voltage @ Pin 9 ($I_{ref}$ = 32 µA) | 1.0 | 1.2 | 1.4 | Vdc |
| **PHASE–LOCKED PIXEL CLOCK SECTION (PLL #2)** | | | | |
| VCO Frequency @ Pin 18 | | | | MHz |
| Minimum (Pin 16 = 1.6 V, $85–7 = 1) | – | 2.0 | 4.0 | |
| Maximum (Pin 16 = 4.0 V, $85–7= 0) | 30 | 45 | 60 | |
| VCO Up (Flag 19) Threshold Voltage @ Pin 16 | 1.5 | 1.7 | 1.9 | Vdc |
| VCO Down (Flag 20) Threshold Voltage @ Pin 16 | 3.1 | 3.3 | 3.5 | |
| VCO Control Voltage Range @ Pin 16 | 1.2 | – | 3.8 | Vdc |
| VCO Control Gain factor ($7FDAC = 00, $85–7 = 0) | 4.0 | 8.0 | 12 | MHz/V |
| Charge Pump Current (Pin 16) | 25 | 50 | 75 | µA |
| High Gain ($83–7 = 0) | | | | |
| Current Ratio | 0.3 | 0.4 | 0.5 | µA/µA |
| Low Gain–to–High Gain | | | | |
| Pixel Clock Output (Pin 18) (Load = 3 FAST TTL loads + 10 pF) | | | | |
| Output Voltage – High | – | 3.9 | – | Vdc |
| Output Voltage – Low | – | 0.15 | – | |
| Rise Time @ 50 MHz | – | 7.0 | – | ns |
| Rise Time @ 9.0 MHz | – | 17 | – | |
| Fall Time @ 50 MHz | – | 5.0 | – | |
| Fall Time @ 9.0 MHz | – | 8.0 | – | |
| 15 kHz Return (Pin 15) | | | | |
| Input Threshold Voltage | – | 1.5 | – | Vdc |
| Falling edge from Fh rising edge | – | 60 | – | ns |
| Minimum Input Low Time | 200 | – | – | |
| **VERTICAL DECODER** | | | | |
| Vertical Frequency Range | 43.3 | – | 122 | Hz |
| Vertical Sync Output | | | | |
| Saturation Voltage ($I_O$ = 800 µA) | – | 0.1 | 0.8 | V |
| Leakage Current @ 5.0 V (Output high) | – | – | 40 | µA |
| Timing from Sync polarity reversal to Pin 4 falling edge (See Figures 33, 34) | | | | µs |
| ($78–7 = 0) | 32 | 36 | 40 | |
| ($78–7 = 1) | 62 | 68 | 74 | |
| Vertical Sync Pulse Width (Pin 4, NTSC or PAL) | 490 | 500 | 510 | µs |
| Field Ident (Pin 7) Output Voltage – High ($I_O$ = – 40 µA) | 2.4 | 4.5 | – | Vdc |
| Output Voltage – Low ($I_O$ = + 800 µA) | – | 0.1 | 0.8 | |
| Timing | – | Fig. 33, 34 | – | |
| **HORIZONTAL SYNC SEPARATOR** | | | | |
| Sync Slicing Levels (Pins 1, 3) | – | 120 | – | mV |
| From Black Level (Pins 26 to 29) | – | 150 | – | |

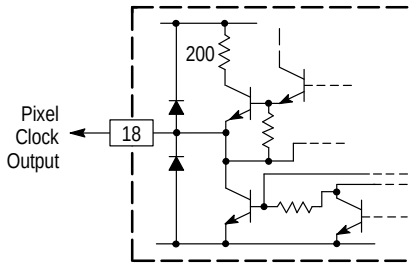
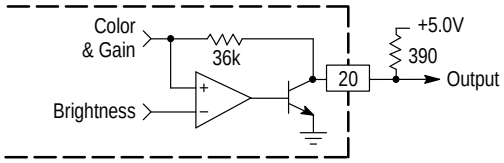
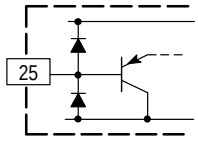
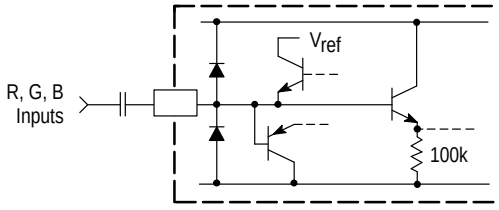
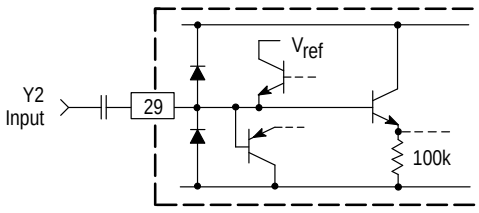
## PIN FUNCTION DESCRIPTION

| FB QFP Pin | FN PLCC Pin | Representative Circuitry (Pin nos. refer to PLCC pkg.) | Description (Pin nos. refer to PLCC pkg.) |
|---|---|---|---|
| 39, 41 | 1, 3 |  | **Video Input 1 & 2** – Video 1 (Pin 1) and Video 2 (Pin 3) are composite video inputs. Either can be NTSC or PAL. Input impedance is high, termination must be external. Also used for the luma and chroma components of an S–VHS signal. Selection of these inputs is done by software. External components protect against ESD and noise. |
| 40 | 2 |  | **ACC Filter** – A 0.1 µF capacitor at this pin filters the feedback loop of the chroma automatic gain control amplifier. Input chroma burst amplitude can be between 30 and 600 $mV_{pp}$. |
| 42 | 4 |  | **Vertical Sync Output** – An open collector output requiring an external pull–up. Output is an active low pulse, 500 µs wide, occurring each field. Timing of this pulse depends on Bit $78–7. |
| 43 | 5 |  | **SCL** – Clock for the $I^2C$ bus interface. See Appendix C for specifications. Maximum frequency is 100 kHz. |
| 44 | 6 |  | **SDL** – Bidirectional data line for the $I^2C$ bus interface. As an output, it is an open collector. (Write Address $8A, Read Address $8B) |
| 1 | 7 |  | **Field ID** – TTL level output indicating Field 1 or Field 2. Polarity depends on state of Bit $78–7 (Vert. Sync Delay). See Table 11 and Figure 33 and 34. |
| 2 | 8 | (Same as Pin 7) | **Burst Gate** – TTL level output used for external clamps, as well as internally. Pulse is active high, ≈ 3.5 µs wide, with the rising edge ≈ 3.0 µs after center of selected incoming sync pulse. |
| 3 | 9 |  | **Reference Current Input** – Current supplied to this pin, typically 32 µA from + 5.0 V through a 110 kΩ resistor, is the reference current for the calibration circuit. Noise filtering should be done at the pin. Voltage at this pin is typically 1.2 V. |

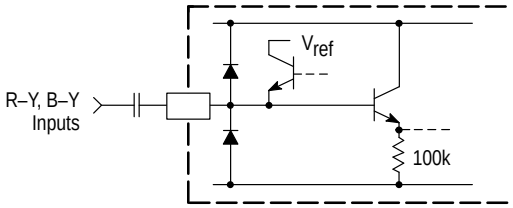
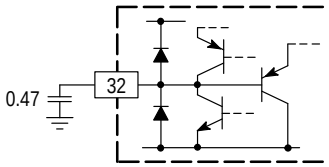
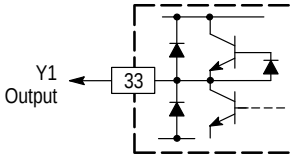
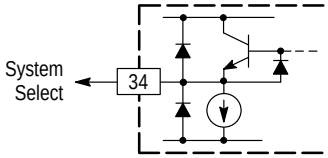
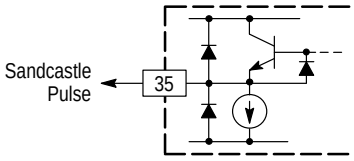
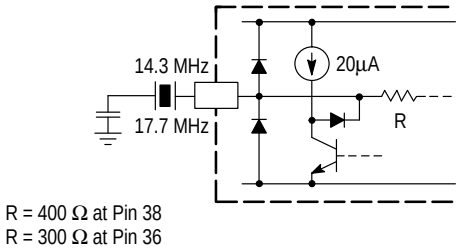
## PIN FUNCTION DESCRIPTION

| FB QFP Pin | FN PLCC Pin | Representative Circuitry (Pin nos. refer to PLCC pkg.) | Description (Pin nos. refer to PLCC pkg.) |
|---|---|---|---|
| 4 | 10 | (See power distribution diagram at the end of this section.) | **Quiet Ground** – Ground for the horizontal PLL filter (PLL #1) at Pin 11. |
| 5 | 11 |  | **H Filter** – Components at this pin filter the output of the phase detector of PLL #1. This PLL becomes phase–locked to the selected incoming horizontal sync. External component values are valid for NTSC and PAL systems. |
| 6 | 12 |  | **H Filter Switch** – An internal switch–to–ground which permits altering the filtering action of the components at Pin 11. |
| 7 | 13 | (Same as Pin 7) | **16 Fh/$C_{Sync}$** – A TTL level output from PLL #1. This pin provides either a square wave equal to Fh x 16 (≈ 250 kHz), or composite sync, depending on the setting of Bit $85–6. |
| 8 | 14 | (Same as Pin 7) | **Fh Reference** – A TTL square wave output which is phase–locked to the selected incoming horizontal sync. The rising edge occurs ≈ 1.3 μs after sync center. |
| 9 | 15 |  | **15 kHz Return** – This TTL input receives the output of an external frequency divider which is part of PLL #2 (Pixel Clock PLL). This signal will be phase and frequency–locked to the Fh signal at Pin 14. If PLL #2 is not used, this pin should be connected to a + 5.0 V supply. |
| 10 | 16 |  | **PLL #2 Filter** – Components at this pin filter the output of the phase detector of PLL 2. This PLL becomes phase–locked to the Fh signal at Pin 14. Recommended values for filter components are shown. External components should be connected to ground at Pin 17. If PLL #2 is not used, this pin should be grounded. |
| 11 | 17 | (See power distribution diagram at the end of this section.) | **GND 3** – Ground for the high frequency PLL #2. Signals at Pins 15 to 19 should be referenced to this ground. |

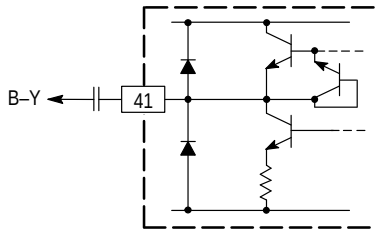
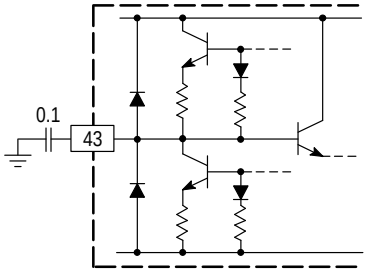
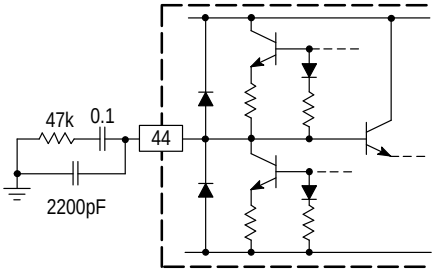
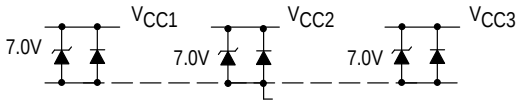
## PIN FUNCTION DESCRIPTION

| FB QFP Pin | FN PLCC Pin | Representative Circuitry (Pin nos. refer to PLCC pkg.) | Description (Pin nos. refer to PLCC pkg.) |
|---|---|---|---|
| 12 | 18 |  | **Pixel Clock Output** – Sampling clock output (TTL) for external A/D converters, and for the external frequency divider. Frequency range at this pin is 6.0 to 40 MHz. |
| 13 | 19 | (See power distribution diagram at the end of this section.) | **$V_{CC3}$** – A + 5.0 V supply (± 5%), for the high frequency PLL #2. Decoupling must be provided from this pin to Pin 17. Ripple on this pin will affect pixel clock jitter. |
| 14 | 20 |  | **R/V Output** – Red (in RGB mode), or R–Y (in YUV mode), output from the color difference stage. A pull–up (390 Ω) to + 5.0 V is required. Blank level is ≈ +1.4 Vdc. Maximum amplitude is ≈ 3.0 Vpp, black–to–white. |
| 15 | 21 | (Same as Pin 20) | **G/Y Output** – Green (in RGB mode), or Y (in YUV mode), output from the color difference stage (same as Pin 20). |
| 16 | 22 | (Same as Pin 20) | **B/U Output** – Blue (in RGB mode), or B–Y (in YUV mode), output from the color difference stage (same as Pin 20). |
| 17 | 23 | (See power distribution diagram at the end of this section.) | **$V_{CC2}$** – A + 5.0 V supply (± 5%), for the color difference stage. Decoupling must be provided from this pin to Pin 24. |
| 18 | 24 | (See power distribution diagram at the end of this section.) | **GND 2** – Ground for the color difference stage. Signals at Pins 20 to 31 should be referenced to this pin. |
| 19 | 25 |  | **FC** – Fast Commutate switch. Taking this pin high (TTL level) connects the RGB inputs (Pins 26 to 28) to the RGB outputs (Pins 20 to 22), permitting an overlay function. The switch can be disabled in software (Bit $80–7). |
| 20, 21, 22 | 26, 27, 28 |  | **Blue (26), Green (27), Red (28) Inputs** – Inputs to the color difference stage. Designed to accept standard analog video levels, these input pins have a clamp and sync separator. They are selected with Pin 25 or in software (Bit $80–7). |
| 23 | 29 |  | **Y2 Input** – Luma #2/Composite sync input. This luma input to the color difference stage is used in conjunction with auxiliary color difference inputs, and/or as a sync input. Clamp and sync separator are provided. |

## PIN FUNCTION DESCRIPTION

| FB QFP Pin | FN PLCC Pin | Representative Circuitry (Pin nos. refer to PLCC pkg.) | Description (Pin nos. refer to PLCC pkg.) |
|---|---|---|---|
| 24, 25 | 30, 31 |  | **B–Y (30), R–Y (31) Inputs** – Inputs to the color difference stage. Designed for standard color difference levels, these inputs can be capacitor coupled from the color difference outputs, from a delay line, or an auxiliary signal source. Input clamp is provided. |
| 26 | 32 |  | **Y1 Clamp** – A 0.47 µF capacitor at this pin provides clamping for the Luma #1 output. |
| 27 | 33 |  | **Y1 Output** – Luma #1 output. This output from the PAL/NTSC/S–VHS decoder is the luma component of the decoded composite video at Pin 1 or 3. It is internally directed to the color difference stage. |
| 28 | 34 |  | **System Select** – A multi–level DC output which indicates the color decoding system to which the PAL/NTSC detector is set by the software. This output is used by the MC44140 chroma delay line. |
| 29 | 35 |  | **Sandcastle Pulse** – A multi–level timing pulse output used by the MC44140 chroma delay line. This pulse encompasses the horizontal sync and burst time. |
| 30, 32 | 36, 38 |  | **Xtal 2 (36), Xtal 1 (38)** – Designed for connection of 4x subcarrier color crystals. Selection is done in software. The selected frequency is used by the PAL/NTSC detector; system identifier; all notches and traps; delay lines; and the horizontal calibration circuit.<br>The crystal frequency should be:<br>14.3 MHz at Pin 36 for NTSC,<br>17.7 MHz at Pin 38 for PAL.<br><br>(See Table 18 for crystal specs.) |
| 31 | 37 | | **No Connect** – This pin is to be left open. |
| 33 | 39 | (See power distribution diagram at the end of this section.) | **Ground 1** – Ground for all sections except PLL #2 and the color difference stage. |
| 34 | 40 | (See power distribution diagram at the end of this section.) | **$V_{CC1}$** – A + 5.0 V (± 5%), supply to all sections except PLL #2 and the color difference stage. |

## PIN FUNCTION DESCRIPTION

| FB QFP Pin | FN PLCC Pin | Representative Circuitry (Pin nos. refer to PLCC pkg.) | Description (Pin nos. refer to PLCC pkg.) |
|---|---|---|---|
| 35 | 41 |  | **B–Y Output** – Output from the PAL/NTSC decoder, it is typically capacitor–coupled to a delay line or to the B–Y input. This pin is clamped, and filtered at the color subcarrier frequency, 2x, and 8x that frequency. |
| 36 | 42 | (Same as Pin 41) | **R–Y Output** – Output from the PAL/NTSC decoder. |
| 37 | 43 |  | **Ident Filter** – A 0.1 μF capacitor filters the system identification circuit in the NTSC/PAL decoder. |
| 38 | 44 |  | **Crystal PLL Filter** – Components at this pin filter the PLL for the crystal chroma oscillator circuit. |
| 4, 11, 13, 17, 18, 33, 34 | 10, 17, 19, 23, 24, 39, 40 |  (Dashed lines indicate substrate connection.) | **Power Distribution** – The three $V_{CC}$ pins must be externally connected to + 5.0 V (± 5%) supply. The four grounds must be externally tied together, preferably to a ground plane. |

## Luma Frequency Response (14.3 MHz) Crystal, (4.5 MHz) Sound Trap

**Figure 2. Comp. Video Mode**

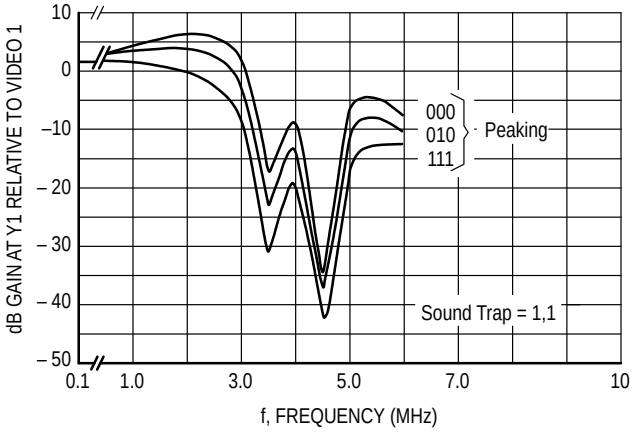
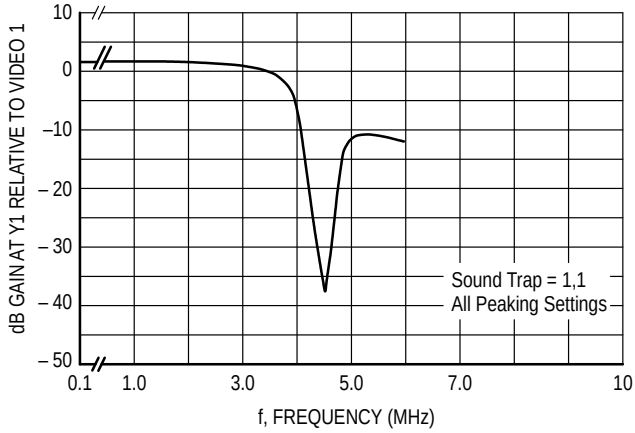



**Figure 3. S–VHS Mode**




## Luma Frequency Response (17.7 MHz) Crystal, (5.5 MHz) Sound Trap

**Figure 4. Comp. Video Mode**

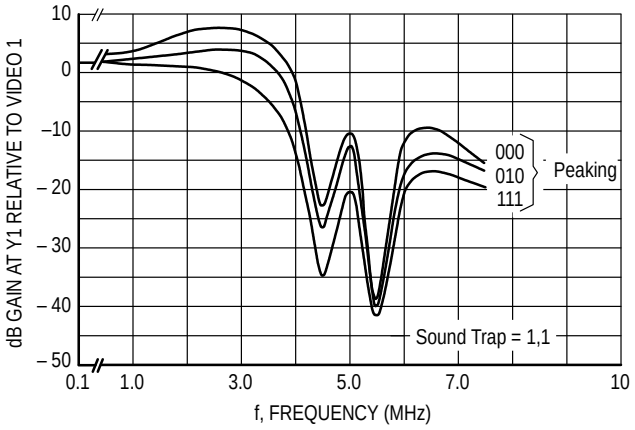
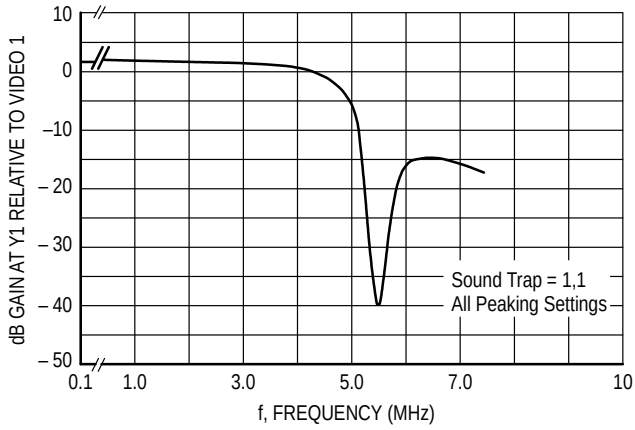



**Figure 5. S–VHS Mode**




## Luma Frequency Response (17.7 MHz) Crystal, (5.5/5.75 MHz) Sound Trap

**Figure 6. Comp. Video Mode**

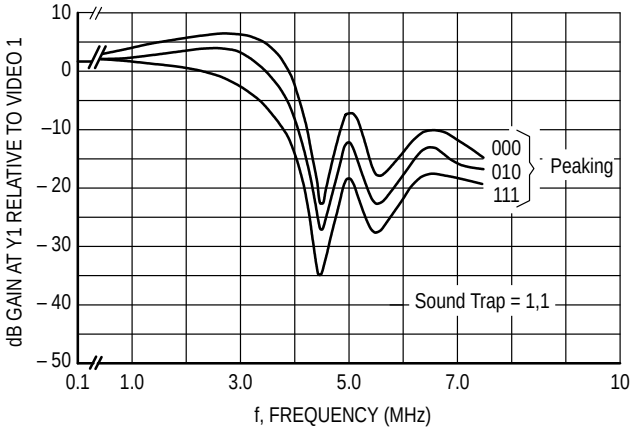
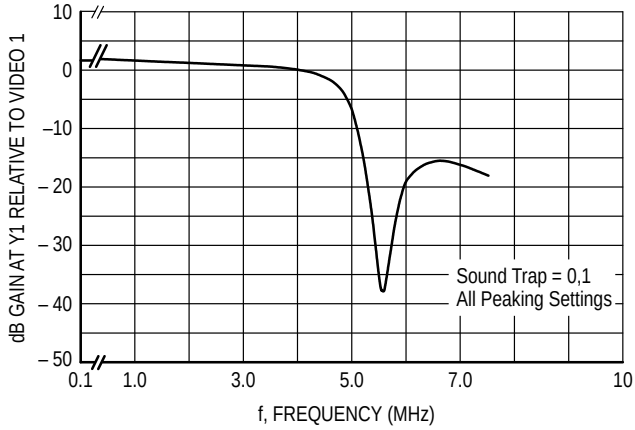



**Figure 7. S–VHS Mode**



## Luma Frequency Response (17.7 MHz) Crystal, (6.0 MHz) Sound Trap

**Figure 8. Comp. Video Mode**

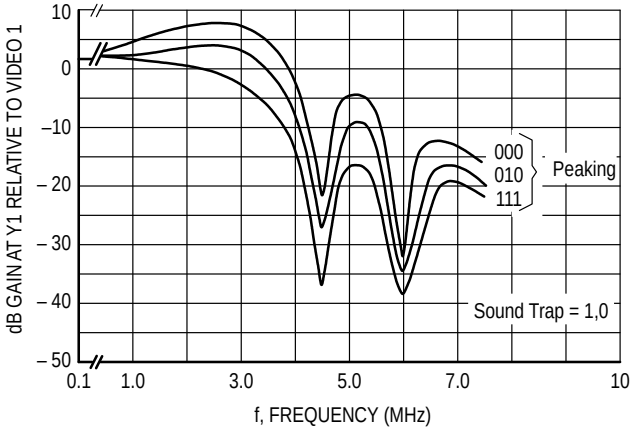
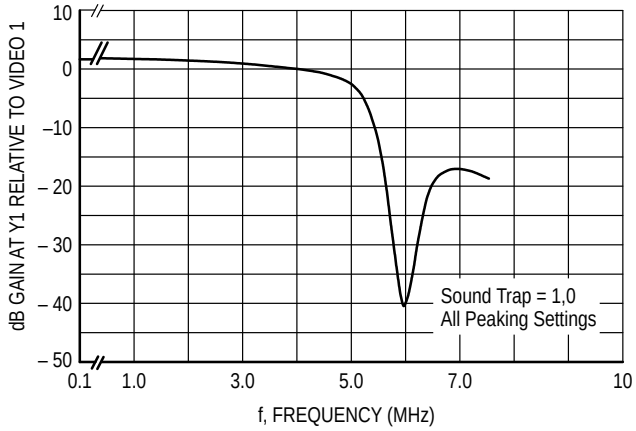



**Figure 9. S–VHS Mode**




## Luma Frequency Response (17.7 MHz) Crystal, (6.5 MHz) Sound Trap

**Figure 10. Comp. Video Mode**

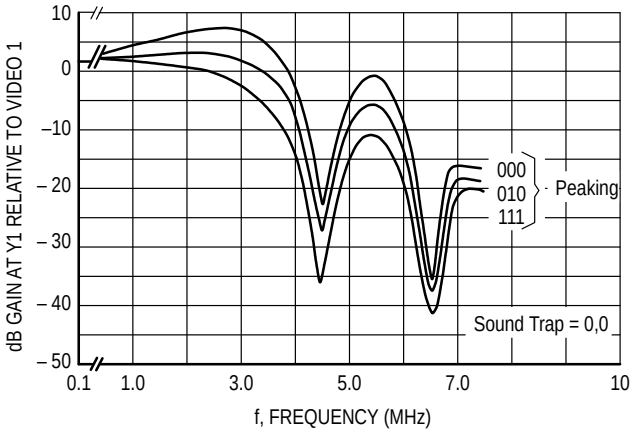



**Figure 11. S–VHS Mode**

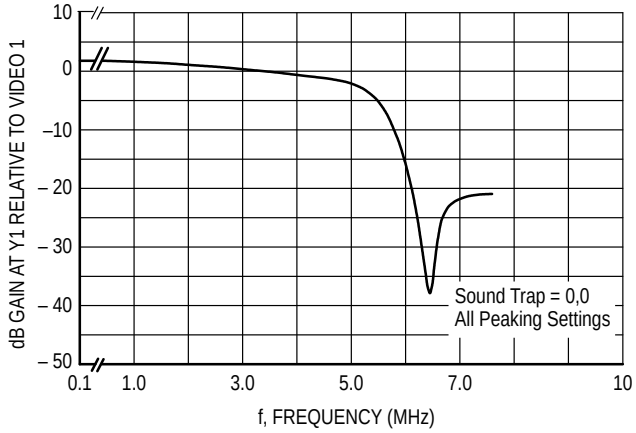



**Figure 12. (3.58 MHz) Chroma Notch**

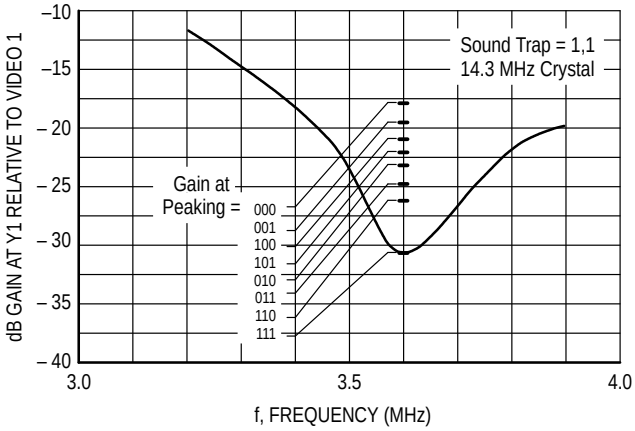
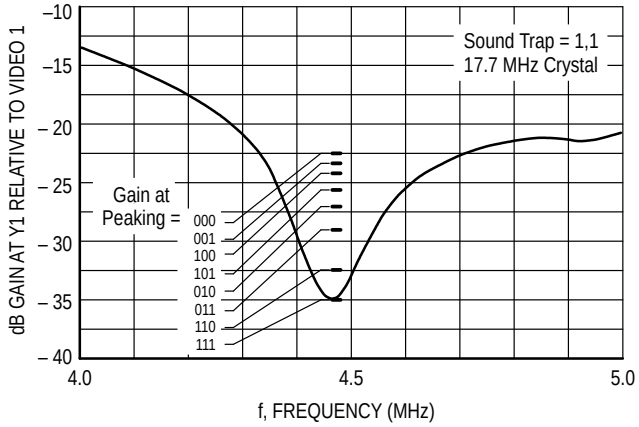



**Figure 13. (4.43 MHz) Chroma Notch**



### (4.5 MHz) Sound Trap

**Figure 14. Comp. Video Mode**

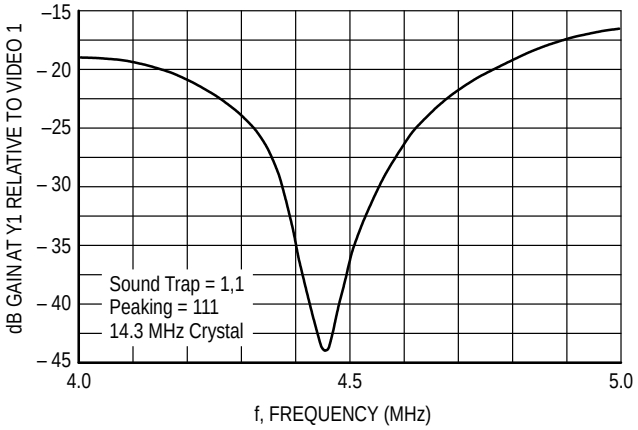
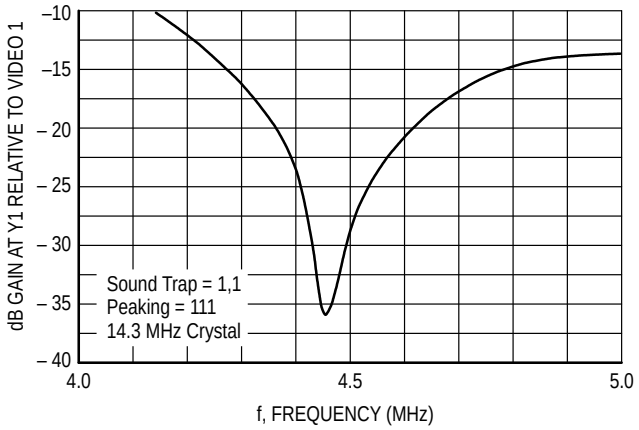



**Figure 15. S–VHS Mode**




### (5.5 MHz) Sound Trap

**Figure 16. Comp. Video Mode**

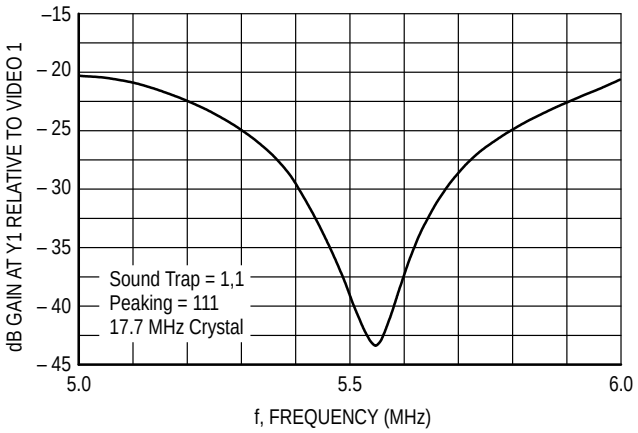
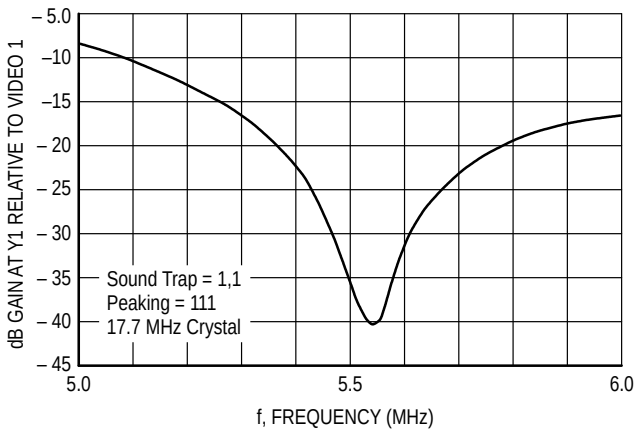



**Figure 17. S–VHS Mode**




### (5.5 + 5.75 MHz) Sound Trap

**Figure 18. Comp. Video Mode**

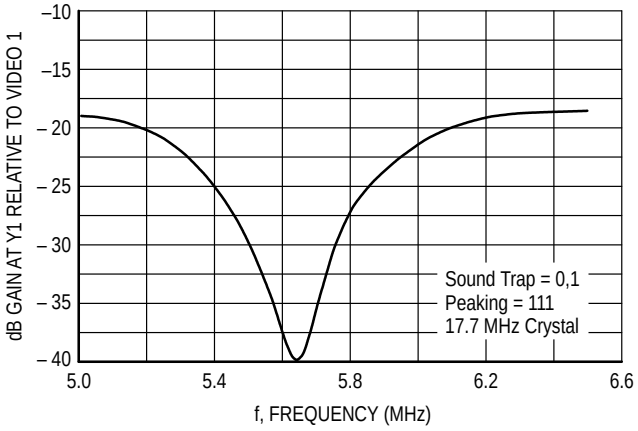
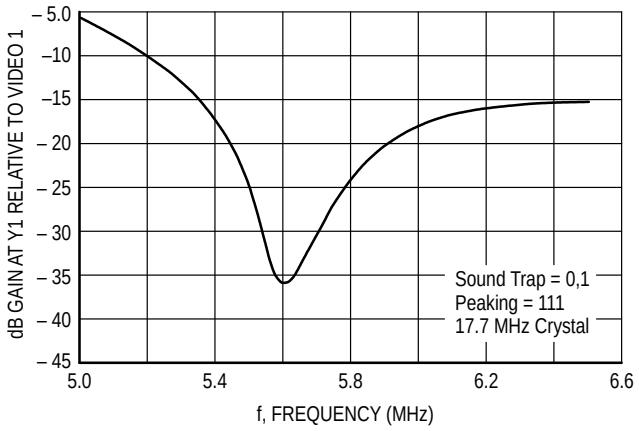



**Figure 19. S–VHS Mode**



**(6.0 MHz) Sound Trap**

**Figure 20. Comp. Video Mode**

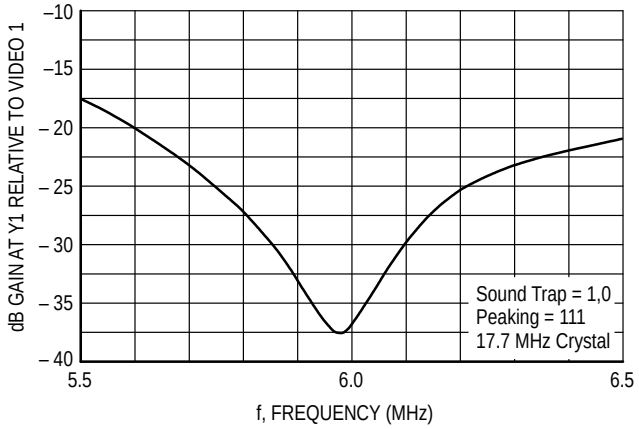
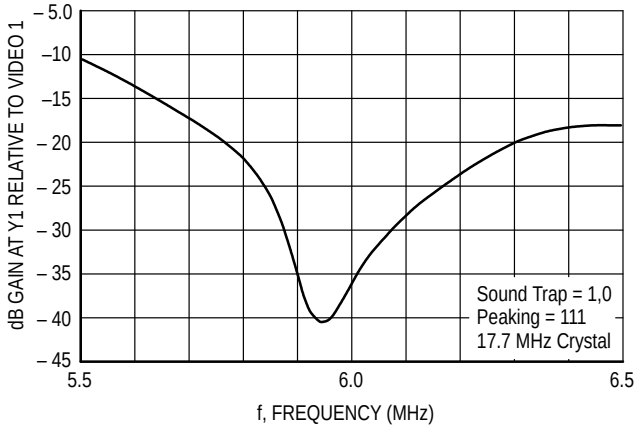



**Figure 21. S–VHS Mode**




**(6.5 MHz) Sound Trap**

**Figure 22. Comp. Video Mode**

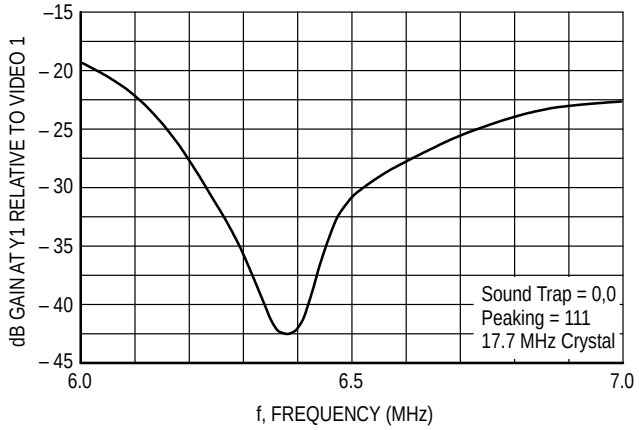



**Figure 23. S–VHS Mode**

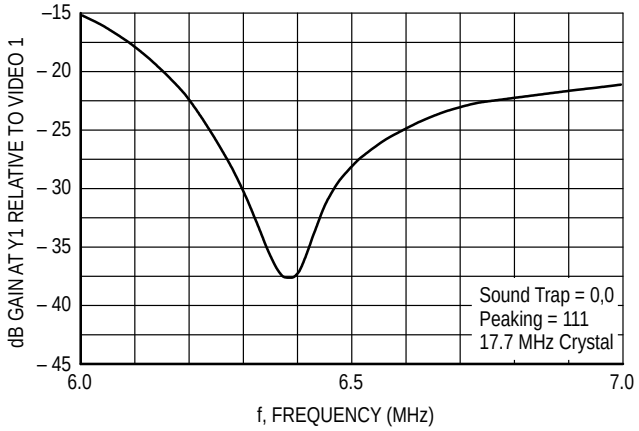



**Figure 24. FC Input Current**

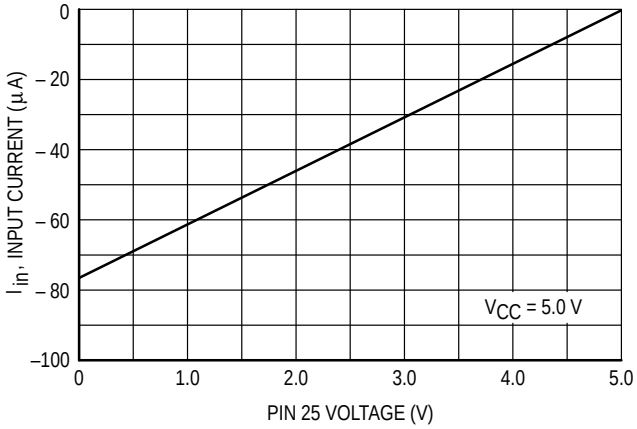
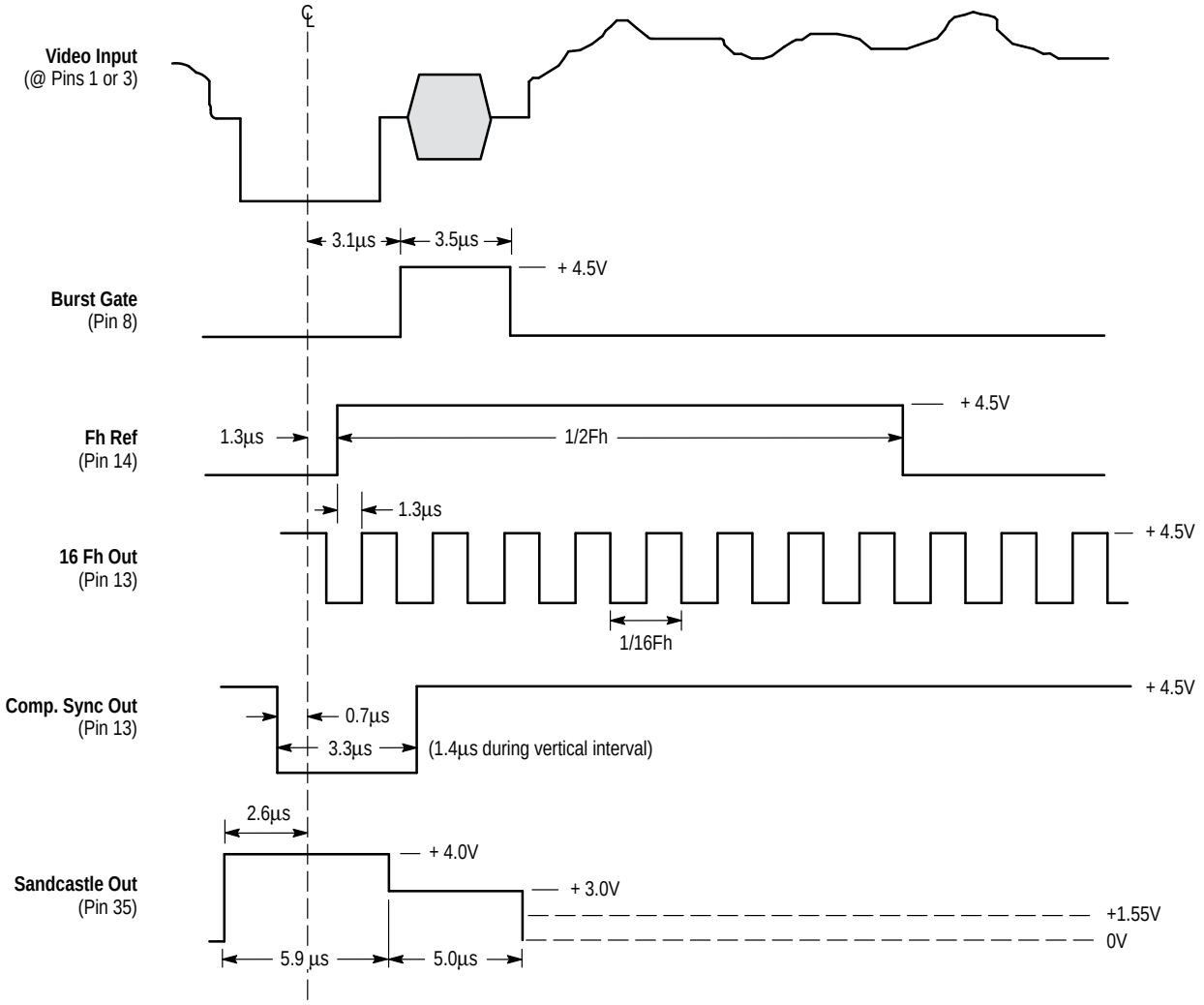


**Figure 25. Horizontal PLL1 Timing/Composite Video Inputs**




**NOTE:** In above waveforms, all timing is referenced to the **center** of the incoming Sync Pulse at Pin 1 or 3.
Above timings based on a 4.6 µs wide sync pulse.
Lower two levels of Sandcastle output alternate, based on video system in effect.
All timings are nominal, and apply to both PAL and NTSC signals.

**Figure 26. Horizontal PLL1 Noise Gate and Filter Pin**

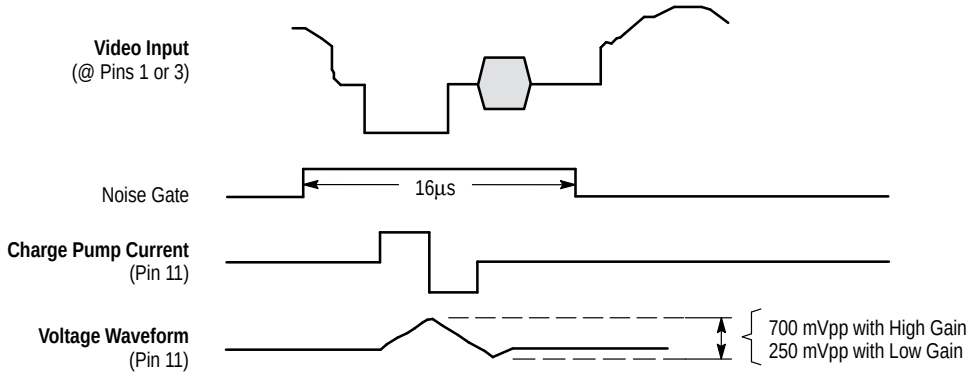
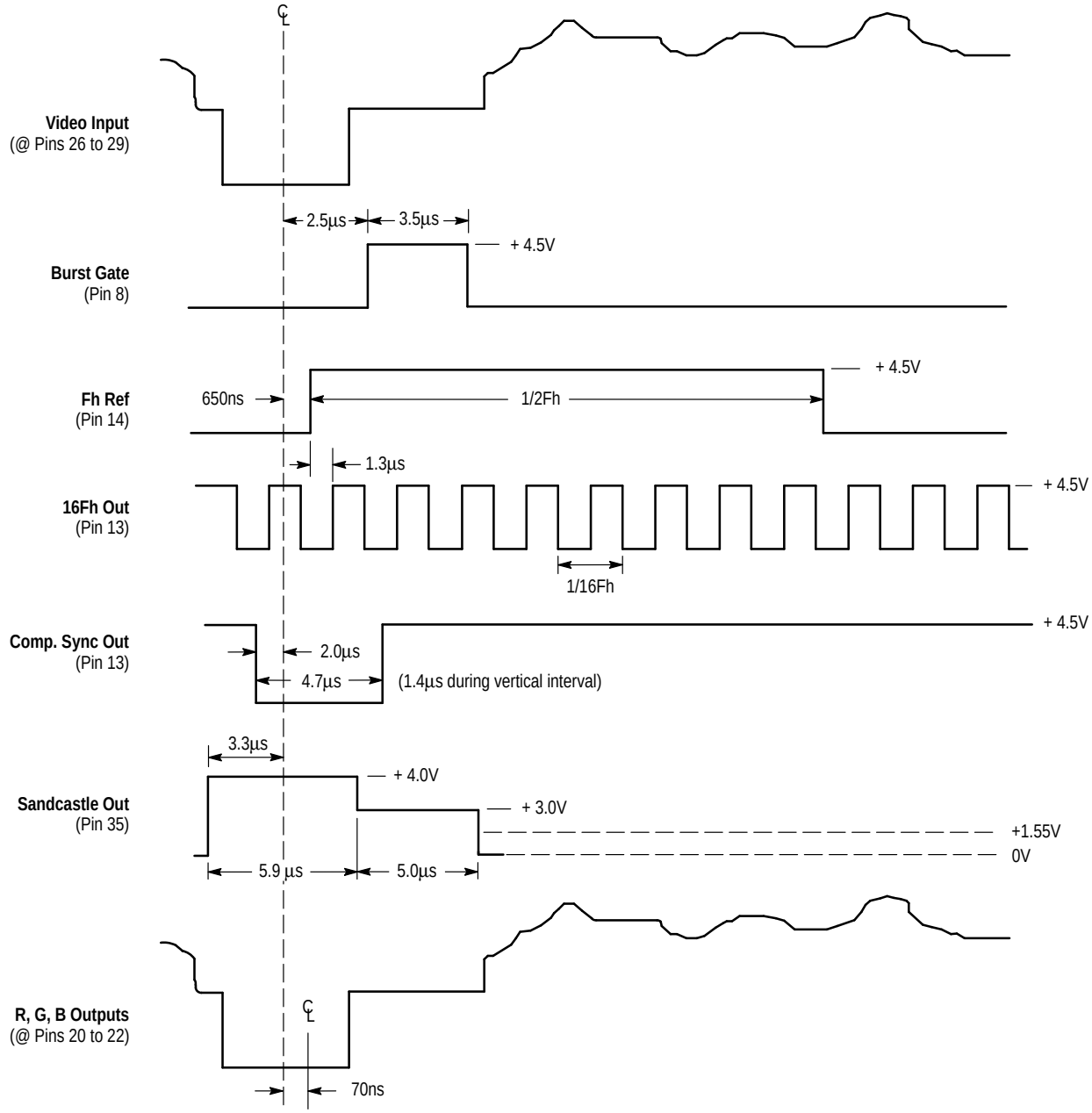


**Figure 27. Horizontal PLL1 Timing/R, G, B and Y2 Inputs**




**NOTE:** In above waveforms, all timing is referenced to the **center** of the incoming Sync Pulse at Pin 26 to 28, or 29.
Above timings based on a 4.6 µs wide sync pulse.
Lower two levels of Sandcastle output alternate, based on video system in effect.

**Figure 28. System Timing/Video Inputs to RGB Outputs**

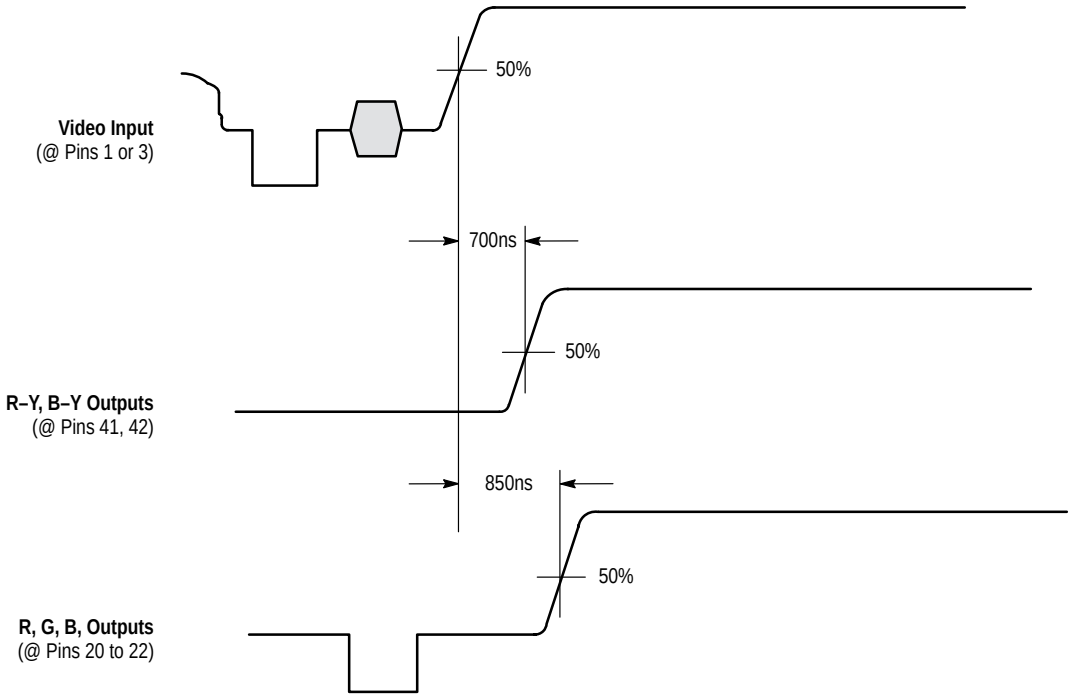



**Figure 29. Fast Commutate Timing**

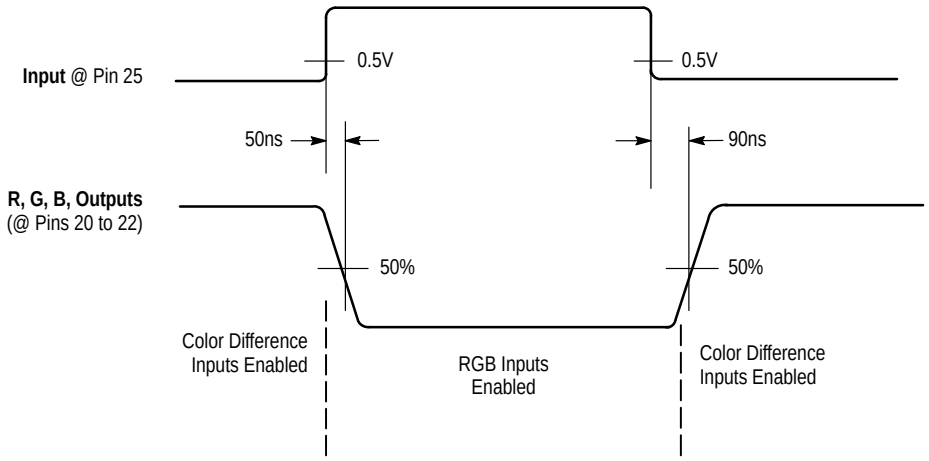


**Figure 30. Horizontal Outputs versus Fields (NTSC System)**

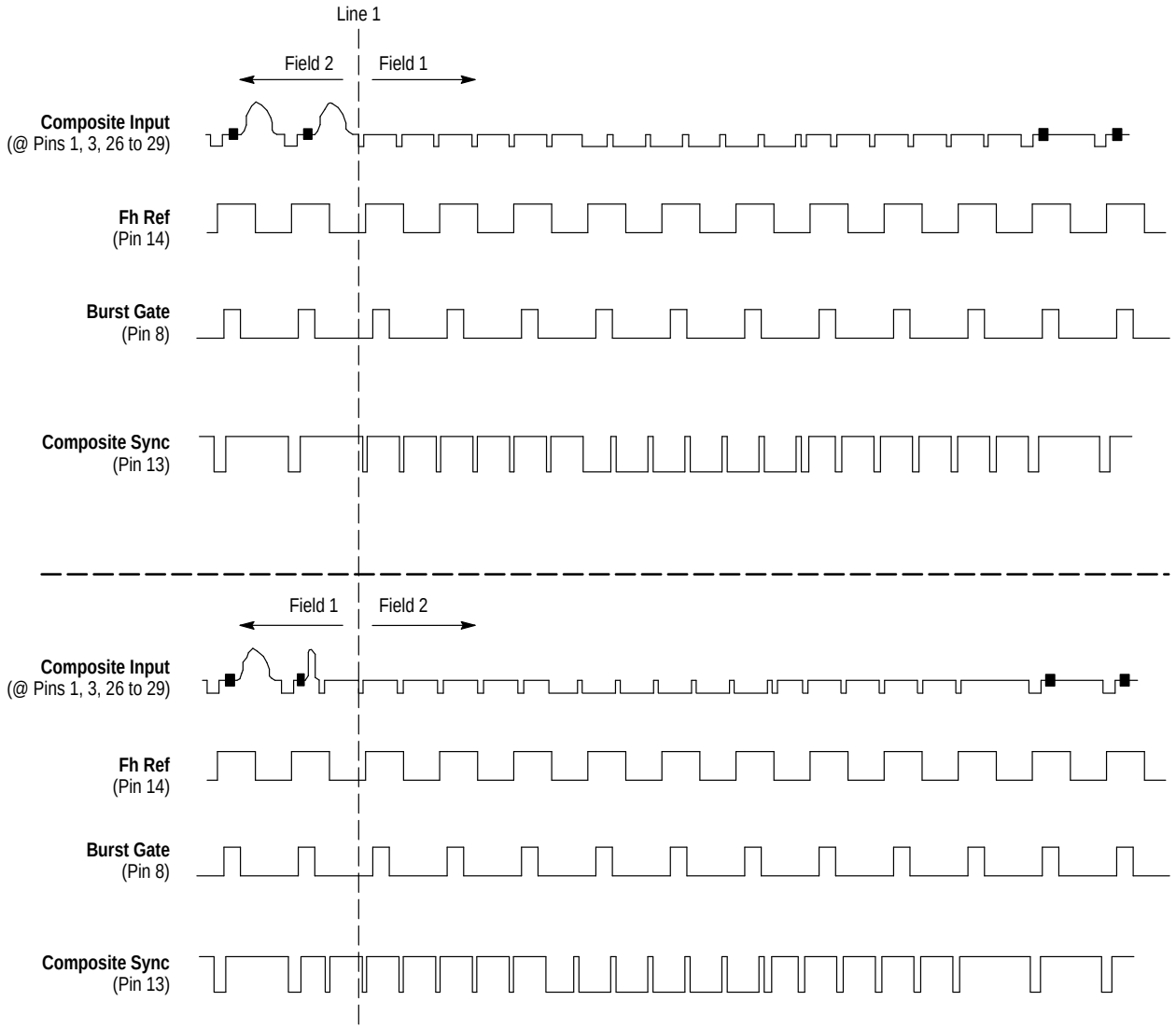


**Figure 31. Horizontal Outputs versus Fields (PAL System)**

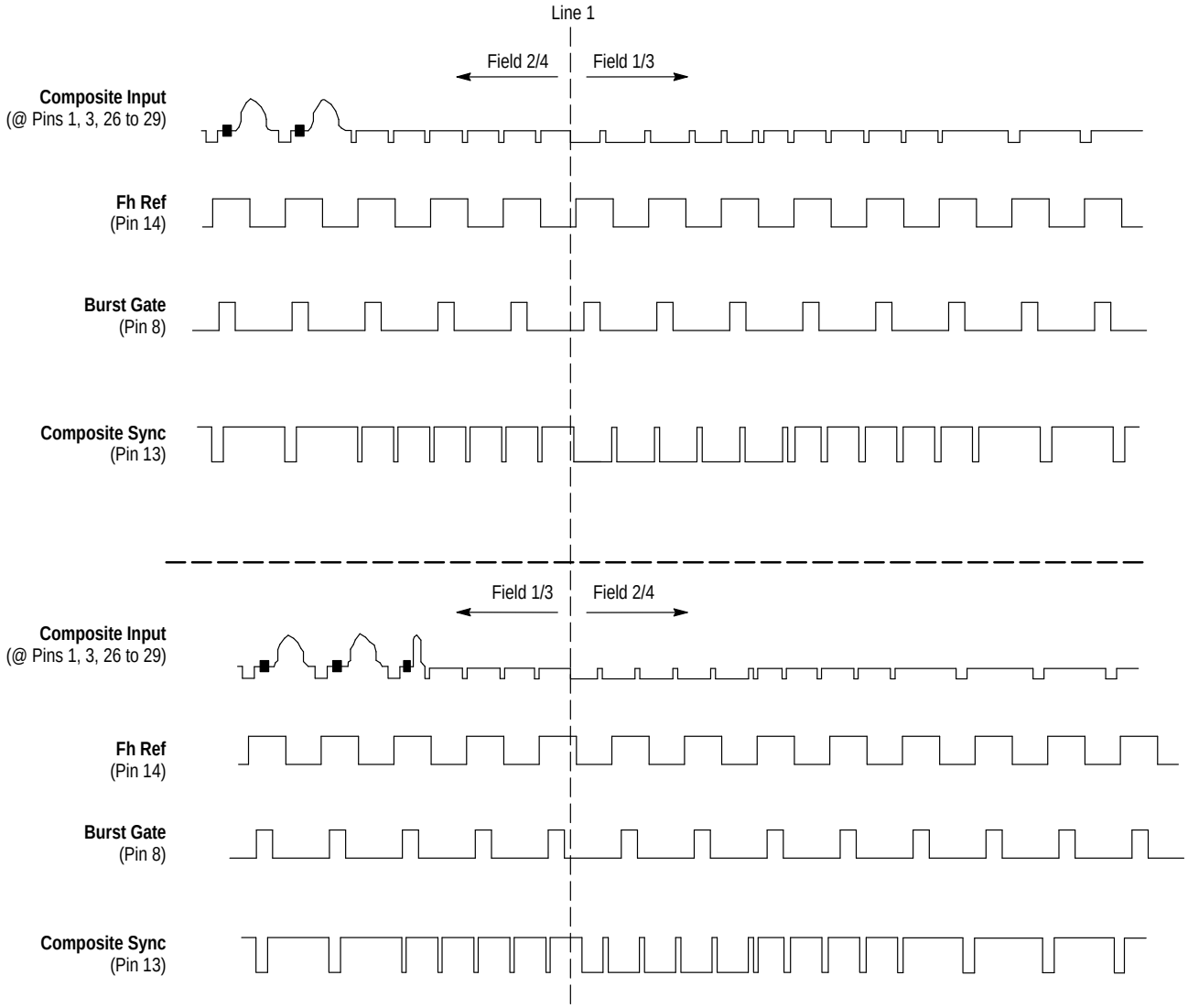



**Figure 32. Horizontal PLL2 Timing**

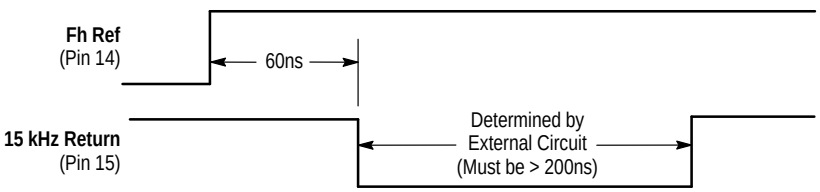


**Figure 33. Vertical Timing (NTSC System)**

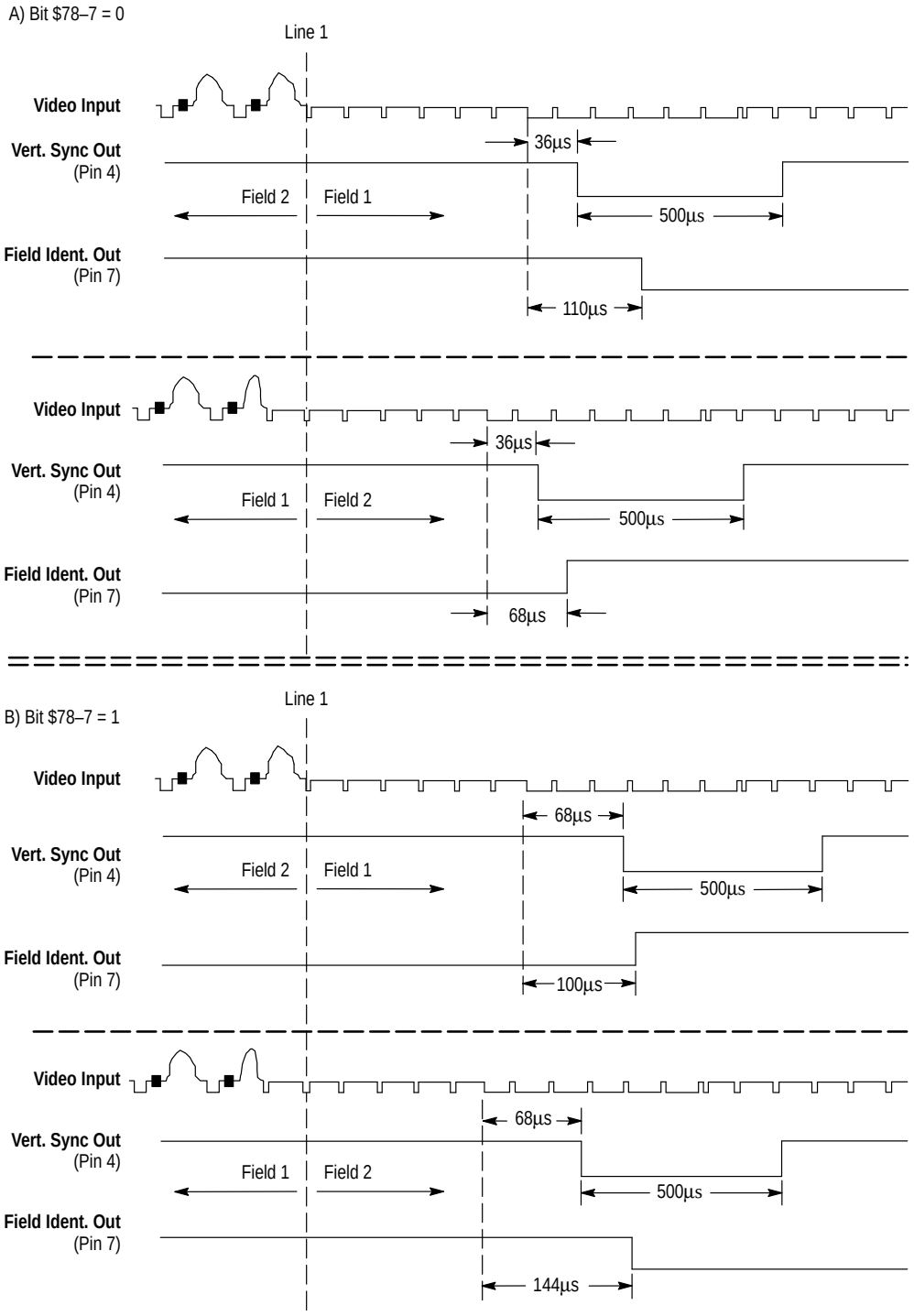
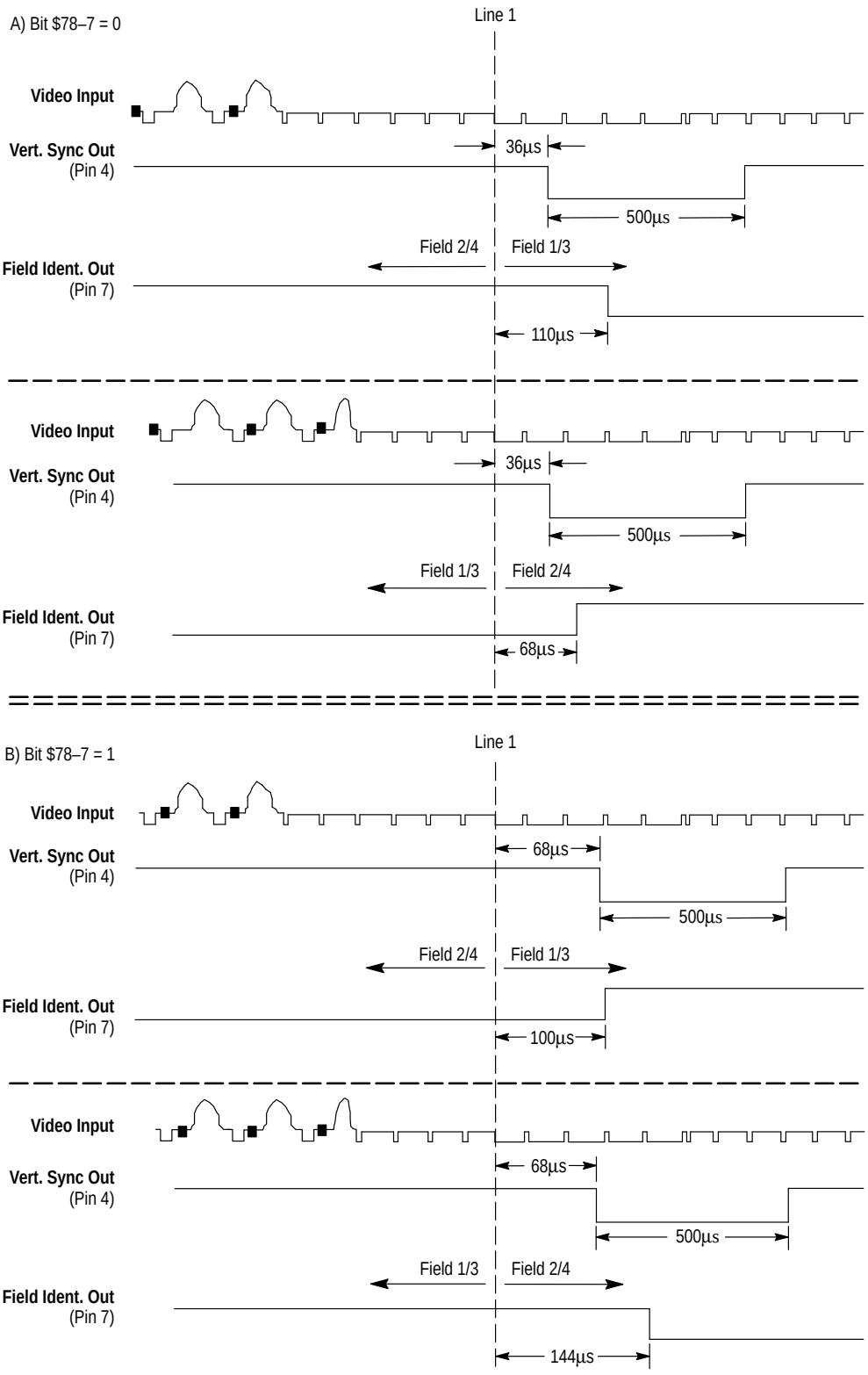


**Figure 34. Vertical Timing (PAL System)**



## FUNCTIONAL DESCRIPTION

### Introduction

The MC44011, a member of the MC44000 Chroma 4 family, is a composite video decoder which has been tailored for applications involving multimedia, picture–in–picture, and frame storage (although not limited to those applications). The first stage of the MC44011 provides color difference signals (R–Y, B–Y, and Y) from one of two (selectable) composite video inputs, which are designed to receive PAL, NTSC, and S–VHS (Y,C) signals. The second stage provides either RGB or YUV outputs from the first stage's signals, or from a separate (internally selectable) set of RGB inputs, permitting an overlay function to be performed. Adjustments can be made to saturation; hue; brightness; contrast; brightness balance; contrast balance; U and V bias; subcarrier phase; and color difference gain ratio.

The above mentioned video decoding sections provide the necessary luma/delay function, as well as all necessary filters for sound traps, luma/chroma separation, luma peaking, and subcarrier rejection. External tank circuits and luma delay lines are not needed. For PAL applications, the MC44140 chroma delay line provides the necessary line–by–line corrections to the color difference signals required by that system.

The MC44011 provides a pixel clock to set the sampling rate of external A/D converters. This pixel clock, and other horizontal frequency related output signals, are phase–locked to the incoming sync. The VCO's gain is adjustable for optimum performance. The MC44011 also provides vertical sync and field identification (Field 1, Field 2) outputs.

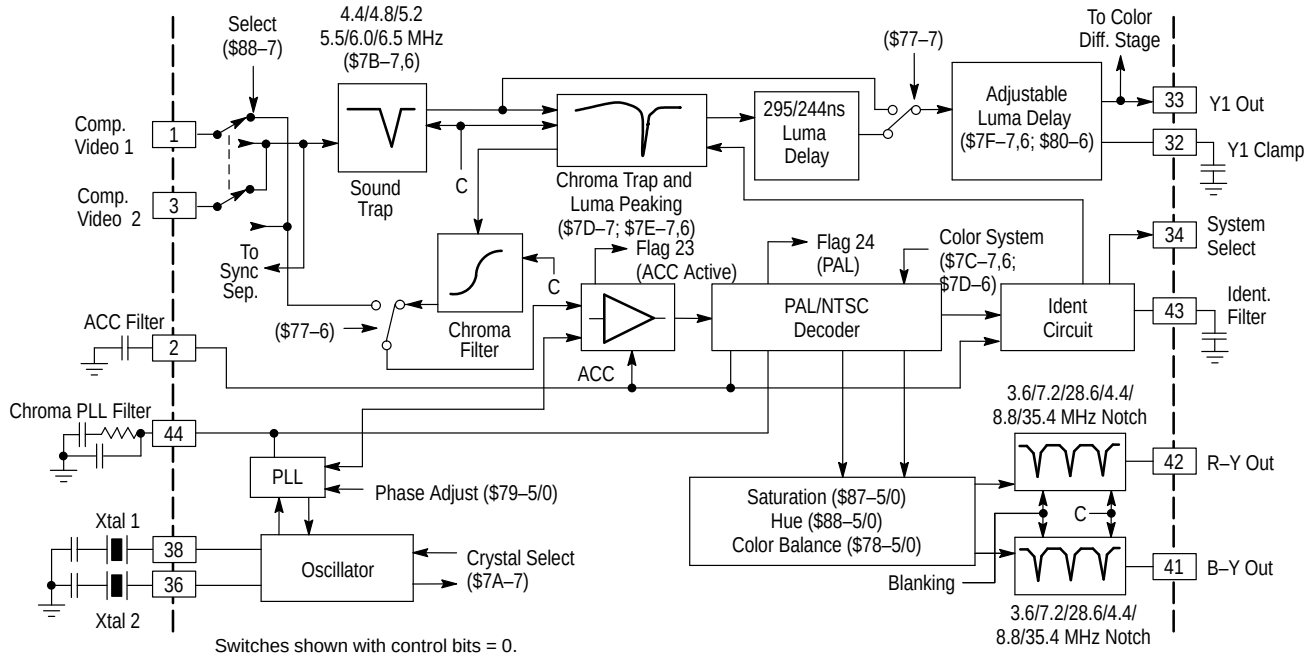
Selection of the various inputs, outputs, and functions, as well as the adjustments, is done by means of a two–wire $I^2C$ interface. The basic procedure requires the microprocessor system to read the internal flags of the MC44011, and then set the internal registers appropriately. This $I^2C$ interface eliminates the need for manual controls (potentiometers) and external switches. All of the external components for the MC44011, except for the two crystals, are standard value resistors and capacitors, and can be non–precision.

*(The DACs mentioned in the following description are 6–bits wide. The settings mentioned for them are given in decimal values of 00 to 63. These are not hex values.)*

### PAL/NTSC/S–VHS Decoder

A block diagram of this decoder section is shown in Figure 35. This section's function is to take the incoming composite video (at Pins 1 or 3), separate it into luma and chroma information, determine if the signal is PAL or NTSC (for the flags), and then provide color difference and luma signals at the outputs. If the input is S–VHS, the luma/chroma separation is bypassed, but the other functions are still in effect.

**Figure 35. PAL/NTSC/S–VHS Decoder Block Diagram**



**Inputs**

The inputs at Pins 1 and 3 are high impedance inputs designed to accept standard 1.0 Vpp positive video signals (with negative going sync). The inputs are to be capacitor–coupled so as not to upset the internal dc bias. When normal composite video is applied, the desired input is selected by Bit $88–7. Bits $77–6 and $77–7 must be set to 0 so that their switches are as shown in Figure 35. The selected signal passes through the sound trap, and is then separated by the chroma trap and the chroma (high pass) filter.

When S–VHS signals (Y,C) are applied to the two inputs, Bit $88–7 is used to direct the luma information to the sound trap, and the chroma information to the ACC circuit (Bit $77–6 must be set to a Logic 1). Bit $77–7 is normally set to a Logic 1 in this mode to bypass the first luma delay line and the chroma trap, but it can be left 0 if the additional delay is desired.

**Sound Trap**

The sound trap will filter out any residual sound subcarrier at the frequency selected by control bits T1 and T2 according to Table 3. The accuracy of the notch frequency is directly related to the selected crystal frequency.

**Table 3. Sound Trap Frequency**

| Crystal Frequency | T1 ($7B–7) | T1 ($7B–6) | Notch Frequency |
|---|---|---|---|
| 17.73 MHZ | 0 | 0 | 6.5 MHz |
| | 0 | 1 | 5.5 + 5.75 MHz |
| | 1 | 0 | 6.0 MHz |
| | 1 | 1 | 5.5 MHz |
| 14.32 MHz | 0 | 0 | 5.25 MHz |
| | 0 | 1 | 4.44 + 4.64 MHz |
| | 1 | 0 | 4.84 MHz |
| | 1 | 1 | 4.44 MHz |

Code 01 (for T1, T2) is used to widen the band rejection where stereo is in use. Typical rejection is 30 dB.

**ACC and PAL/NTSC Decoder**

The chroma filter bandpass characteristics (3.58 or 4.43 MHz) is determined by the selected crystal. The output of the chroma filter is sent to the ACC circuit which detects the burst signal, and provides automatic gain control once the crystal oscillator has achieved phase lock–up to the burst. The dc voltage at Pin 2 is ≈1.5 to 2.0 V. This will occur if the burst amplitude exceeds 30 mVpp, and if the correct crystal is selected (Bit $7A–7). A 17.734472 MHz crystal is required for PAL, and a 14.31818 MHz crystal is required for NTSC. When Flag 23 is high, it indicates that the crystal's PLL has locked up, and the ACC circuit is active, providing automatic gain control. A small amount of phase adjustment (≈ ± 5°) of the crystal PLL, for color correction, can be made with control DAC $79–5/0. Pin 2 is the filter for the ACC loop, and Pin 44 is the filter for the crystal oscillator PLL.

The PAL/NTSC decoder then determines if the signal is PAL or NTSC by looking for the alternating phase characteristic of the PAL burst. When Flag 24 is high, PAL has been detected. Bits SSA, SSB, SSC, and SSD (Table 4) must then be sent to the decoder to set the appropriate decoding method.

**Table 4. Color System Select**

| SSA ($7C–6) | SSB ($7D–6) | SSC ($7C–7) | SSD ($7A–6) | Color System |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Not Used |
| 0 | 1 | 0 | 0 | PAL |
| 1 | 0 | 0 | 0 | NTSC |
| 1 | 1 | 0 | 0 | Color Kill |
| X | X | 1 | 0 | External |

Upon receiving the SSA to SSD bits, the decoder provides the correct color difference signals, and with the Identification circuit, provides the correct level at the System Select output (Pin 34). This output is used by the MC44140 delay line.

The color kill setting (SSA = SSB = 1) should be used when the ACC flag is 0, when the color system cannot be properly determined, or when it is desired to have a black–and–white output (the ACC circuit and flag will still function if the input signal has a burst signal). The "External" setting (SSC = 1) is used when an external (alternate) source of color difference signals are applied to the MC44140 delay line. (See Miscellaneous Applications Information for more details.)

**Color Difference Controls and Outputs**

The color difference signals (R–Y, B–Y) from the PAL/NTSC decoder are directed to the saturation, hue and color balance controls, and then through a series of notch filters before being output at Pins 41 and 42. Blanking and clamping are applied to these outputs.

The saturation control DAC($87–5/0) varies the amplitude of the two signals from 0 Vpp (DAC setting = 00), to a maximum of ≈1.8 Vpp (at a DAC setting of 63). The maximum amplitude (without clipping) is ≈1.5 Vpp, but a nominal setting is ≈1.3 Vpp at a DAC setting of 15.

The hue control ($88–5/0) varies the relative amplitude of the two signals to provide a hue adjustment. The nominal setting for this DAC is 32.

The color balance control ($78–5/0) provides a fine adjustment of the relative amplitude of the two outputs. This provides for a more accurate color setting, particularly when NTSC signals are decoded. The nominal setting for this DAC is 32, and should be adjusted before the hue control is adjusted.

The notch filters provide filtering at the color burst frequency, and at 2x and 8x that frequency. Additionally, blanking and clamping (derived from the horizontal PLL) are applied to the signals at this stage. The nominal output dc level is ≈ 2.0 to 2.5 Vdc, and the load applied to these outputs should be >10 kΩ. Sync is not present on these outputs.

### Luma Peaking, Delay Line, and Y1 Output

When composite video is applied, the luma information extracted in the chroma trap is then applied to a stage which allows peaking at ≈ 3.0 MHz with the 17.7 MHz crystal (≈ 2.2 MHz with the 14.3 MHz crystal). The amount of peaking at Y1 is with respect to the gain at the minimum peaking value (P1, P2, P3 = 111), and is adjustable with Bits $7D–7, and $7E–7,6 according to Table 5.

The luma delay lines allow for adjustment of that delay so as to correspond to the chroma delay through this section. Table 6 indicates the amount of delay using the D1–D3 bits ($7F–7,6, and $80–6). The delay indicated is the total delay from Pin 1 or 3 to the Y1 output at Pin 33. The amount of delay depends on whether Composite Video is applied, or YC signals (S–VHS) are applied.

The output impedance at Y1 is ≈ 300 Ω, and the black level clamp is at ≈ +1.1 V. Sync is present on this output. Y1 is also internally routed to the color difference stage.

**Table 5. Luma Peaking**

| P1 ($7D–7) | P2 ($7E–6) | P3 ($7E–7) | Y1 Peaking |
|---|---|---|---|
| 0 | 0 | 0 | + 9.5 dB |
| 0 | 0 | 1 | + 8.5 |
| 1 | 0 | 0 | + 7.7 |
| 1 | 0 | 1 | + 6.5 |
| 0 | 1 | 0 | + 5.3 |
| 0 | 1 | 1 | + 3.8 |
| 1 | 1 | 0 | + 2.2 |
| 1 | 1 | 1 | 0 |

17.7 MHz Crystal, 6.5 MHz Sound Trap, Comp. Video Mode

**Table 6. Luma Delay**

| D1 ($7F–6) | D2 ($80–6) | D3 ($7F–7) | 14.3 MHz Crystal | | 17.7 MHz Crystal | |
|---|---|---|---|---|---|---|
| | | | Comp. Video ($77–7 = 0) | S–VHS ($77–7 = 1) | Comp. Video ($77–7 = 0) | S–VHS ($77–7 = 1) |
| 0 | 0 | 0 | 690 ns | 395 ns | 594 ns | 350 ns |
| 0 | 0 | 1 | 760 | 465 | 650 | 406 |
| 0 | 1 | 0 | 830 | 535 | 707 | 463 |
| 0 | 1 | 1 | 900 | 605 | 763 | 519 |
| 1 | 0 | 0 | 970 | 675 | 819 | 575 |
| 1 | 0 | 1 | 1040 | 745 | 876 | 632 |
| 1 | 1 | 0 | 970 | 675 | 819 | 575 |
| 1 | 1 | 1 | 1040 | 745 | 876 | 632 |

### Color Difference Stage and RGB/YUV Outputs

A block diagram of this section is shown in Figure 36. This section's function is to take the color difference input signals (Pins 30,31), or the RGB inputs (Pins 26 to 28), and output the information at Pins 20 to 22 as either RGB or YUV.

The inputs (on the left side of Figure 36) are analog RGB, or color difference signals (R–Y and B–Y) with Y1 or Y2 as the luma component. Pin 25 (Fast Commutate) is a logic level input, used in conjunction with $\overline{\text{RGB EN}}$ (Bit $80–7), to select the RGB inputs or the color difference inputs. The outputs (Pins 20 to 22) are either RGB or YUV, selected with Bit $82–7. The bit numbers adjacent to the various switches and gates indicate the bits used to control those functions. Table 7 indicates the modes of operation.

**Table 7. Color Difference Input/Output Selection**

| FC | $\overline{\text{RGB EN}}$ $80–7 | YX EN $82–6 | YUV EN $82–7 | Function |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | RGB inputs, RGB outputs, no saturation control |
| 1 | 0 | 1 | 0 | RGB inputs, RGB outputs, with saturation control |
| 1 | 0 | 1 | 1 | RGB inputs, YUV outputs, with saturation control |
| 1 | 0 | 0 | 1 | Not usable |
| FC Low and/or RGB EN Hi | | X | 0 | R–Y, B–Y inputs, RGB outputs. Y1 or Y2 must be selected |
| FC Low and/or RGB EN Hi | | X | 1 | R–Y, B–Y inputs, YUV outputs. Y1 or Y2 must be selected |

In addition to Table 7, the following guidelines apply:

a) To select the RGB inputs, both FC must be high and RGB EN must be low. Therefore, the RGB inputs can be selected either by the $I^2C$ bus by leaving FC permanently high, or by the FC input by leaving Bit $80–7 permanently low. For overlay functions, where high speed, well controlled switching is necessary, the FC pin must be the controlling input.

b) When the R–Y, B–Y inputs are selected, either Y1 or Y2 must be selected, and the other must be deselected. The YX input is automatically disabled in this mode.

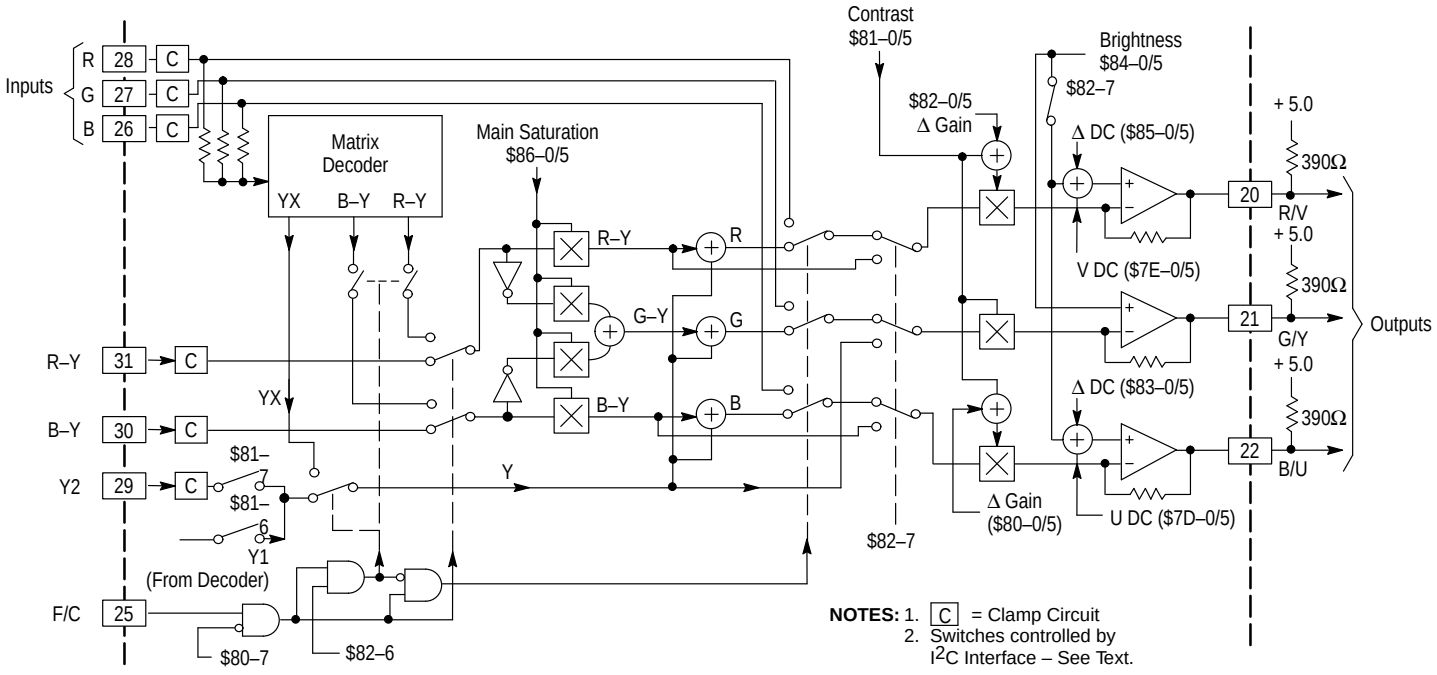
c) In applications where the color difference inputs are obtained from the NTSC/PAL decoder (from a composite video signal), Y1 is used. The Y2 input is normally used where alternately sourced color difference signals are applied, either through the MC44140 delay line, or through other external switching to Pins 30 and 31.

In Figure 36, the bit numbers followed by "– 0/5" indicate DAC operated controls (contrast, brightness, etc.), which are controlled by the $I^2C$ bus. The DACs have 6–bit resolution, allowing 64 adjustment steps. Table 8 provides guidelines on the DAC operation.

**Table 8. DAC Operation – Color Difference Section**

| Function | Bits | RGB Outputs ($82–7 = 0) | YUV Outputs ($82–7 = 1) |
|---|---|---|---|
| Brightness | $84–0/5 | Affects dc black and maximum levels of the three outputs, but not the clamp level, nor the amplitude. | Affects dc black and white levels of the Y output only, but not the clamp level, nor the amplitude. |
| Δ DC – Red<br>Δ DC – Blue | $85–0/5<br>$83–0/5 | Fine tune the Red and Blue brightness levels. | Allows a small amount of color tint control (not to be confused with hue). |
| Contrast | $81–0/5 | Provides gain adjustment (black–to–white) of the three outputs. | Provides gain adjustment of the three outputs. |
| Δ Gain – Red<br>Δ Gain – Blue | $82–0/5<br>$80–0/5 | Fine tune the Red and Blue contrast levels. | Fine tune of the U and V gain levels. |
| V DC<br>U DC | $7E–0/5<br>$7D–0/5 | Must be set to 00. | Should nominally be set to 32. This sets the dc level of the U and V outputs at ≈ mid–scale. |
| Main Saturation | $86–0/5 | Affects color saturation, except when the RGB inputs bypass this section (YX EN = 0). | Affects color saturation levels of the UV outputs. Does not affect the Y output. |

**Figure 36. Color Difference Stage and Outputs**



The RGB and Y2 inputs are designed to accept standard 1.0 Vpp analog video signals. They are not designed for TTL level signals. The color difference inputs are designed to accept signals ranging up to 1.8 Vpp. All signals are to be capacitor–coupled as clamping is provided internally. Input impedance at these six pins is high.

For applications involving externally supplied color difference signals, sync can be supplied on the luma input (Y2), or it can be supplied separately at the RGB inputs. Where the color difference signals are obtained from the NTSC/PAL decoder, sync is provided to this section on the internal Y1 signal. See Sync Separator section for more details on injecting sync into the MC44011.

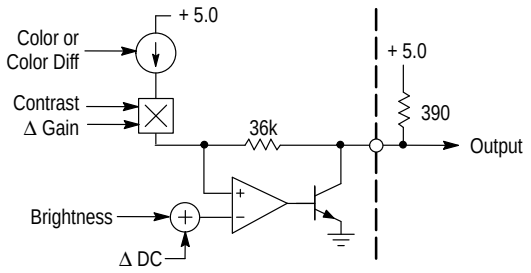
Sync is present on all three outputs in the RGB mode, and on the Y output only (Pin 21) in the YUV mode.

The Fast Commutate input (FC, Pin 25) is a logic level input with a threshold at ≈ 0.5 V. Input impedance is ≈ 67 kΩ, and the graph of Figure 24 shows the input current requirements. Propagation delay from the FC pin to the RGB/YUV outputs is ≈ 50 ns when enabling the RGB inputs, and ≈ 90 ns when disabling the inputs. (See Figure 29 Fast Commutate Timing diagram.) If Pin 25 is open, that is equivalent to a Logic 1, although good design practices dictate that inputs should never be left open. The voltage on this pin should not be allowed to go more the 0.5 V above $V_{CC2}$ or below ground.

The three outputs (Pins 20 to 22) are open–collector, requiring an external pull–up. A representative schematic is shown in Figure 37.

The output amplitude can be varied from 100 mVpp to 3.0 Vpp by use of the contrast and saturation controls. Any output load to ground should be kept larger than 1.0 kΩ. In the RGB mode, DACs $7D and $7E should be set to 00, which results in clamping levels of ≈ +1.4 Vdc. In the YUV mode, DACs $7D and $7E should be set to 00, which results in clamping levels of ≈ +1.4 Vdc. In the YUV mode, the DACs should be set to 32 to bias the U and V outputs to ≈ +2.3 V. The Y output clamp will remain at ≈ +1.4 V in the YUV mode.

**Figure 37. Output Stage**




**Horizontal PLL (PLL1)**

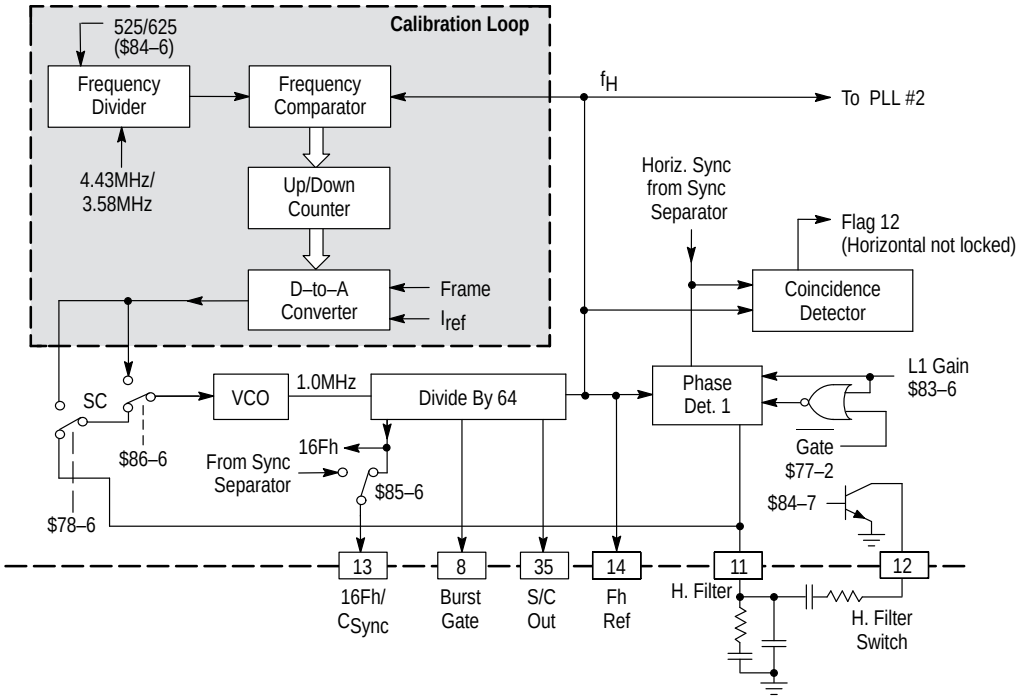
PLL1 (shown in Figure 38) provides several outputs which are phase–locked to the incoming horizontal sync. In normal operation, the two switches at the left side of Figure 38 are as shown, and (usually) the transistor at Pin 12 is off.

The phase detector compares the incoming sync (from the sync separator) to the frequency from the ÷ 64 block. The phase detector's output, filtered at Pin 11, controls the VCO to set the correct frequency (≈1.0 MHz) so that the output of the ÷ 64 is equal to the incoming horizontal frequency.

The line–locked outputs are:

1) **Fh Ref** (Pin 14) – A square wave, TTL levels, at the horizontal frequency, and phase–locked to the sync source according to the timing diagram of Figures 25 and 27.
2) **Burst Gate** (Pin 8) – This is a positive going pulse, TTL levels, coincident with the burst signal. See the timing diagram of Figures 25 and 27.

**Figure 38. Horizontal PLL (PLL1)**



3) **Sandcastle Output** (Pin 35) – This is a multilevel output, at the horizontal frequency, used by the MC44140 delay line. See the timing diagram of Figures 25 and 27.
4) **16Fh/$C_{Sync}$** (Pin 13) – This is a dual purpose output, TTL levels, user selectable. When Bit $85–6 is set to 0, Pin 13 is a square wave at 16x the horizontal frequency (250 kHz for PAL, ≈ 252 kHz for NTSC). When Bit $85–6 is set to 1, Pin 13 is negative composite sync, derived from the internal sync separator. See the timing diagram of Figures 25 and 27.

The first three outputs mentioned above, and Pin 13 when set to 16 Fh, are consistent, and do not change duty cycle or wave shape during the vertical sync interval. These four outputs will also be present regardless of the presence of a video signal at the selected input.

When Pin 13 is set to $C_{Sync}$ output, it follows the incoming composite sync format. If there is no video signal present at the selected input, this output will be a steady logic high.

Loading on these pins should not be less than 2.0 kΩ to either ground or + 5.0 V.

Pin 11 is the filter for the PLL, and requires the components shown in Figure 38, and with the values shown in the application circuit of Figure 42. Pin 12 is a switch which allows the filtering characteristics at Pin 11 to be changed. Switching in the additional components (set $84–7 =1) increases the filter time constant, permitting better performance in the presence of noisy signals.

The gain of the phase detector may be set high or low, depending on the jitter content of the incoming horizontal frequency, by using Bit $83–6. Broadcast signals usually have a very stable horizontal frequency, in which case the low gain setting ($83–6 = 0) should be used. When the video source is, for example, a VCR, the high gain setting may be preferable to minimize instability artifacts which may show up on the screen.

The gating function ($77–2) provides additional control where the stability of the incoming horizontal frequency is in question. With this bit set to 0, gating is in effect, causing the phase detector to not respond to the incoming sync pulses during the vertical interval. This reduces disturbances in this PLL due to the half–line pulses and their change in polarity. The gating may be disabled by setting this bit to 1 where the timing of the incoming sync is known to be stable. The gating cannot be enabled if the phase detector gain is set high ($83–6 = 1).

### Calibration Loop

The calibration loop (upper left portion of Figure 38) maintains a near correct frequency of this PLL in the absence of incoming sync signals. This feature minimizes re–adjustment and lock time when sync signals are re–applied. The calibration loop is similar to the PLL function, receiving one frequency from the crystal (either 4.43 MHz or 3.58 MHz) divided down to a frequency similar to the standard horizontal frequency. Bit $84–6 is used to set the frequency divider to the correct ratio, depending on which crystal is selected (see Table 9). The output of the frequency comparator operates an up/down counter, which in turn sets the D–to–A converter to drive the VCO through switch Sc. The resulting frequency at the output of the divide–by–64 block is then fed to the frequency comparator to complete the loop.

When a sync signal is not present at Phase Detector #1, and at the Coincidence Detector, as indicated by the coincidence detector's output (Flag 12), Bit $78–6 should be set to 0. This will cause the switch (Sc) to transfer to the D–to–A converter for two lines (lines 4, 5) in each vertical field, and will maintain the PLL1 at a frequency near the standard horizontal frequency (between 14 to 16 kHz). When lock to an incoming sync is established, Bit $78–6 may be set to 1, disabling the periodic recalibration function, or it may be left set to 0.

If a more accurate horizontal frequency is desired in the absence of an input signal, Bit $86–6. can be set to 1 (and Bit $84–6 set according to Table 9). This holds the horizontal frequency to ≈ 15.7 kHz. In this mode, Flag 12 will stay 0, as the PLL will not be able to lock–up to a newly applied external signal. To reset the system, set $86–6 to 0, write $00 to register $00, and then check Flag 12 to determine when the loop locks to an incoming signal.

**Table 9. Calibration Loop**

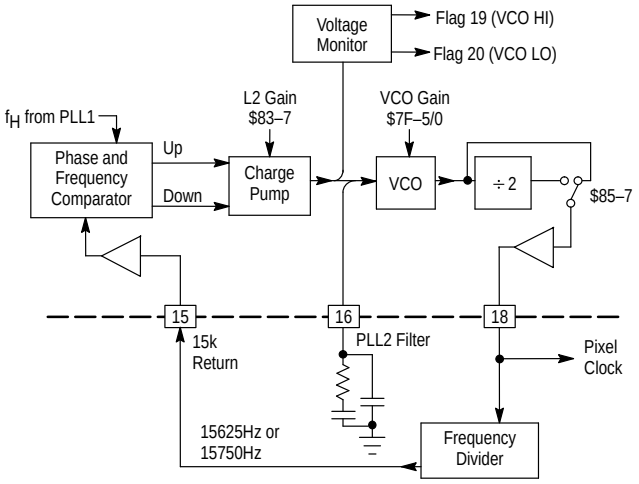
| Crystal | Set Bit $84–6 to |
|---|---|
| 14.3 MHz | 1 |
| 17.7 MHz | 0 |

On initial power up, Bit $86–6 (PLL1 EN) is automatically set to 1, engaging the calibration loop continuously. This condition will remain until this bit is set to 0, and $00 is written to register $00, as part of the initialization routine.

### Pixel Clock PLL (PLL2)

The second PLL, depicted in Figure 39, generates a high frequency clock which is phase–locked to the horizontal frequency.

**Figure 39. Pixel Clock PLL (PLL2)**



The phase and frequency comparator receive inputs from PLL1 ($f_H$, the horizontal frequency), and the frequency returned from the external divider. Any difference between these two signals causes the Up or Down output to change the charge pump's timing. The charge pump output is composed of two equal current sources which alternately source and sink current to the filter at Pin 16. The voltage at Pin 16 (which is the input to the VCO) is therefore determined by the relative timing of those two current sources, and the filter characteristics. A coarse control of the loop gain is set with Bit $83–7. Low gain is obtained by setting this bit to a 1, which sets the charge pump's output current sources to ≈ ± 20 μA. Setting this bit to 0 sets the current sources to ≈ ± 50 μA, or high gain.

Depending on the output frequency desired, and whether or not a 50–50 square wave is needed at the pixel clock, the ÷2 may be engaged (Bit $85–7). Generally, the ÷ 2 should not be engaged for high frequencies, and should be engaged for low frequencies, so as to keep the VCO's input voltage in a comfortable range (between 1.7 and 3.3 V). If the input voltage is outside this range, Flag 19 or 20 will switch high, indicating the need to fine tune the VCO's gain (control DAC $7F). The usable adjustment range for this DAC is 00 to ≈ 50. Settings of 51 to 62 will generally produce non–square wave outputs, and can be unstable. A setting of 63 will shut off the VCO, which should be done if the pixel clock is not used. When not used, Pin 18 will be at a constant low level.

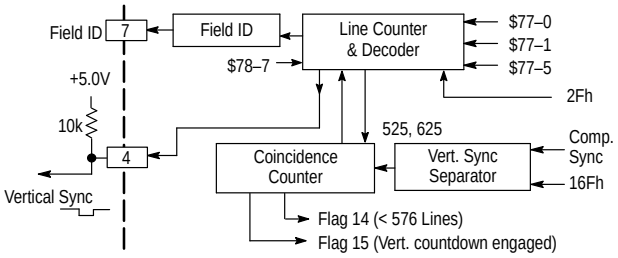
The pixel clock frequency is equal to the horizontal frequency ($f_H$) x the frequency divider ratio. The frequency divider can be made up of programmable counters (e.g. MC74F161A Applications Information), or it can be integrated into another device (e.g., an ASIC). The returned signal to Pin 15 must be TTL/CMOS logic levels, and must have a low time of > 200 ns. The phase comparator will phase–lock the falling edge of the returned signal with the rising edge of the $f_H$ signal at Pin 14 (see Figure 32).

**Vertical Decoder**

The vertical decoder section, depicted in Figure 40, provides a vertical sync pulse and a field identification signal, as well as flags which indicate if vertical lockup has occurred, and if the number of horizontal lines per frame is greater or less than 576.

Inputs to this section consists of the composite sync from the sync separator, and horizontal related signals from the horizontal PLL (PLL1).

**Figure 40. Vertical Decoder**




The sync output (Pin 4) is an active low signal which starts after the horizontal half–line sync pulses change polarity (see Figures 33 and 34). The pulse width is nominally 500 μs for both PAL and NTSC signals. The position of this sync pulse's leading edge can be altered slightly with Bit $78–7, but this does not change the pulse width. Since the pulse width is generated digitally by counters, it will not vary with temperature, supply voltage, or manufacturing distribution. The sync output is an open–collector NPN output, requiring an external pull–up resistor. Minimum value for the pull–up is 1.0 kΩ, with 10 kΩ recommended for most applications.

Flag 14 (< 576 lines) is derived from the counter which compares the number of horizontal lines in each frame with a preset value of 576. This flag can be used externally to help determine whether PAL or NTSC signals are being provided to the MC44011. Flag 15 (Vertical countdown engaged) indicates that the vertical decoder has locked–up to the incoming composite sync information for eight consecutive fields (CB1, CA1 = 11).

The operation of the vertical decoder is controlled by Bits $77–0 and $77–1, according to Table 10.

**Table 10. Vertical Decoder Mode**

| CB1 ($77–1) | CA1 ($77–0) | Vertical Sync Mode |
|---|---|---|
| 0 | 0 | Force 625 |
| 1 | 0 | Force 525 |
| 0 | 1 | Injection Lock |
| 1 | 1 | Auto–Count |

The Injection Lock mode has a quicker response time, but less noise immunity, than the Auto–Count mode, and is normally used when attempting to lock–up to a new signal (such as when changing video input selection). Flag 15 will not switch high when in this mode. The Auto–Count mode, having a higher noise immunity, should be set once the horizontal PLL is locked–up (by reading Flag 12), and then Flag 15 should be checked after 8 fields for vertical lock–up.

The modes designated Force 525 and Force 625 can be used for those cases where it is desired to force the vertical sync pulse to occur twice every 525 or 625 lines, regardless of the incoming signal. In either of these modes, the MC44011's vertical section will not lock–up to the vertical sync information contained in the incoming composite video signal. If there is no incoming video signal, the vertical sync will still occur every 525 or 625 lines generated by the horizontal PLL. Flag 14 will indicate the number of lines selected, and Flag 15 will be a steady high.

Bit $77–5 (FSI) is used only in the PAL mode to select the vertical sync output rate. With this bit set to 0, the vertical sync pulses will be synchronized with the composite vertical sync input (every 20 ms). With this bit set to 1, the MC44011 will add a second vertical output sync pulse 10 ms after the one occurring at the vertical interval, giving a vertical sync rate of 100 Hz.

The Field ID output (Pin 7) indicates which field is being processed when interlaced signals are applied, but the polarity depends on Bit $78–7. Table 11 indicates Pin 7 output. When non–interlaced signals are being processed, Pin 7 will be a constant high level when $78–7 is set to 1, and will be a constant low level when $78–7 is set to a 0. Loading on Pin 7 should not be less than 2.0 kΩ to either ground or + 5.0 V. Figures 33 and 34 indicate the timing.

**Table 11. Field ID Output**

| 36/68 μs ($78–7) | Field | Field ID (Pin 7) |
|---|---|---|
| 1 | 1 | High |
| 1 | 2 | Low |
| 0 | 1 | Low |
| 0 | 2 | High |

**Sync Separator**

The sync separator block provides composite sync information to the horizontal PLL, and to various other blocks within the MC44011 from one of several sources. It also provides composite sync output at Pin 13 when Bit $85–6 = 1. The sync source is selectable via the I2C bus according to Table 12.

**Table 12. Sync Source**

| $V_{in}$ Sync ($86–7) | Y2 Sync ($87–7) | RGB Sync ($88–6) | Sync Source |
|---|---|---|---|
| 0 | 0 | 0 | None |
| 0 | 0 | 1 | RGB (Pins 26 – 28) |
| 0 | 1 | 0 | Y2 (Pin 29) |
| 1 | X | X | Comp. Video (Pins 1, 3) |

Setting Bit $86–7 to a 1 overrides the other bits, thereby deriving the sync from the composite video input (either Pin 1 or 3) selected by Bit $88–7.

When RGB is selected, sync information on Pins 26 to 28 is used. Sync may be applied to all three inputs, or to any one with the other two AC grounded. If RGB signals are applied to these pins, sync may be present on any one or all three.

When Y2 is selected, sync information on Pin 29 is used. The sync amplitude applied to any of the above pins must be greater than 100 mV, and it must be capacitor coupled.

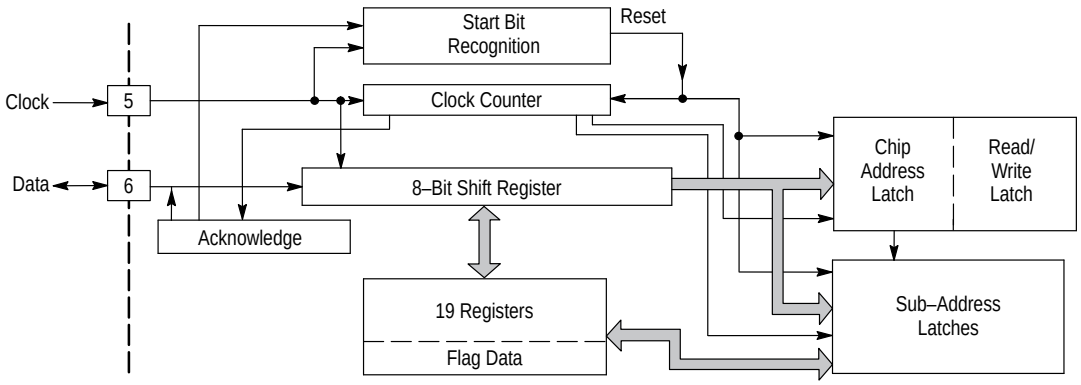
This system allows a certain amount of flexibility in using the MC44011, in that if the sync information is not present as part of the applied video signals, sync may be applied to another input. In other words, the input selected for the sync information need not be the same as the input selected for the video information.

## SOFTWARE CONTROL OF THE MC44011

**I2C Interface**

Communication to and from the MC44011 follows the I2C interface arrangement and protocol defined by Philips Corporation. In simple terms, I2C is a two line, multimaster bidirectional bus for data transfer. See Appendix C for a description of the I2C requirements and operation. Although an I2C system can be multimaster, the MC44011 never functions as a master.

**Figure 41. I2C Bus Interface and Decoder**




The MC44011 has a write address of $8A, and a flag read address of $8B. It requires that an external microprocessor read the internal flags, and then set the appropriate registers. The MC44011 does not do any automatic internal switching when applied video signals are changed. A block diagram of the I2C interface is shown in Figure 41. Since writing to the MC44011's registers can momentarily create jitter and other undesirable artifacts on the screen, writing should be done only during vertical retrace (before line 20). Reading of flags, however, can be done anytime.

**Write to Control Registers**

Writing should be done only during vertical retrace. A write cycle consists of three bytes (with three acknowledge bits):

1) The first byte is always the write address for the MC44011 ($8A).
2) The second byte defines the sub–address register (within the MC44011) to be operated on ($77 through $88, and $00).
3) The third byte is the data for that register.

Communication begins when a start bit (data taken low while clock is high), initiated by the master, is detected, generating an internal reset. The first byte is then entered, and if the address is correct ($8A), an acknowledge is generated by the MC44011, which tells the master to continue the communication. The second byte is then entered, followed by an acknowledge. The third byte is the operative data which is directed to the designated register, followed by a third acknowledge.

**Sub–Address Registers**

The sub–addresses of the 19 registers are at $77 through $88, and $00. Fourteen of the registers use Bits 0–5 to operate DACs which provide the analog adjustments. Most of the other bits are used to set/reset functions, and to select appropriate inputs/outputs. Table 13 indicates the assignments of the registers.

**Table 13. Sub–Address Register Assignments**

| Sub Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| $77 | S–VHS Y | S–VHS C | FSI | $\overline{\text{L2 GATE}}$ | $\overline{\text{BLCP}}$ | $\overline{\text{L1 GATE}}$ | CBI | CAI |
| $78 | 36/38 µs | Cal Kill | (R–Y)/(B–Y) adjust DAC | | | | | |
| $79 | HI | VI | Subcarrier balance DAC | | | | | |
| $7A | Xtal | SSD | | | | | | |
| $7B | T1 | T2 | | | | | | |
| $7C | SSC | SSA | | | | | | |
| $7D | P1 | SSB | Blue bias for YUV operation DAC | | | | | |
| $7E | P3 | P2 | Red bias for YUV operation DAC | | | | | |
| $7F | D3 | D1 | Pixel Clock VCO Gain adjust DAC | | | | | |
| $80 | $\overline{\text{RGB EN}}$ | D2 | Blue Contrast trim DAC | | | | | |
| $81 | Y2 EN | Y1 EN | Main Contrast DAC | | | | | |
| $82 | YUV EN | YX EN | Red Contrast trim DAC | | | | | |
| $83 | L2 Gain | L1 Gain | Blue Brightness trim DAC | | | | | |
| $84 | H Switch | 525/625 | Main Brightness DAC | | | | | |
| $85 | PClk/2 | C Sync | Red Brightness trim DAC | | | | | |
| $86 | $V_{in}$ Sync | $\overline{\text{PLL1 En}}$ | Main Saturation DAC (Color Difference section ) | | | | | |
| $87 | Y2 Sync | 0 | (R–Y)/(B–Y) Saturation balance DAC (Decoder section) | | | | | |
| $88 | V2/V1 | RGB Sync | Hue DAC | | | | | |
| $00 | Set to $00 to start Horizontal Loop if $88–6 = 0 | | | | | | | |

Table 14 is a brief explanation of the individual control bits. A more detailed explanation of the functions is found in the block diagram description of the text (within the Functional Description section). Table 15 provides an explanation of the DACs. Each DAC is 6 bits wide, allowing 64 adjustment steps. The proper sequence and control of the bits and DACs, to achieve various system functions, is described in the Applications Information section.

**Table 14. Control Bit Description**

| Control Bit | Name | Description |
|---|---|---|
| $77–7 | S–VHS–Y | Set to 0 for normal Composite Video inputs at V1 and/or V2 (Pins 1, 3). Set to 1 for S–VHS (YC) operation. When 1, the Y–input at the selected video input (V1 or V2, selected by Bit $88–7) bypasses the initial luma delay line, and associated luma/chroma filters and peaking. The signal passes through the second luma delay, adjustable with Bits D1–D3. Luma is output at Pin 33. |
| $77–6 | S–VHS–C | Set to 0 for normal Composite Video inputs at V1 and/or V2 (Pins 1, 3). Set to 1 for S–VHS (YC) operation. When 1, the chroma input at the non–selected video input (V1 or V2 by Bit $88–7) is directed to the ACC loop and PAL/NTSC detector. Color difference signals are then output at Pins 41 and 42. |
| $77–5 | FSI | Set to 0 for a Vertical Sync output rate of 50 Hz. Set to 1 for 100 Hz. Useable in PAL systems only. |
| $77–4 | $\overline{\text{L2 GATE}}$ | When set to 0, the pixel clock charge pump (PLL2) operation is inhibited during the Vertical Retrace to minimize momentary instabilities. When set to 1, PLL2 operation is not inhibited. |
| $77–3 | $\overline{\text{BLCP GATE}}$ | When 0, Vertical Gating of the black level clamp pulse during the Vertical Retrace occurs to minimize momentary instabilities. The Vertical Gating can be inhibited by setting this bit to 1. |
| $77–2 | $\overline{\text{L1 GATE}}$ | When set to 0, the horizontal PLL's phase detector (PLL1) operation is inhibited during the Vertical Retrace to minimize momentary instabilities. When set to 1, the phase detector is not inhibited. If PLL1 gain is high (Bit $83–6 = 1), gating cannot be enabled. |
| $77–1, 0 | CB1, CA1 | Sets the Vertical Timebase operating method according to Table 10. |
| $78–7 | 36/68 µs | When 0, the time delay from the sync polarity reversal within the Composite Sync to the leading edge of the Vertical Sync output (Pin 4) is 36 µs. When 1, the time delay is 68 µs. (See Figure 33 and 34). |
| $78–6 | CalKill | When 0, the Horizontal Calibration Loop is enabled for two lines (lines 4 and 5) in each field. When 1, the Calibration Loop is not engaged. Upon power–up, this bit is ineffective (Calibration Loop is enabled) until bit $86–6 is set to 0, and register $00 is set to $00. |
| $79–7 | HI | This bit is not used in the MC44011, and must be set to 1. |
| $79–6 | VI | This bit is not used in the MC44011, and must be set to 1. |
| $7A–7 | Xtal | When 0, the crystal at Pin 38 (17.7 MHz) is selected. When 1, the crystal at Pin 36 (14.3 MHz) is selected. |
| $7A–6 | SSD | This bit is not used in the MC44011, and must be set to 0. |
| $7B–7, 6 | T1, T2 | Used to set the Sound Trap Notch filter frequency according to Table 3. |
| $7C–7, 6 $7D–6 | SSC, SSA, SSB | Sets the NTSC/PAL decoder to the correct system according to Table 4. |
| $7D–7 $7E–7, 6 | P1, P2, P3 | Sets the Luma Peaking in the decoder section according to Table 5. (See text). |
| $7F–7, 6 $80–6 | D3, D1, D2 | Sets the Luma Delay in the decoder section according to Table 6. (See text). |
| $80–7 | $\overline{\text{RGB EN}}$ | When 0, permits the RGB inputs (Pins 26 to 28) to be selected with the Fast Commutate (FC) input (Pin 25). When 1, the FC input is disabled, preventing the RGB inputs from being selected. When the RGB inputs are selected, the Color Difference inputs (Pins 30, 31) are deselected. |
| $81–7 | Y2 EN | When 1, the Y2 Luma input (Pin 29) is selected. When 0, it is deselected. |
| $81–6 | Y1 EN | When 1, the Y1 Luma Signal (provided by the decoder section to the color difference section) is selected. When 0, it is deselected. |
| $82–7 | YUV EN | When 0, Pins 20 to 22 provide RGB output signals. When 1, those pins provide YUV output signals. |
| $82–6 | YX EN | Effective only when the RGB inputs are selected. When 0, the RGB inputs (Pins 26 to 28) are directed to the RGB outputs (Pins 20 to 22) via the Contrast and Brightness controls. When 1, the RGB inputs are directed through the Color Difference Matrix, allowing Saturation control in addition to the Brightness and Contrast controls. See Figure 36. |
| $83–7 | L2 Gain | When 0, the gain of the pixel clock VCO (PLL2) is high (50 µA). When 1, the gain is low (20 µA). |
| $83–6 | L1 Gain | When 0, the Horizontal Phase Detector Gain (PLL1) is low. When 1, the gain is high. |
| $84–7 | H Switch | When 0, Pin 12 is open. When 1, Pin 12 is internally switched to ground, allowing the PLL1 filter operation to be adjusted for noisy signals. |
| $85–7 | PClk/2 | When 0, the PLL2 VCO provides the Pixel Clock at Pin 18 directly. When 1, the VCO output is directed through a ÷ 2 stage, and then to Pin 18. |

**Table 14. Control Bit Description** (continued)

| Control Bit | Name | Description |
|---|---|---|
| $84–6 | 525/625 | This bit sets the division ratio from the crystal for the reference frequency for the Horizontal Calibration Loop. For NTSC systems, set to 1. For PAL systems, set to 0. |
| $85–6 | C Sync | When 0, Pin 13 will provide a square wave of ≈ 250 kHz (16 x Fh). When 1, Pin 13 provides a negative composite sync signal. See Figures 25, 27, 30, 31. |
| $86–7 | $V_{in}$ Sync | When 1, Composite Sync at the selected Video input (Pin 1 or 3) is used for all internal timing. When 0, the Sync source is selected by Bits $87–7 and $88–6. See Table 12. |
| $86–6 | PLL1 Enable | After power up, this bit must be set to 0, and then register $00 set to $00, to enable the Horizontal Loop (PLL1). Setting this bit to a 1 will disable the Horizontal Loop, and engages the Calibration Loop. |
| $87–7 | Y2 Sync | When 1, and $86–7 = $88–6 = 0, Composite Sync at the Y2 input (Pin 29) is used for all internal timing. When 0, the Sync source is selected by Bits $86–7 or $88–6. See Table 12. |
| $87–6 | 0 | This bit must always be set to 0. |
| $88–7 | V2/V1 | When Composite Video is applied, and this bit is 0, the Video 2 input (Pin 3) is directed to the Sound Trap. When 1, the Video 1 input (Pin 1) is selected. In S–VHS applications, when 0, Pin 3 is the Y (luma) input, and Pin 1 is the chroma input. When this bit is 1, Pin 1 is the luma input, and Pin 3 is the chroma input. |
| $88–6 | RGB Sync | When 1, and $86–7 = $87–7 = 0, Composite Sync at any or all of the RGB inputs (Pin 26 to 28) is used for all internal timing. When 0, the sync source is selected by Bits $86–7 or $87–7. See Table 12. |

**Table 15. Control DAC Description**

| Control Bits | Description |
|---|---|
| $78–5/0 | This DAC allows for a relative gain adjustment of the R–Y and B–Y outputs (Pins 41, 42) as a means of adjusting the color decoding accuracy. Nominal setting is 32. |
| $79–5/0 | Used to balance out reference errors of the color subcarrier, primarily for NTSC. Nominal setting is 32. Adjustment range is ≈ ± 5°. |
| $7D–5/0 | Used to set the U (Pin 22) dc bias level. When in the YUV mode ($82–7 = 1), this setting should nominally be 32. When in RGB mode, set to 00. |
| $7E–5/0 | Used to set the V (Pin 22) dc bias level. When in the YUV mode ($82–7 = 1), this setting should nominally be 32. When in RGB mode, set to 00. |
| $7F–5/0 | Used to fine tune the gain of the Pixel Clock VCO to obtain optimum performance without instabilities. A setting of 63 will shut off the VCO. Setting 50 to 62 provide non–square wave outputs, and can be unstable. As the setting is increased from 00 to 49, the gain is increased. Changing this register does not change the Pixel Clock frequency. |
| $80–5/0 | Used to fine tune the contrast of the Blue output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue. |
| $81–5/0 | Used to adjust the gain of the three outputs. In RGB mode this is the Contrast control. |
| $82–5/0 | Used to fine tune the contrast of the Red output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue. |
| $83–5/0 | Used to fine tune the brightness of the Blue output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue. |
| $84–5/0 | Used to adjust the brightness of the three RGB outputs. In YUV mode this DAC affects only Y output (Pin 21). |
| $85–5/0 | Used to fine tune the brightness of the Red output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue. |
| $86–5/0 | Used to adjust the saturation of the RGB/YUV outputs of the Color Difference section. |
| $87–5/0 | Used to adjust the saturation of the R–Y, B–Y outputs (Pins 41, 42) of the Decoder section. |
| $88–5/0 | Used to adjust the hue of the R–Y, B–Y outputs (Pins 41, 42). Nominal setting is 32. |
| $00–7/0 | This register must be set to 00, after Bit $86–6 is set to 0, to enable the Horizontal Loop (PLL1) after power up, or anytime when Bit $86–6 is set to 0 after having been a 1. |

The above DACs are 6–bits wide. The settings mentioned above, and in subsequent paragraphs are given in decimal values of 00 to 63. These are not hex values.

**Reading Flags**

A read cycle need not be restricted to the vertical interval, but may be done anytime. A flag read cycle consists of three bytes (with three acknowledge bits):

- The first byte is always the Read address for the MC44011 ($8B).
- The second and third bytes are the flag data.

Communication begins when a start bit (data taken low while clock is high), initiated by the master (not the MC44011), is detected, generating an internal reset. The first byte (address) is then entered, and if correct, an acknowledge is generated by the MC44011. The flag bits will then exit the MC44011 as two 8 bit bytes at clock cycles 10–17 and 19–26. The master (receiving the data) is expected to generate the acknowledge bits at clocks 18 and 27. The master must then generate the stop bit.

The MC44011 flags must be read on a regular basis to determine the status of the various circuit blocks. The MC44011 does not generate interrupts. It is recommended the flags be read once per field or frame. See Table 16 for a description of the flags.

**Table 16. Flag Description**

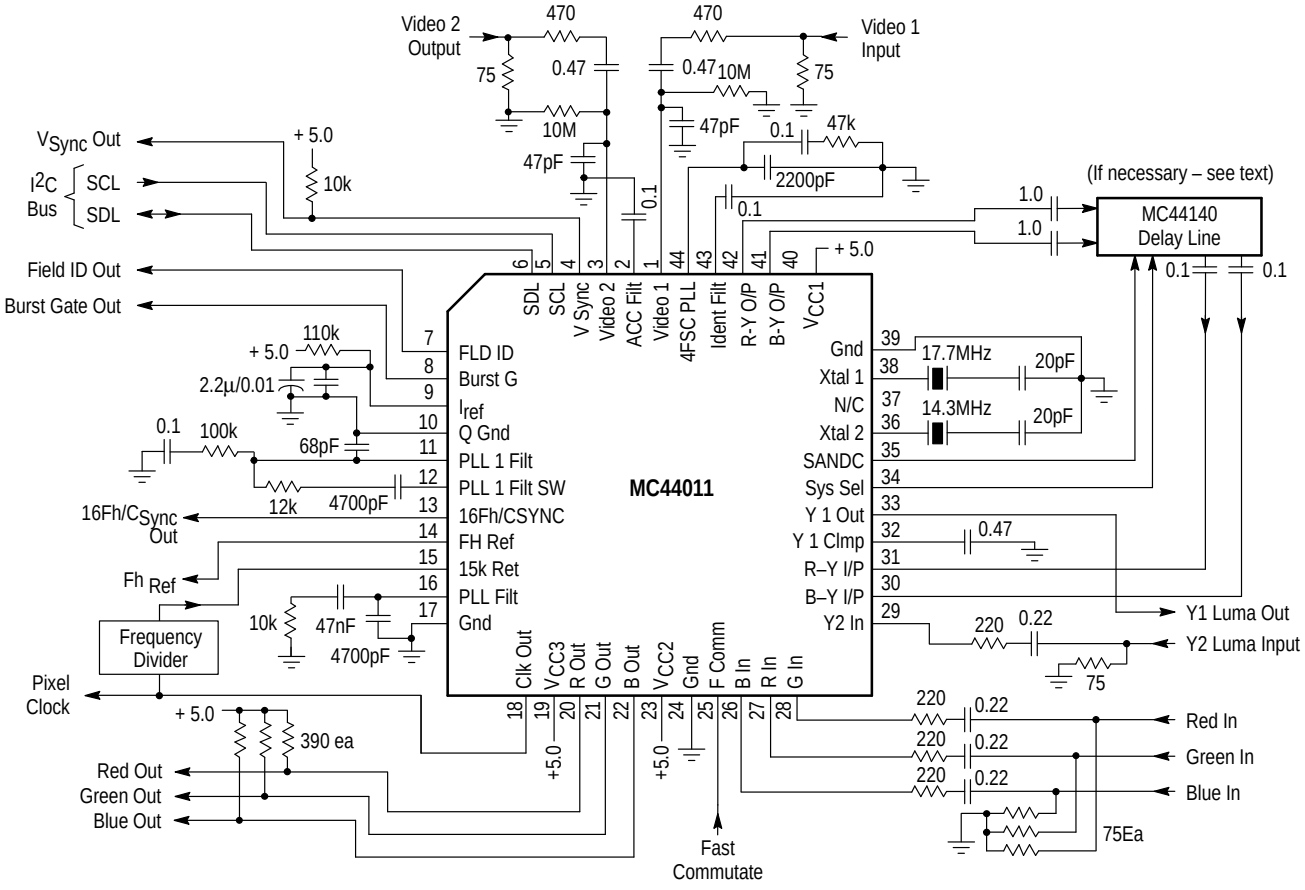
| Clock No. | Description (When Flag = 1) |
|---|---|
| 10 | Internally set to a Logic 1. |
| 11 | Horizontal Loop (PLL1) enabled, indicating the loop can be driven by the incoming sync. This bit will be low upon power up, and will change to a 1 after initialization of control Bit $86–6 and register $00. |
| 12 | Horizontal Loop (PLL1) not locked. Lack of incoming sync, or wrong sync source selection, or the wrong horizontal frequency, will cause the Coincidence Detector to indicate a “not locked” condition. |
| 13 | Internally set to Logic 0. |
| 14 | Less than 576 horizontal lines counted per frame. This flag helps determine the applied video system. When high, a 525 line system (NTSC) is indicated. When low, a 625 line system (PAL) is indicated. |
| 15 | Vertical Countdown engaged. When high, this flag indicates the Vertical Countdown section has successfully maintained lock for 8 consecutive fields, indicating therefor a successful vertical lock–up. This flag is low in the Injection Lock mode. |
| 16 | Internally set to a Logic 1. |
| 17 | Internally set to a Logic 1. |
| 18 | (Acknowledge pulse). |
| 19 | Pixel clock VCO control voltage too low (< 1.7 V at Pin 16). This indicates the VCO may not function correctly as the control voltage is near one end of its range. The DAC setting at register $7F–5/0 must be increased, and/or the ÷ 2 block must be selected (set $85–7 = 1), to clear this flag. |
| 20 | Pixel clock VCO control voltage too high (> 3.3 V at Pin 16). This indicates the VCO may not function correctly as the control voltage is near one end of its range. The DAC setting at register $7F–5/0 must be reduced, and/or the ÷ 2 block must be deselected (set $85–7 = 0) to clear this flag. This flag will be high if the VCO is off (DAC $7F = 63). |
| 21 | Internally set to a Logic 1. |
| 22 | Internally set to a Logic 0. |
| 23 | ACC Loop is active, indicating it is locked up to the color burst signal. The Color Burst amplitude must exceed 30 $mV_{pp}$, and the correct crystal selected, for lock–up to occur. |
| 24 | PAL system identified by the decoder, indicating the decoder recognizes the line–by–line change in the burst phase. When NTSC is applied, this flag is 0. |
| 25 | Not used. |
| 26 | Internally set to a Logic 0. |
| 27 | (Acknowledge pulse). |

## APPLICATIONS INFORMATION

### Design Procedure and PC Board Layout

The external components required by the MC44011 are shown in Figure 42. Except for the crystals, all the components are standard value resistors and capacitors, and can be non–precision. Table 17 describes the external components for each pin.

**Figure 42. Basic Functional Circuit**




### Crystal Specifications and Operation

The crystals used with the MC44011 should comply with Table 18 specifications.

**Table 18. Crystal Specifications**

| | |
|---|---|
| Frequency:<br>(4 x Subcarrier) | NTSC (14.31818 MHz)<br>PAL (17.734472 MHz)<br>PAL–M (14.30244 MHz) |
| Pull–in range: | ± 1600 Hz<br>(with respect to crystal frequency) |
| Tolerance: | 30 ppm (with fixed load capacitor) |
| Temperature Coefficient: | 50 ppm (with fixed load capacitor) |
| Operating Mode: | Fundamental series resonance |
| Load Capacitance: | Nominally 20 pF |
| Motional Capacitance: | 10 to 30 fF |
| Series Resistance: | < 30 Ω (nominally 10 Ω) |

The oscillator output resistance at Pin 36 is nominally 300 Ω for NTSC mode, and 400 Ω at Pin 38 for PAL mode. It is recommended that a stray capacitance (PC board, package pins, etc.) of 4.0 to 5.0 pF be included when selecting a crystal.

The above values for tolerance and temperature coefficent can be increased if a trimmer capacitor is used for the load capacitor.

The crystal PLL filter (Pin 44) voltage is between 1.8 and 3.8 V in normal operation. If the color output of the MC44011 is incorrect, or non–existent (ACC flag off), this voltage should be checked. If it is beyond either of the above limits, the capacitor in series with the crystal should be changed so as to allow the PLL to pull–in the crystal. The capacitor is generally specified by the crystal manufacturer, but should also comply with Table 18 specifications. If no burst is present, Pin 44 voltage will be ≈1.3 V.

The selected crystal frequency can be checked by using a scope at the non–selected crystal pin. The signal amplitude is nominally 200 to 400 mVpp. In this way the selected crystal's frequency is not affected by the scope probe.

**Table 17. External Components**

| Pin No. | Name | Function |
|---|---|---|
| 1, 3 | Video 1, Video 2 | Input signals must be capacitor–coupled. The 470 Ω resistors protect the pins from ESD and RFI. The 75 Ω resistors are not required by the MC44011, but depend on the signal source. The 47 pF capacitors filter high frequency noise. |
| 2 | ACC Filter | The 0.1 μF ceramic capacitor filters the Automatic Gain circuit. |
| 4 | Vert. Sync | The pull–up resistor is required for this open–collector output. |
| 5, 6 | SCL, SDL | Pull–up resistors are required on each $I^2C$ line since outputs are open–collector. They are typically located at the master device. |
| 7 | Field ID | No external components required. |
| 8 | Burst Gate | No external components required. |
| 9 | $I_{ref}$ | The 110 kΩ resistor provides ≈ 32 μA from the + 5.0 V source. This pin must be well filtered to the Quiet Ground (Pin 10). |
| 10 | Quiet GND | This is the Reference Ground for Pin 9 and the PLL1 Filter. |
| 11 | PLL1 Filter | The 100 kΩ resistor, and the 0.1 μF and 68 pF capacitors are the filter network for this PLL. Connect to Pin 10 ground. |
| 12 | PLL1 Filt. SW | The 12 kΩ resistor and 470 pF capacitor give the filter a longer time constant when Pin 12 is switched in. |
| 13 | 16 Fh/$C_{Sync}$ | No external components required. |
| 14 | Fh Ref | No external components required. |
| 15 | 15 k Return | TTL Return signal from external frequency divider. |
| 16 | PLL2 Filter | The 10 kΩ resistor and 47 nF and 4.7 nF capacitors are the filter network for this PLL. Connect to Pin 17 ground. |
| 17 | Ground | Ground for the Pixel Clock circuit. |
| 18 | Clk Out | Pixel Clock output to external frequency divider and triple A/D converter. |
| 19 | $V_{CC3}$ | + 5.0 V supply for the Pixel Clock circuit. |
| 20, 21, 22 | R, G, B Out | The 390 Ω pull–up resistors are required for these open–collector outputs. The pull–ups should go to a clean, well filtered + 5.0 V supply. These pins cannot drive 75 Ω directly. If required to do so, see text for suggested buffer. |
| 23 | $V_{CC2}$ | + 5.0 V supply for the Color Difference section. |
| 24 | Ground | Ground for the Color Difference section. |
| 25 | Fast Comm. | No external components required. This input *should not* be left open. |
| 26, 27, 28 | B, G, R In | Input signals must be capacitor–coupled. The 220 Ω resistors protect the pins from ESD and RFI. |
| 29 | Y2 Input | Input signals must be capacitor–coupled. The 220 Ω resistor protects the pin from ESD and RFI. The 75 Ω resistor is not required by the MC44011, but depends on the signal source. |
| 30, 31 | B–Y, R–Y In | Input signals must be capacitor–coupled. The MC44140 is required if PAL signals are processed (see text). |
| 32 | Y1 Clamp | The 0.1 μF ceramic capacitor provides clamping for the Y1 output. |
| 33 | Y1 Out | No external components required. This pin cannot drive 75 Ω directly. If required to do so, see text for suggested buffer. |
| 34, 35 | System Sel., Sandcastle | For use by the MC44140 delay line. No other external components required. |
| 36, 38 | Xtal 2, Xtal 1 | A 17.7 MHz crystal is required (at Pin 38) for PAL signals, and a 14.3 MHz crystal is required (at Pin 36) for NTSC signals. If only one crystal is required, leave the other pin open. The series capacitor depends on the crystal manufacturer. (See Table 18 for crystal specs.) |
| 37 | N/C | No external components required. |
| 39 | Ground | Ground for Color Decoder section. |
| 40 | $V_{CC1}$ | + 5.0 V supply for the Color Decoder section. |
| 41, 42 | B–Y, R–Y Out | The MC44140 is required if PAL signals are processed. Otherwise, capacitor–couple to Pins 30, 31 (see text). |
| 43 | Indent. Filter | The 0.1 μF ceramic capacitor provides filtering for the Identification circuit. |
| 44 | 4FSC PLL | The 47 kΩ resistor, and 0.1 μF and 2.2 nF capacitors are the filter network for the crystal PLL. Connect to Pin 39 ground. |

**Power Supplies and Ground**

There are three $V_{CC}$ pins (Pins 19, 23, and 40) which must be connected to a source of +5.0 V, ± 5%. Since the three pins are internally connected by diodes, none can be left open, even if a particular section (such as the Pixel Clock Generator) is to be unused. Total current required is ≈135 mA (including the RGB output load current). There are four ground pins (Pins 10, 17, 24, and 39) which must be connected together, and preferably connected to a ground plane.

Pins 19 and 17 are the $V_{CC}$ and ground for the Pixel Clock Generator, and the circuitry associated with the Pixel Clock should be referenced to those two pins.

Pins 23 and 24 are the $V_{CC}$ and ground for the Color Difference section, which includes the RGB outputs. The output pull–up resistors should be connected to the $V_{CC}$ at Pin 23.

Pins 40 and 39 are the $V_{CC}$ and ground for the Color Decoder, Sync Separator, Horizontal PLL and the Vertical Decoder. Pin 10 is the Quiet Ground for the horizontal PLL's VCO and filter, and therefore, the components on Pins 9 and 11 should be connected as close as possible to Pin 10.

Bypassing of the power supplies must be done as close as possible to each $V_{CC}$ pin, and at the output pull–up resistors. Recommended bypassing components are a 10 μF tantalum capacitor in parallel with a 0.01μF ceramic.

**Input Signals**

The various video inputs, Video 1 and 2, Red In, Green In, Blue In, R–Y, B–Y, and Y2 inputs, are designed to accept standard level analog video waveforms. They are not designed for digital signals. The input impedance of the above pins is high. The need for 75 Ω terminations for those video signals depends on the video source itself. All of the above signals must be capacitor–coupled as clamping is provided internally.

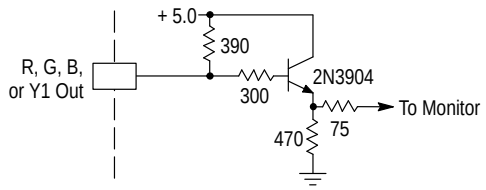
The $I^2C$ inputs (SCL, SDL) are designed according to the $I^2C$ specifications, which define $V_{OL}$ as between 0 and 1.5 V, and $V_{OH}$ as between 3.0 V to $V_{CC}$. See Appendix C.

The 15 k Return and Fast Commutate (Pins 15 and 25, respectively) are designed for TTL level signals. If unused, they should not be left open, but connected to + 5.0 V, or ground, as appropriate.

**Output Signals**

The RGB/YUV outputs are open–collector, and require pull–up resistors (typically 390 Ω) to a clean + 5.0 V ($V_{CC2}$). The output impedance is such that the load impedance (to ground) should be >1.5 kΩ. If it is desired to drive a 75 Ω load (e.g., a monitor) from these outputs, a simple buffer (see Figure 43) can be added.

**Figure 43. Output Buffer**




The Y1 output (Pin 33) has an output impedance of ≈ 300 Ω, and can be used as a monitoring point, or to drive the input of the MC44145 sync separator, or other high impedance loads (minimum load for Y1 is 1.0 kΩ). If it is to be used to drive a 75 Ω load, the buffer shown in Figure 43 can be used, *except the 390 Ω resistor must be deleted*.

The Vertical Sync output (Pin 4) is an open–collector logic level output, and requires a pull–up resistor to + 5.0 V. 10 kΩ is recommended, but it can be as low as 1.0 kΩ. The $I^2C$ data line (SDL, Pin 6) is also open–collector when it is an output, and can sink a maximum of 3.0 mA. Only one pull–up resistor is required on the SDL line (regardless of the number of devices on that line), and it is typically near the master device. The Field ID, Burst Gate, 16 Fh/$C_{Sync}$, Fh Ref, and Pixel Clock outputs are logic level totem–pole outputs.

**PC Board**

The PC board layout should be neat and compact, and should preferably have a ground plane. If feasible, a second plane should be provided for the + 5.0 V supply, but this is not mandatory. The components at Pins 9 and 11 should be connected to the same ground track which goes to Pin 10. The $V_{CC}$ and ground should be connected as directly as possible to the power supply, and not routed through a maze of digital circuitry before arriving at the MC44011. Since the MC44011 is intended to be used with A/D converters and high speed digital signals, it is expected digital circuitry will be on the same board. Care should be taken in the layout to prevent digital noise from entering the analog portions of the MC44011. The most sensitive pins are Pins 1,2, 3, 9, 10, 11, 12, 16, and 44, and should be protected from noise.

**Initialization and Programming Information**

Upon powering up the MC44011, initialization consists of first filling the registers with initial values to set a known condition. Table 19 provides recommended values for the initial settings, although these may be tailored for each application (with the exception of Bits $79–6,7, $7A–6, $86–6, and $87–6). Table 19 settings will set up the MC44011 to the following conditions:

- Composite video input at Video 1 (Pin 1), NTSC, using the crystal at Xtal 2 (Pin 36).
- Y1 enabled, RG outputs enabled, and Composite Sync at Pin 13
- RGB inputs not enabled (R–Y, B–Y inputs are enabled)
- The Sound Trap at 4.5 MHz
- The Luma Peaking at 0 dB
- The Luma Delay at minimum
- High gain and high noise rejection for the horizontal PLL
- Vertical decoder set to Injection Lock mode
- The Pixel Clock VCO is off

After the registers are initialized, then set Bit $86–6 to 0, and load register $00 with $00. This will enable the horizontal PLL, permitting normal operation.

**Table 19. Recommended Initial Settings**

| Sub Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| $77 | S–VHS Y = 0 | S–VHS C = 0 | FSI = 0 | L2 Gain = 0 | BLCP = 0 | L1 Gain = 0 | CBI = 0 | CAI = 1 |
| $78 | 36/68 µs = 0 | Calkill = 0 | (R–Y)/(B–Y) Adjust DAC = 32 | | | | | |
| $79 | HI = 1 | VI = 1 | Subcarrier Balance DAC = 32 | | | | | |
| $7A | Xtal =1 | SSD = 0 | | | | | | |
| $7B | T1 =1 | T2 = 1 | | | | | | |
| $7C | SSC = 0 | SSA = 1 | | | | | | |
| $7D | P1 =1 | SSB = 0 | Blue Bias = 00 | | | | | |
| $7E | P3 = 1 | P2 = 1 | Red Bias = 00 | | | | | |
| $7F | D3 = 0 | D1 = 0 | Pixel Clock VCO Gain Adjust = 63 | | | | | |
| $80 | RGB EN = 1 | D2 = 0 | Blue Contrast Trim = 32 | | | | | |
| $81 | Y2 EN = 0 | Y1 EN = 1 | Main Contrast = 47 | | | | | |
| $82 | YUV EN = 0 | YX EN = 0 | Red Contrast Trim = 32 | | | | | |
| $83 | L2 Gain = 1 | L1 Gain = 1 | Blue Brightness Trim = 32 | | | | | |
| $84 | H Switch = 1 | 525/625 = 1 | Main Brightness = 30 | | | | | |
| $85 | PClk/2 = 1 | $C_{Sync}$ = 1 | Red Brightness Trim = 32 | | | | | |
| $86 | $V_{in}$ Sync = 1 | PLL1 EN = 1 | Main Saturation (Color Difference section ) = 32 | | | | | |
| $87 | Y2 Sync = 0 | 0 | (R–Y)/(B–Y) Saturation Balance (Decoder section) = 15 | | | | | |
| $88 | V2/V1 = 1 | $RGB_{Sync}$ = 0 | Hue = 32 | | | | | |

These settings are for power–up initialization only. Refer to the text, and Appendix B, for subsequent modifications based on the application.

Then, after selecting the desired input(s) (from Pins 1, 3, or 26 to 31), and based on the applied signals at those inputs, and by reading the flags, the registers are adjusted for the desired and proper mode of operation. A suggested routine for setting modes is given in Appendix B. The “initial values” in the Control DACs table of Appendix B are those in Table 19. The remainder of the flow chart is a recommendation only, and should be tailored for each application.

The monitoring of flags should be done on a regular basis, and it is recommended it be done once per field. See Table 16 (in the Functional Description section) for a summary of the flags. Should any flags change, the following procedures are recommended:

**Flag 11 (Horizontal Enabled)** – Once enabled by setting Bit $86–6 = 0, this flag should always remain a 1. Should it change to 0, reset $86–6 to 0, and write $00 to register $00 again. If the flag does not return to a 1, this indicates a possible device malfunction.

**Flag 12 (Horizontal Out–of–Lock)** – When 1, this indicates:

a) the wrong input is selected (Bits $88–7, $81–7, $80–7, and $77–7,6), or;
b) the wrong sync source is selected (Bits $86–7, $87–7, and $88–6), or;
c) the incoming signal is somewhat unstable, as from a VCR tape (change Bit $83–6), and/or;
d) the incoming signal is noisy (change Bit $84–7), or;
e) a loss of the incoming signal with sync.

(It is possible for this flag to flicker when the video signal is from a poor quality tape, or other poor quality source.)

**Flag 14 (Less than 576 lines)** – This flag, from the vertical decoder, is used to help determine if the signal is PAL or NTSC. Should it change, this indicates the incoming signal has changed format, or possibly one of the items listed under Flag 12 above.

**Flag 15 (Vertical Countdown Engaged)** – Bits 77–0 and 1 must be set to 1 (after Flag 12 reads 0) for this flag to indicate correctly. Then this flag will change to a 1 after 8 fields of successful synchronization of the internal counters with the incoming signal. To change to a 0 requires 8 consecutive fields of non–synchronization. If this flag changes to 0, this indicates a loss of signal, a change of signal format, or instability in the horizontal PLL.

**Flags 19, 20 (VCO Control Voltage Low/High)** – These flags are meaningful only if the Pixel Clock Generator is used. If Flag 19 is a 1, the gain of the pixel clock VCO needs to be increased by increasing the value of register $7F, and/or set Bit $85–7 =1. If Flag 20 is a 1, the value of the register must be decreased, and/or set Bit $85–7 = 0. If the VCO is turned off ($7F = 63), Flag 19 will be 0, and Flag 20 will be 1.

**Flag 23 (ACC Active)** – If this flag is a 0, it indicates the ACC loop is not active. This will happen if the burst signal is less than 30 mVpp, if the incorrect crystal is selected ($7A–7), if the crystal PLL is not locked, or if the horizontal PLL is not locked.

**Flag 24 (PAL Identified)** – This flag is a 1 when PAL signals are applied, and a 0 when NTSC signals are applied, or when no burst is present.

It is recommended that the Color Decoder section, and crystal, should be set according to the state of Flags 14, 23, and 24 according to Table 20.

**Table 20. Color Standard Selection Table**

| Flags | | | Bit Settings | | | | |
|---|---|---|---|---|---|---|---|
| #14 <576 Lines | #23 ACC Active | #24 PAL Signal | Crystal | SSA ($7C–6) | SSB ($7D–6) | SSC ($7C–7) | System |
| X | 0 | X | Either | 1 | 1 | 0 | Color Kill |
| 0 | 1 | 0 | Either | 1 | 1 | 0 | Color Kill |
| 0 | 1 | 1 | 17.7 MHz | 0 | 1 | 0 | PAL |
| 1 | 1 | 0 | 14.3 MHz | 1 | 0 | 0 | NTSC |
| 1 | 1 | 1 | (Note 1) | 0 | 1 | 0 | PAL–M |

**NOTES:** 1. PAL–M, used in Brazil and other South American countries, can be decoded by the MC44011, but requires a 14.3024 MHz crystal.
2. SSD ($7A–6) is always set to 0.

## MISCELLANEOUS APPLICATIONS INFORMATION

### Use of the MC44140 Delay Line

The MC44140 delay line is generally required if PAL signals are to be decoded, so as to average out the line–by–line color information associated with PAL color decoding. If the same single PAL video source is always used in a particular application, the delay line can be eliminated, and any slight phase errors can be corrected with the DAC of register $79–5/0. If, however, various video sources can be used, and/or if the video signal is less than broadcast quality, it is recommended the MC44140 delay line be included.

The MC44140 acts on the color difference signals before they enter the color difference stage of the MC44011. It will, however, pass NTSC signals through without modifications. The MC44011 uses the System Select output (Pin 34) to indicate to the delay line which signals are being processed. The System Select voltage is set when the color decoder is set with Bits SSA, SSB, SSC, SSD. The Sandcastle output (Pin 35) provides the horizontal timing signals to the delay line. In addition, the MC44140 uses the crystal frequency for the internal counters.

The MC44140 is inserted into the circuit between the Color Difference outputs and inputs of the MC44011. In addition, the MC44140 provides pins (Pins 8,9) for inserting an alternate source of color difference signals to the MC44011 by setting the System Select to external (Bit $7C–7 = 1). See Figure 44 for a suggested circuit.

If only NTSC signals are to be processed by the MC44011, the MC44140 is not needed. In this case, connect Pin 42 to Pin 31 with a 0.1µF capacitor, and similarly connect Pin 41 to Pin 30.

**Figure 44. Incorporating the MC44140 Delay Line**

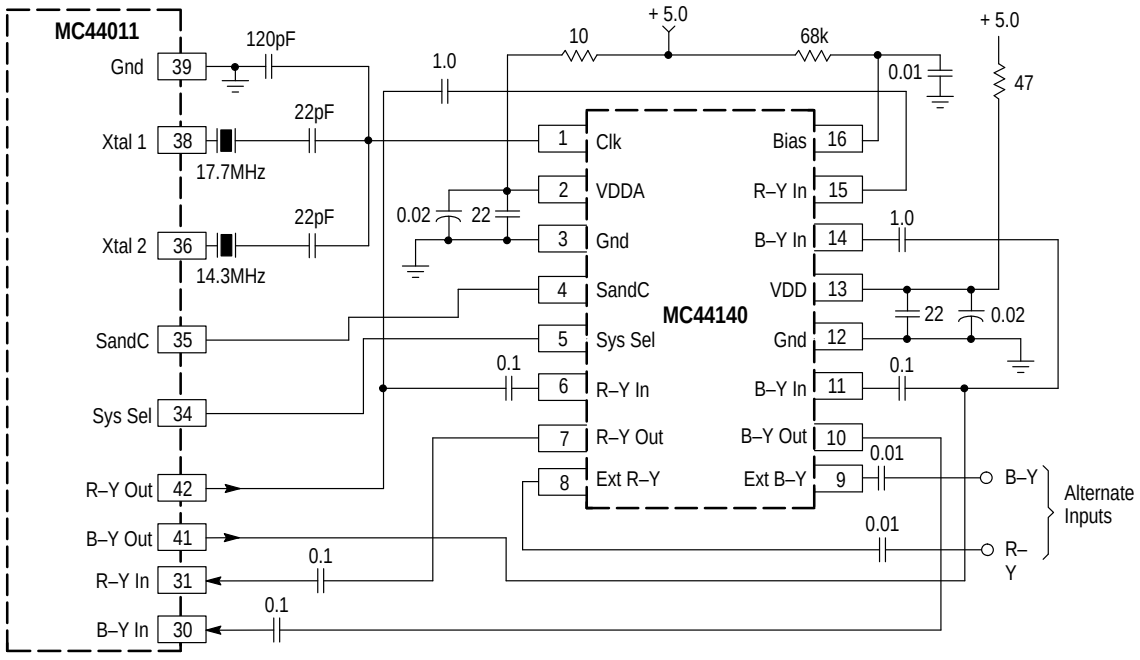
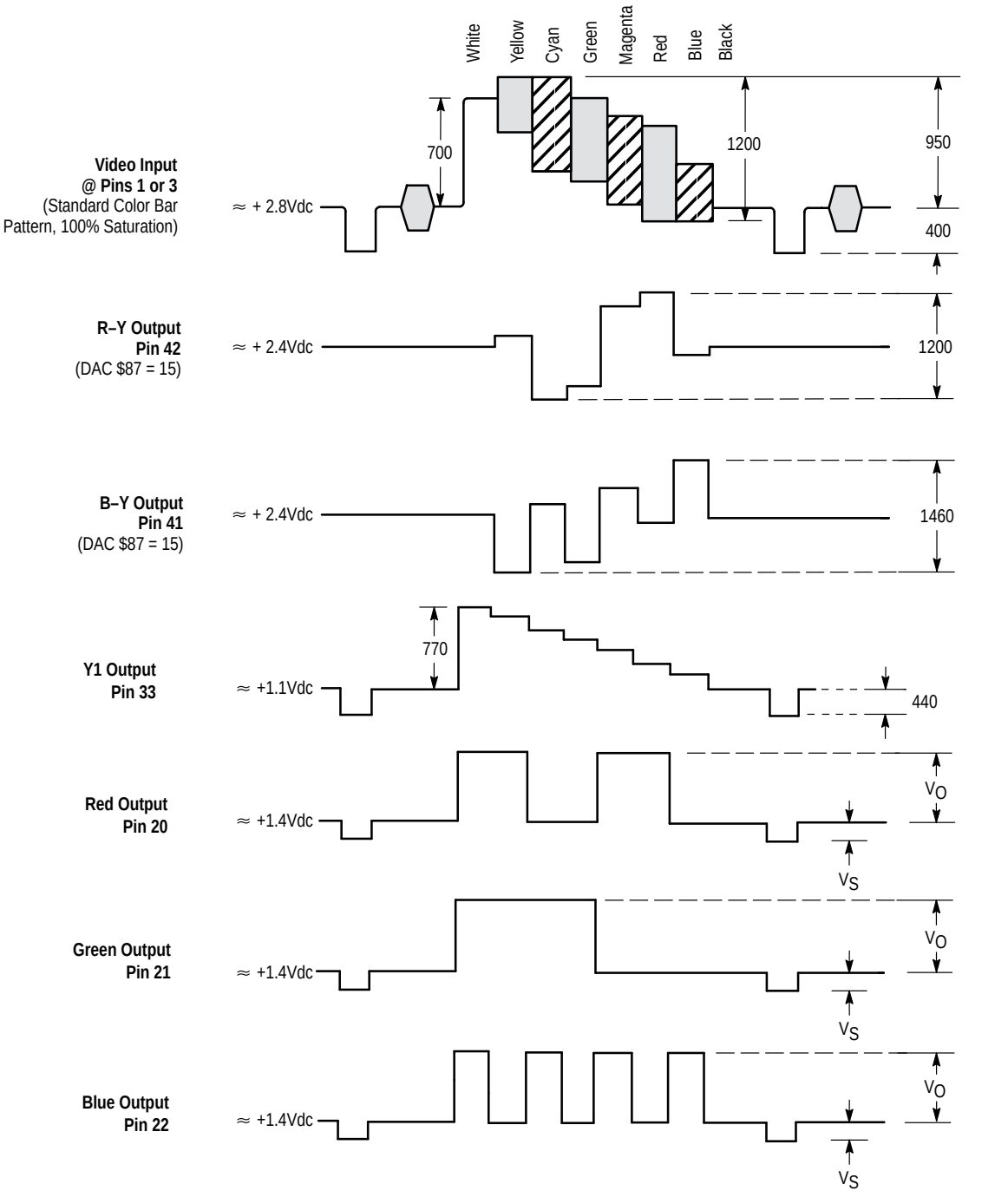


**Figure 45. Typical Waveforms**




DACs set per Table 19. All amplitudes in milliVolts.
Voltages are nominal, and do not represent guaranteed limits.

| DAC 81 | $V_O$ | $V_S$ |
|---|---|---|
| 32 | 1725 | 220 |
| 47 | 2360 | 340 |
| 63 | 3160 | 440 |

**Use of the MC44145 Pixel Clock Generator**

For most applications the Pixel Clock Generator (PLL2) within the MC44011 will be suitable. In those cases, however, where the pixel clock frequency is set to within ±1.0 MHz of the selected crystal frequency (14.3 MHz or 17.7 MHz), or to within ±1.0 MHz of double the selected crystal frequencies, undesirable noise artifacts may be present on the RGB outputs. In these cases the MC44145 should be used to generate the Pixel Clock. The circuitry within the MC44145 duplicates that of the MC44011, but since it is physically removed from the circuitry within the MC44011, the interfering noise is not generated. If the MC44145 is used, the Pixel Clock Generator within the MC44011 should be shut off by setting the DAC of register $7F to 63, eliminating the components at Pin 16, and grounding Pin 16.

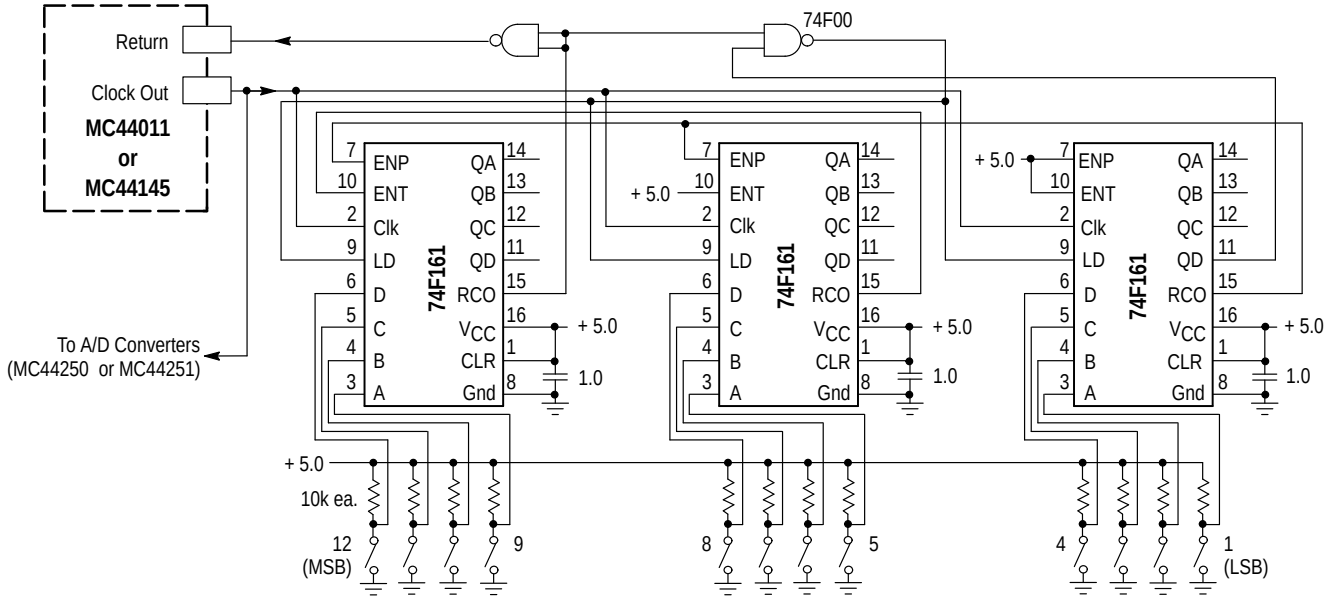
If the desired pixel clock frequency is close to the limits mentioned above, then experimentation may be used to determine the need for the MC44145.

**Frequency Divider**

The frequency of the Pixel Clock is determined by the horizontal frequency and an external frequency divider. The divider simply divides down the Pixel Clock Frequency so that it equals the horizontal frequency. The PLL within the MC44011 (or the MC44145) compares the horizontal frequency with the returned frequency, and adjusts the internal VCO accordingly, to achieve the proper relationship between the two. The PLL will phase–lock the negative–going edge of the returned signal with the positive–going edge of the Fh signal (Pin 14 of the MC44011). The returned signal must be TTL logic level amplitudes, and have a minimum low time of 200 ns. A suggested circuit for the divider, shown in Figure 46, uses 74F161 programmable binary counters. The 12 switches at the bottom are used to set the division ratio, and hence the Pixel Clock frequency.

The division ratio is determined by dividing the desired clock frequency by the horizontal frequency, and then using the closest whole number. After determining the binary equivalent of that number, close each switch corresponding to a 1, and leave open each switch corresponding to a 0. Alternately, the switches could be deleted, and Pins 3, 4, 5 and 6 of each 74F161 hard–wired to + 5.0 V or ground, or controlled by a microprocessor where different pixel clock frequencies are required.

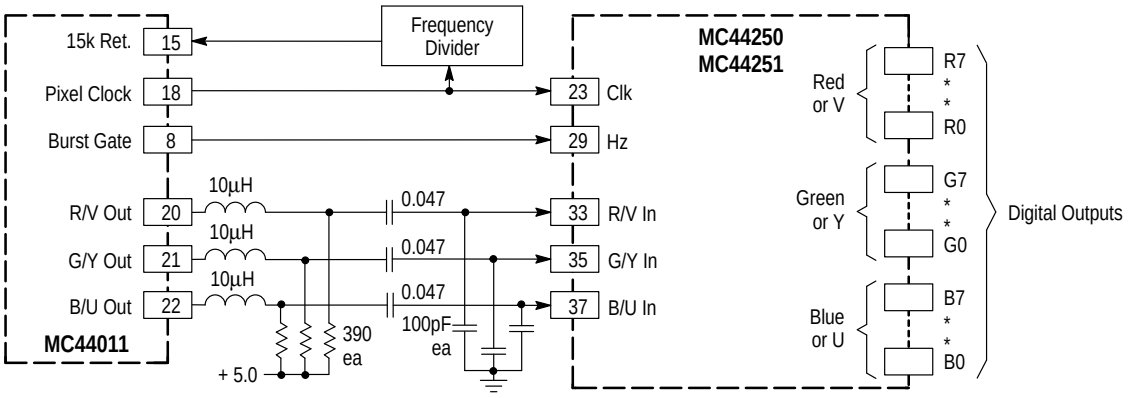
**Figure 46. Suggested Frequency Divider**



**Connecting the MC44011 to the MC44250 or MC44251 A/D Converter**

The MC44250 and MC44251 triple A/D converters are designed to accept RGB or YUV inputs, and provide 8–bit equivalents of each. Additionally, the inputs have black level clamps, allowing the input signals to be capacitor–coupled. The simplified schematic of Figure 47 shows the connections between the MC44011 and the MC44250/1, including anti–aliasing filters between the devices. Connection to other A/D converters would be done in a similar manner. Refer to the appropriate data sheet for details.

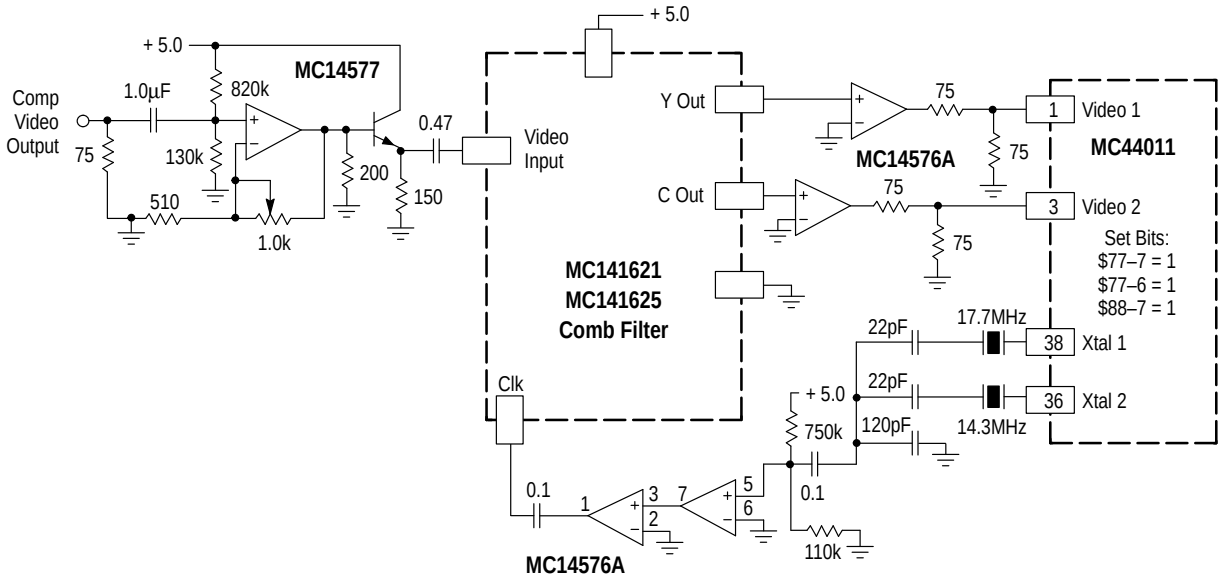
**Figure 47. Connecting to a Triple A/D Converter**




**Connecting the MC44011 to the MC141621 or MC141625 NTSC Comb Filter**

A comb filter can be used ahead of the MC44011 to enhance picture quality by providing a more accurate separation of the luma and chroma components from the composite video, without sacrificing bandwidth. The usual benefits are reduced dot crawl, and increased color purity. Figure 48 (a simplified schematic) shows the normal mode of implementing the MC141621 (NTSC) or MC141625 (PAL/NTSC) comb filter with the MC44011. The two comb filters can also provide the Y and C signals in digital format. Refer to their data sheets for details. The MC14576A op amps have an internally set gain of 2.

**Figure 48. Implementing the Comb Filter**



## APPENDIX A

### Control Bit Summary

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| $77 | S–VHS Y | S–VHS C | FSI | L2 Gate | BLCP | L1 Gate | CBI | CAI |
| | 0 = Comp. Video<br>1 = S–VHS | | 0 = 50 Hz<br>1 = 100 Hz | 0 = PLL2 Gating | 0 = Clamp Gating | 0 = PLL1 Gating | | |
| $78 | 36/68 | CalKill | Vertical Time Constant | | | | 1 = Cal Loop Disabled | |
| $79 | HI | V1 | Set to 1, 1 | | | | | |
| $7A | Xtal | SSD | Set to 0 | | | | 1 = Pin 36 Crystal | |
| $7B | T1 | T2 | | | | | | |
| $7C | SSC | SSA | | | | | | |
| $7D | P1 | SSB | | | | | | |
| $7E | P3 | P2 | | | | | | |
| $7F | D3 | D1 | | | | | | |
| $80 | RGB EN | D2 | 0 = RGB Inputs Enabled | | | | | |
| $81 | Y2 EN | Y1 EN | 1 = Y1 Enabled | | | | 1 = Y2 Enabled | |
| $82 | YUV EN | YX EN | 1 = RGB Matrix Enabled | | | | 1 = YUV Outputs | |
| $83 | L2 Gain | L1 Gain | 1 = PLL1 Gain High | | | | 1 = PLL2 Gain Low | |
| $84 | H Switch | 525/625 | 1 = NTSC | | | | 1 = Switch Closed | |
| $85 | PClk/2 | C Sync | 1 = Comp. Sync | | | | 1 = ÷ 2 Enabled | |
| $86 | $V_{in}$ Sync | PLL1 EN | 0 = PLL1 Enabled | | | | 1 = Comp. Video Sync Source | |
| $87 | Y2 Sync | 0 | Set to 0 | | | | 1 = Y2 Sync Source | |
| $88 | V2/V1 | RGB Sync | 1 = RGB Sync Source | | | | 1 = Pin 1 Input | |

| CBI | CAI | Sync Mode |
|---|---|---|
| 0 | 0 | Force 625 |
| 1 | 0 | Force 525 |
| 0 | 1 | Inj. Lock |
| 1 | 1 | Auto Count |

| Sound Trap Notch Frequency | | | |
|---|---|---|---|
| T1 | T2 | PAL | NTSC |
| 0 | 0 | 6.5 MHz | 5.25 MHz |
| 0 | 1 | 5.5 + 5.75 MHz | 4.44 + 4.64 MHz |
| 1 | 0 | 6.0 MHz | 4.84 MHz |
| 1 | 1 | 5.5 MHz | 4.44 MHz |

| SSA | SSB | SSC | Color System |
|---|---|---|---|
| 0 | 0 | 0 | Not Used |
| 0 | 1 | 0 | PAL |
| 1 | 0 | 0 | NTSC |
| 1 | 1 | 0 | Color Kill |
| X | X | 1 | External |

| P1 | P2 | P3 | Y1 Peak |
|---|---|---|---|
| 0 | 0 | 0 | 9.5 dB |
| 0 | 0 | 1 | 8.5 |
| 1 | 0 | 0 | 7.7 |
| 1 | 0 | 1 | 6.5 |
| 0 | 1 | 0 | 5.3 |
| 0 | 1 | 1 | 3.8 |
| 1 | 1 | 0 | 2.2 |
| 1 | 1 | 1 | 0 |

| | | | Luma Delay | |
|---|---|---|---|---|
| D1 | D2 | D3 | 14.3 MHz | 17.7 MHz |
| 0 | 0 | 0 | 690 ns | 594 ns |
| 0 | 0 | 1 | 760 | 650 |
| 0 | 1 | 0 | 830 | 707 |
| 0 | 1 | 1 | 900 | 763 |
| 1 | 0 | 0 | 970 | 819 |
| 1 | 0 | 1 | 1040 | 876 |
| 1 | 1 | 0 | 970 | 819 |
| 1 | 1 | 1 | 1040 | 876 |

Comp. Video Mode

### Control DACs

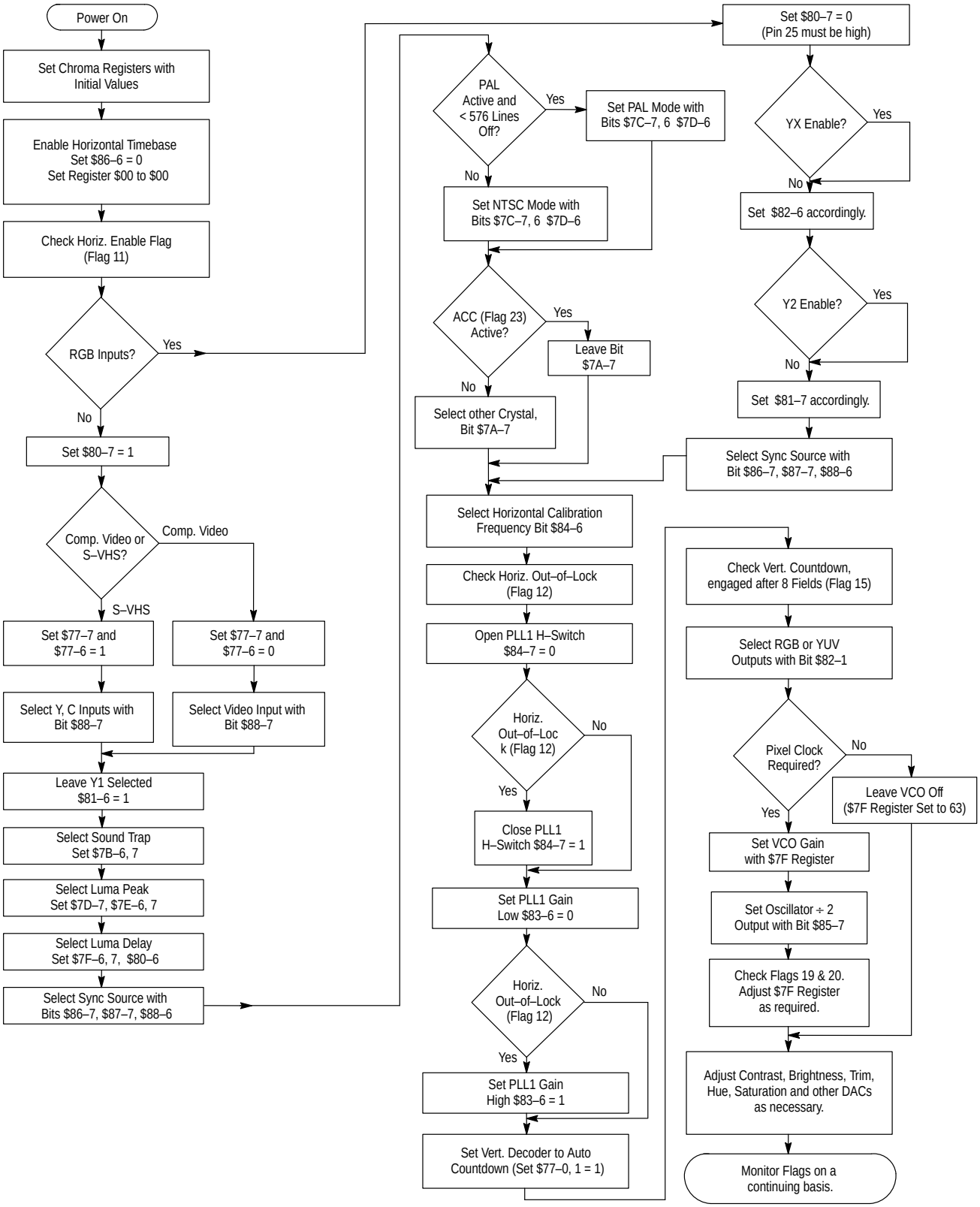
| | | | |
|---|---|---|---|
| $78 | R–Y/B–Y Gain Adjustment | $82 | Red Contrast Trim |
| $79 | Subcarrier Phase | $83 | Blue Brightness Trim |
| $7D | Blue DC Bias | $84 | Main Brightness |
| $7E | Red DC Bias | $85 | Red Brightness Trim |
| $7F | Pixel Clock VCO Gain | $86 | Saturation (Color Diff. Section) |
| $80 | Blue Contrast Trim | $87 | Saturation (Decoder) |
| $81 | Main Contrast | $88 | Hue |

### Flags

| | | | |
|---|---|---|---|
| 10 | Internally Set to 1 | 19 | Pixel Clock VCO Gain too low |
| 11 | Horizontal Loop (PLL1) Enabled | 20 | Pixel Clock VCO Gain too high |
| 12 | Horizontal Loop not Locked | 21 | Internally Set to 1 |
| 13 | Internally Set to 0 | 22 | Internally Set to 0 |
| 14 | Less than 576 Lines | 23 | ACC Loop Active |
| 15 | Vertical Decoder Engaged | 24 | PAL Signals Detected |
| 16 | Internally Set to 1 | 25 | Not Used |
| 17 | Internally Set to 1 | 26 | Internally Set to 0 |

## APPENDIX B

### Suggested Mode Setting Routine (Simplified)



## APPENDIX C

## I²C Description

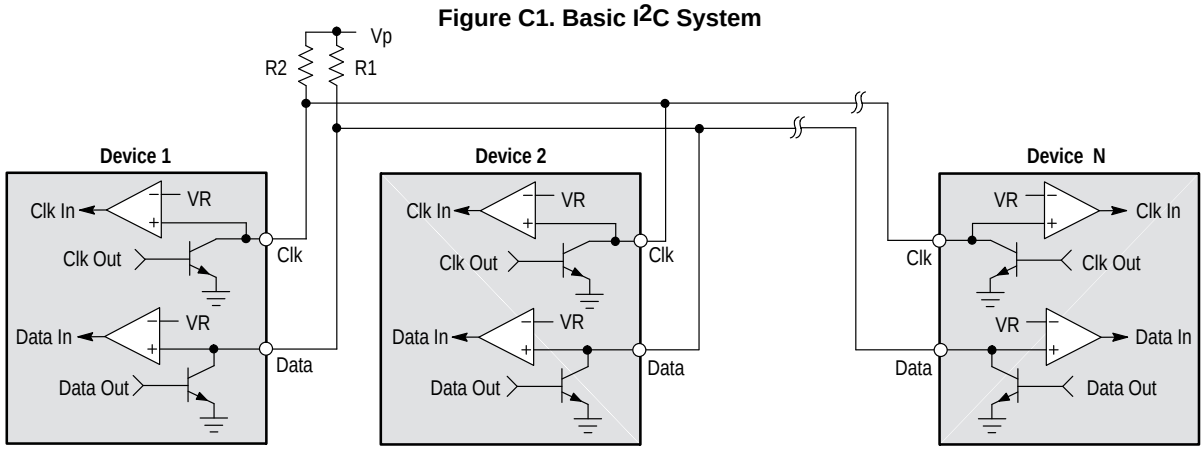
### Introduction

The I²C system, a patented and proprietary system developed by Philips Corporation, defines a two–wire communication system. The number of devices in a system is limited only by the system capacitance and data rate. Each device is assigned two unique addresses – one for writing to it, and one for reading from it. Any device may act as a master by initiating a data transfer with any other device (the slave). Data transfer is in 8–bit bytes, and can be in either direction, but not in both directions in one data transfer operation.

### Hardware Aspects

The system bus consists of two wires, Clock and Data. All devices must have open–collector (or open–drain) outputs. A single pull–up resistor is required on each line, as shown in Figure C1.

**Figure C1. Basic I²C System**




Devices such as the MC44011, which never act as a master, need not have the output drive transistor at the Clock pin. Nominal value for R1 and R2 is 10 kΩ, but can be different to account for system capacitance at high data rates. VR is a switching threshold for input signals.

The significant electrical characteristics are as follows:

– Maximum data rate (Clock frequency) is 100 kHz;
– $V_{OL}$ max is 0.4 V when sinking 3.0 mA;
– $V_{IL}$ max is 0.3 x Vp, but at least +1.5 V;
– $V_{IH}$ min is + 3.0 V for a + 5.0 V system, or 0.7 x Vp for other supply voltages.
– The maximum input current at Clock and Data at $V_{OL}$ max (when they are inputs) is –10 μA;
– The maximum input current at Clock and Data at 0.9 x Vp (when they are inputs) is +10 μA;
– The maximum pin capacitance is 10 pF;
– Maximum bus capacitance is 400 pF.

### Data Transfer

Prior to initiating a data transfer, both lines must be high (all drive transistors off). A device which initiates a data transfer assumes the role of the master, and generates a START condition by taking the Data line low while Clock is still high. At this time, all other devices become listeners. The master will supply the clock for the entire sequence.

The master then sends the 8–bit address by operating both the clock and data lines. Data must be stable during the clock's high time, and can change during the clock's low time. The MSB is sent first. The address must end in a 0 if it is a Write operation (data transfer from master–to–slave), and it must end in a 1 if it is a Read operation.

At the 9th Clock Pulse, the master must release the Data line high, and the slave must provide an acknowledge bit by pulling Data low during this clock time. If the master does not receive a proper acknowledge, it can terminate the operation.

After the first acknowledge, the role of the two devices depends on whether it is a Write or a Read operation, but the master always supplies the clock.

– In a Write operation the master is the transmitter, and the slave is the receiver.
– In a Read operation the slave is the transmitter, and the master is the receiver.

The transmitter then sends the next 8–bit byte. At the 18th Clock Pulse (and every 9th clock pulse thereafter), the transmitter releases the Data line, and the receiver acknowledges by pulling Data low. There is no limit to how many bytes may be sent after the address.

When all data is transferred, the Data line must be released by the transmitter so that the master can set the STOP condition. This is done by first pulling Data low (during clock low), then releasing Data high while clock is high. After this, the bus is free for any other device to initiate a new data transfer.

### Definitions

**Master** – The device which initiates a data transfer (regardless of the data direction), generates the clock, and terminates the transfer.

**Slave** – The device addressed by the master.

**Transmitter** – The device which supplies data to the bus.

**Receiver** – The device which receives data from the bus.

Notice that the master is not necessarily the transmitter, and the slave is not necessarily the receiver.

### Other

For additional information on the I²C bus specifications; modes of operation; arbitration; and synchronization, contact Philips Corporation.

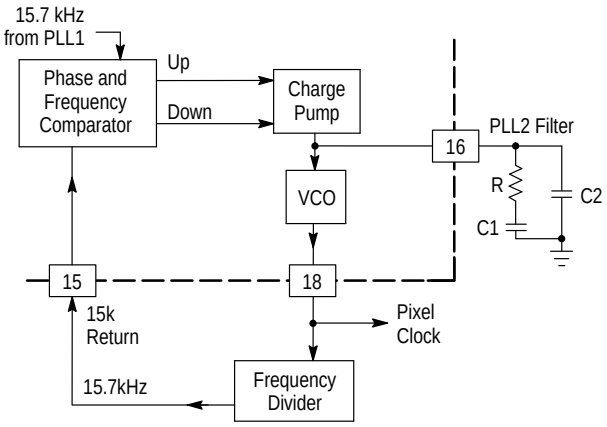
## APPENDIX D

## PLL Loop Theory

**High Frequency Line–Locked Clock Generator**

This section is not intended as a complete loop theory, its aim is merely to point out the idiosyncrasies of the loop, and provide the user with enough information for the selection of filter components. For a more in depth explanation, the references at the end of this section may be consulted.

**Figure D1. PLL2 Basic Configuration**




The following general remarks apply to the loop (PLL2):
– The loop frequency is ≈15.7 kHz.
– In spite of the samples nature of the loop, a continuous time approximation is possible if the loop bandwidth is sufficiently small.
– Ripple on $V_C$ (filter pin) is a function of loop bandwidth.
– The loop is a type II, 3rd order. However, since C2 is small, the pole it creates is far removed from the low frequency dominant poles, and the loop can be analyzed as a 2nd order loop.

The following remarks apply to the Phase and Frequency Comparator:
– Phase and frequency sensitive.
– Independent of duty cycle.
– It has 3 allowed states: up, down, and off (high impedance).
– The VCO is always pulled in the right direction during acquisition.
– The Comparator's gain is higher at or near lock.

The last two remarks imply that only the higher value need be taken into account, as acquisition will be slower but always in the correct direction, whereas the higher gain will come into action as soon as the error reaches 2π.

The following values are selected and defined:
C2 = C1/10 or less, to satisfy the requirement that the effect of C2 on the low frequency response of the loop be minimal, and similar to a 2nd order loop.

$\xi$ = 0.707 (damping factor).
$\omega i$ = 15750 x 2p = 98960 rad/sec (input frequency).
$\tau$ = RC as the loop filter
K = Ko x Ip x R/(2πN) – the loop gain
K′ = K x $\tau$ = $4\xi^2$ (the normalized loop gain)
Ko = 70 x $10^6$ rad/V

Stability analysis with C2 = C1/10 and K′ = 2 ($\xi$ = 0.707) gives a minimum value of 7.5 for the ratio $\omega i/K$. To have some margin, a reasonable value can be 15 to 20 or higher.

Selecting $\omega i/K = 20$ yields,
$K = \omega i/20 \approx 5000$.

Using the following items:
K′ = 2,
$\tau$ = 2/K = 400 μs,
K = Ko x Ip x R/(2πN)
Ip = 20 μA
N = 2000 (average value)

yields a value of 22 kΩ for R. Using a value of 400 μs for $\tau$, C1 calculates to 18 nF, and C2 calculates to 1.8 nF.

With the above values, the loop's natural frequency ($\omega n$), and loop bandwidth ($\omega 3dB$) can be calculated:
$\omega n = \{(Ko/N) \times Ip/(2\pi C)\}^{0.5}$ = 3520 rad/sec.
fn = 3520/2π = 560 Hz.
$\omega 3dB \approx 2 \times \omega n$ = 1120 Hz (valid if $\xi$ = 0.707).

The circuit designer should be cautioned at this point that the above calculated values are not necessarily optimum for every application. Besides the fact that several assumptions were made in the discussion, the equations cannot account for items such as the PC board layout, characteristics of the external divider, and noise from various sources. The above calculated values provide for a functional circuit, which should then be tweaked to obtain minimum jitter at the pixel clock output.

When initially adjusting the filter component values, it is advisable to maintain the same general time constant (400 μs in this example), and the same x10 relationship between C1 and C2.

References:
(1) *Charge–Pump Phase–Lock–Loops* by Floyd M. Gardner, IEEE Transactions on Communications, Vol. com–28, no. 11, Nov. 1980.
(2) *Phaselock Techniques* by Floyd M. Gardner, J. Wiley & Sons, 1979.
(3) *Phase–Locked–Loops* by Roland E. Best, McGraw Hill, 1984.
(4) AN–535, *Phase–Locked–Loop Design Fundamentals*, Motorola.

## GLOSSARY

**Aspect Ratio** – The ratio of the width of a TV screen to the height. In standard TVs, it is 4:3. In HDVT it will likely be 16:9.

**Back Porch** – The blanking time after the sync signal during which the color burst is inserted.

**Blank, Pedestal** – The signal level which is either at black, or slightly more negative than black (“blacker–than–black”), and is used to turn off the screen dot during retrace. Also referred to as the *pedestal*.

**Brightness** – A measure of the dc levels of the luma component. Changing brightness will change the minimum and maximum luma levels together.

**Burst** – The 8 to 10 cycle sine wave which is inserted in the back porch. It’s frequency is the color subcarrier (3.58 MHz or 4.43 MHz), and is used as a phase reference for the color decoder.

**Burst Gate** – A signal identifying the time during which the burst signal occurs.

**C, Chrominance** – The color component of the video signal. The color is determined by the phase of the chrominance component relative to the burst signal.

**Clamping** – A process which establishes a fixed dc voltage level, usually during the back porch time.

**Color Difference Signals** – B–Y, R–Y, also designated as U and V.

**Color Decoder** – A circuit which separates composite video into Red, Blue, and Green, luminance, and sync signals.

**Color Encoder** – A circuit which combines Red, Blue, and Green, luminance, and sync signals into composite video.

**Comb Filter** – A multi–bandpass filter which separates the luma and chrominance components from the video signal, without sacrificing bandwidth.

**Component Video, YUV** – A format whereby the video information is kept as separate luma, R–Y, and B–Y signals *(YUV)*. U is the same as B–Y, and V is the same as R–Y.

**Composite Sync** – A sync signal which combines horizontal and vertical sync information. The waveform is made up of regularly spaced negative going pulses for the horizontal sync, and then half–line pulses and polarity reversal to indicate the vertical sync and retrace time.

**Composite Video** – The video signal which consists of sync, back porch, color burst, video information (luma and chroma), and front porch. This is the signal normally broadcast by TV stations.

**Contrast** – A measure of the difference between minimum and maximum luma amplitudes. Increasing contrast produces a “blacker” black and a “whiter” white.

**dB** – A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P1/P2) for power measurements, and
20 x log (V1/V2) for voltage measurements.

**Field** – One of the two or more equal parts into which a frame is divided in an interlaced system.

**Frame** – The information which makes up one complete picture. It consists of 525 lines in NTSC systems, and 625 lines in PAL systems. An interlaced system is typically composed of two fields.

**Front Porch** – The blanking time immediately before the sync signal.

**Horizontal Sync** – The negative going sync pulses at the beginning of each line. The pulses indicate to the circuit to begin sweeping the dot across the screen.

**Hue** – A measure of the correctness of the colors on a screen.

**Interlaced System** – A method of generating a picture on the screen whereby the even number lines are processed, and then the odd number lines are processed, thereby completing a full picture.

**IRE** – Abbreviation for *International Radio Engineers*, it is the amplitude unit used to define video levels. In standard NTSC signals, blank–to–white is 100 IRE units, and blank–to–sync tip is 40 IRE units. In a 1.0 Vpp signal, one IRE unit is 7.14 mV.

**Luma, Y** – The brightness component of the video signal. Usually abbreviated “Y”, it defines the shade of gray in a black–and–white TV set. In color systems, it is composed of 0.30 red, 0.59 green and 0.11 blue.

**NTSC** – *National Television System Committee*. This committee set the color encoding standards and format for television broadcast in the United States.

**PAL** – *Phase Alternating Line*. A color encoding system in which the burst is alternated 90° each line to help compensate for color errors which may occur during transmission. This system is popular mainly in Europe.

**Pixel** – The smallest picture element, or dot, on a screen. It is determined by the design of the CRT, as well as the system bandwidth.

**R–Y, B–Y** – Referred to as *color difference signals*. These are two of the three signals of component video. When combined with Y, the full color and luminance information is available.

**Retrace** – The rapid movement of the blanked dot from the screen’s right edge to the left edge so it can start scanning a new line. It is also the rapid movement from the lower right corner to the upper left corner during vertical blanking.

**RGB** – The three main colors *(red, blue, green)* used in the acquiring, and subsequent display of a video signal.

**S–VHS** – A format whereby the video information is kept as separate luma and chroma signals (Y and C).

**Sandcastle** – A signal which indicates the horizontal blanking time. It encompasses the front porch, sync, and back porch. Two amplitudes distinguish the front porch + sync time from the back porch.

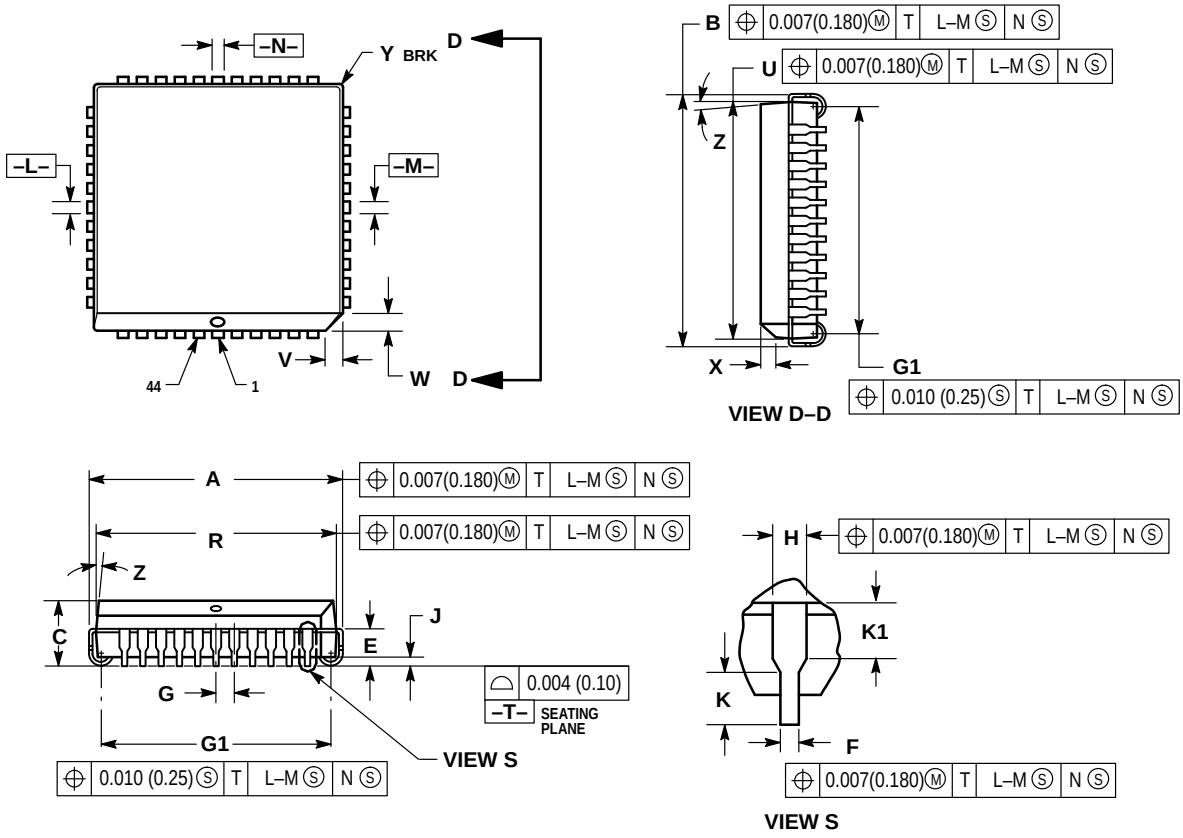
**Saturation** – A measure of the intensity of the color on a screen. Also related to its purity.

**Sync Separator** – A circuit which will detect, and output, the sync signal from a composite video waveform.

**Vertical Sync** – The synchronizing signal which indicates to the circuitry to drive the dot to the upper left corner of the screen, thereby starting a new field. This signal is derived from the composite sync.

## OUTLINE DIMENSIONS

**FN SUFFIX**
PLASTIC PACKAGE
CASE 777–02
(PLCC)
ISSUE C

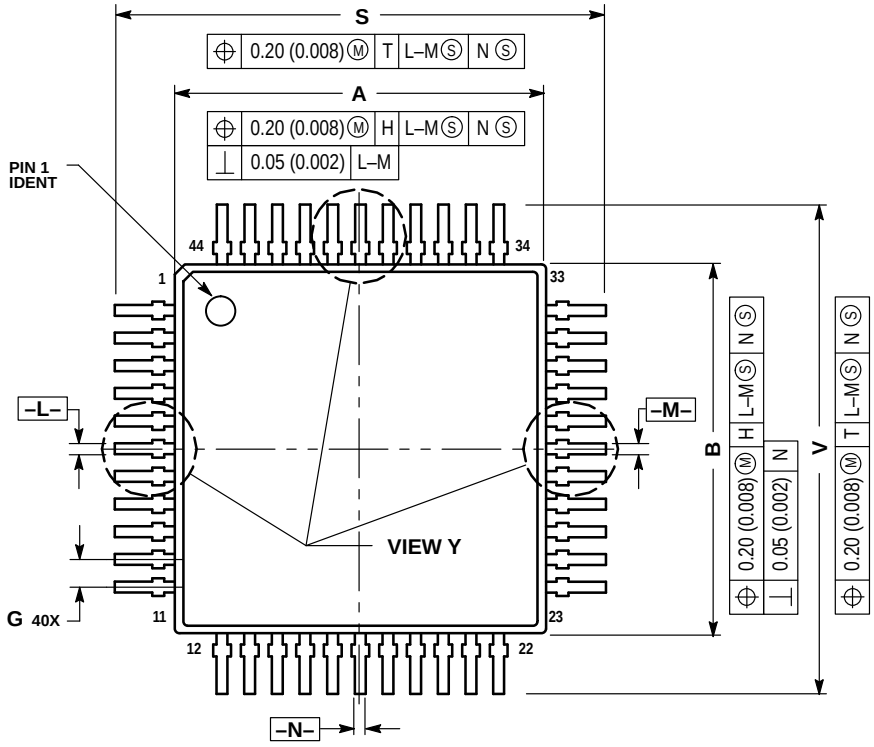


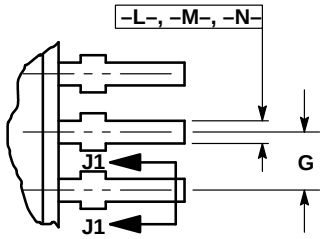

NOTES:
1. DATUMS –L–, –M–, AND –N– ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.685 | 0.695 | 17.40 | 17.65 |
| B | 0.685 | 0.695 | 17.40 | 17.65 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.650 | 0.656 | 16.51 | 16.66 |
| U | 0.650 | 0.656 | 16.51 | 16.66 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.610 | 0.630 | 15.50 | 16.00 |
| K1 | 0.040 | — | 1.02 | — |

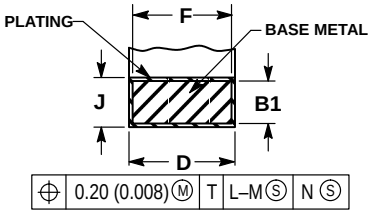
## OUTLINE DIMENSIONS

**FB SUFFIX**
PLASTIC PACKAGE
CASE 824E–02
(QFP)
ISSUE A

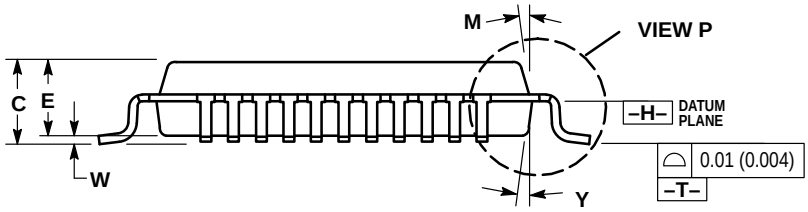


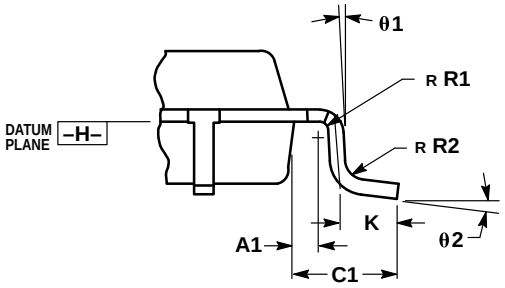




**VIEW Y**
**3 PL**




**SECTION J1–J1**
**44 PL**




**VIEW P**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.90 | 10.10 | 0.390 | 0.398 |
| B | 9.90 | 10.10 | 0.390 | 0.398 |
| C | 2.00 | 2.21 | 0.079 | 0.087 |
| D | 0.30 | 0.45 | 0.0118 | 0.0177 |
| E | 2.00 | 2.10 | 0.079 | 0.083 |
| F | 0.30 | 0.40 | 0.012 | 0.016 |
| G | 0.80 BSC | | 0.031 BSC | |
| J | 0.13 | 0.23 | 0.005 | 0.009 |
| K | 0.65 | 0.95 | 0.026 | 0.037 |
| M | 5° | 10° | 5° | 10° |
| S | 12.95 | 13.45 | 0.510 | 0.530 |
| V | 12.95 | 13.45 | 0.510 | 0.530 |
| W | 0.000 | 0.210 | 0.000 | 0.008 |
| Y | 5° | 10° | 5° | 10° |
| A1 | 0.450 REF | | 0.018 REF | |
| B1 | 0.130 | 0.170 | 0.005 | 0.007 |
| C1 | 1.600 REF | | 0.063 REF | |
| R1 | 0.130 | 0.300 | 0.005 | 0.012 |
| R2 | 0.130 | 0.300 | 0.005 | 0.012 |
| θ1 | 5° | 10° | 5° | 10° |
| θ2 | 0° | 7° | 0° | 7° |

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