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MOTOROLA

MC3479

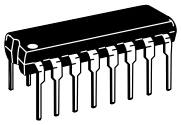
Stepper Motor Driver

STEPPER MOTOR DRIVER

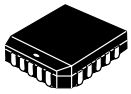
SEMICONDUCTOR TECHNICAL DATA

The MC3479 is designed to drive a two–phase stepper motor in the bipolar mode. The circuit consists of four input sections, a logic decoding/sequencing section, two driver–stages for the motor coils, and an output to indicate the Phase A drive state.

- Single Supply Operation: 7.2 to 16.5 V
- 350 mA/Coil Drive Capability
- Clamp Diodes Provided for Back–EMF Suppression
- Selectable CW/CCW and Full/Half Step Operation
- Selectable High/Low Output Impedance (Half Step Mode)
- TTL/CMOS Compatible Inputs
- Input Hysteresis: 400 mV Minimum
- Phase Logic Can Be Initialized to Phase A
- Phase A Output Drive State Indication (Open–Collector)
- Available in Standard DIP and Surface Mount

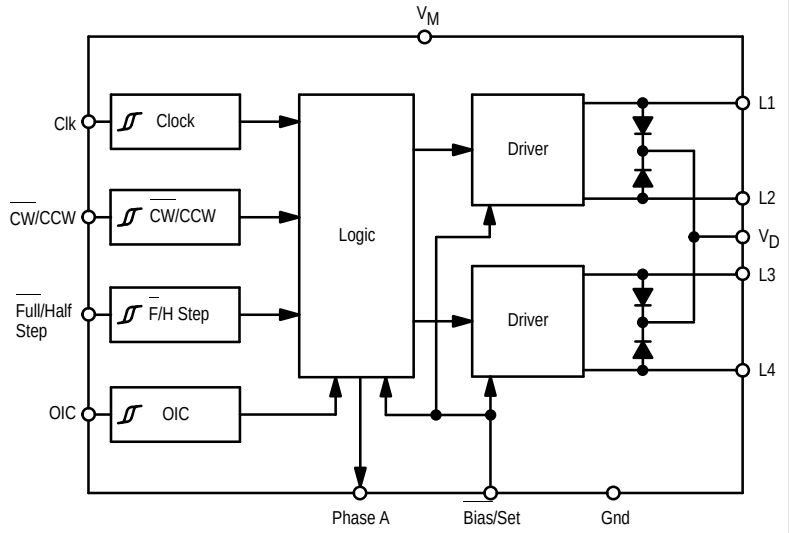


P SUFFIX
PLASTIC PACKAGE
CASE 648C

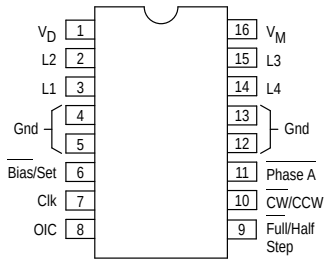


FN SUFFIX
PLASTIC PACKAGE
CASE 775
(PLCC 20)

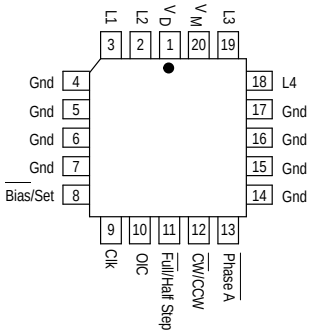
Figure 1. Representative Block Diagram



PIN CONNECTIONS



(Top View)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3479P	T_A = 0° to +70°C	Plastic
MC3479FN		Plastic

INPUT TRUTH TABLE

	Input Low	Input High
CW/CCW	CW	CCW
Full/Half Step	Full Step	Half Step
OIC	Hi Z	Low Z
Clk	Positive Edge Triggered	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_M	+ 18	Vdc
Clamp Diode Cathode Voltage (Pin 1)	V_D	V_M + 5.0	Vdc
Driver Output Voltage	V_{OD}	V_M + 6.0	Vdc
Drive Output Current/Coil	I_{OD}	± 500	mA
Input Voltage (Logic Controls)	V_{in}	– 0.5 to + 7.0	Vdc
Bias/Set Current	I_{BS}	– 10	mA
Phase A Output Voltage	V_{OA}	+ 18	Vdc
Phase A Sink Current	I_{OA}	20	mA
Junction Temperature	T_J	+ 150	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_M	+ 7.2	+ 16.5	Vdc
Clamp Diode Cathode Voltage	V_D	V_M	V_M + 4.5	Vdc
Driver Output Current (Per Coil) (Note 1)	I_{OD}	—	350	mA
Input Voltage (Logic Controls)	V_{in}	0	+ 5.5	Vdc
Bias/Set Current (Outputs Active)	I_{BS}	– 300	– 75	μA
Phase A Output Voltage	V_{OA}	—	V_M	Vdc
Phase A Sink Current	I_{OA}	0	8.0	mA
Operating Ambient Temperature	T_A	0	+ 70	°C

NOTE: 1. See section on Power Dissipation in Application Information.

DC ELECTRICAL CHARACTERISTICS *(Pin numbers refer to the DIP Package)
(Specifications apply over the recommended supply voltage and temperature range, [Notes 2, 3] unless otherwise noted.)

Characteristic	*Pins	Symbol	Min	Typ	Max	Unit
INPUT LOGIC LEVELS						
Threshold Voltage (Low–to–High)	7, 8, 9, 10	V_{TLH}	—	—	2.0	Vdc
Threshold Voltage (High–to–Low)		V_{THL}	0.8	—	—	Vdc
Hysteresis		V_{HYS}	0.4	—	—	Vdc
Current: (V_I = 0.4 V) (V_I = 5.5 V) (V_I = 2.7 V)		I_{IL}	–100 — —	— — —	— +100 +20	μA
DRIVER OUTPUT LEVELS						
Output High Voltage (I_{BS} = – 300 μA): (I_{OD} = – 350 mA) (I_{OD} = – 0.1 mA)	2, 3, 14, 15	V_{OHD}	 V_M – 2.0 V_M – 1.2	 — —	 — —	Vdc
Output Low Voltage (I_{BS} = – 300 μA, I_{OD} = 350 mA)		V_{OLD}	—	—	0.8	Vdc
Differential Mode Output Voltage Difference (Note 4) (I_{BS} = – 300 μA, I_{OD} = 350 mA)		DV_{OD}	—	—	0.15	Vdc
Common Mode Output Voltage Difference (Note 5) (I_{BS} = – 300 μA, I_{OD} = – 0.1 mA)		CV_{OD}	—	—	0.15	Vdc
Output Leakage, Hi Z State (0 ≤ V_{OD} ≤ V_M, I_{BS} = – 5.0 μA) (0 ≤ V_{OD} ≤ V_M, I_{BS} = – 300 μA, F/H = 2.0 V, OIC = 0.8 V)		 I_{OZ1} I_{OZ2}	 – 100 – 100	 — —	 + 100 + 100	μA

NOTES: 2. Algebraic convention rather than absolute values is used to designate limit values.
3. Current into a pin is designated as positive. Current out of a pin is designated as negative.
4. $DV_{OD} = |V_{OD1,2} - V_{OD3,4}|$ where: $V_{OD1,2} = (V_{OHD1} - V_{OLD2})$ or $(V_{OHD2} - V_{OLD1})$, and $V_{OD3,4} = (V_{OHD3} - V_{OLD4})$ or $(V_{OHD4} - V_{OLD3})$.
5. $CV_{OD} = |V_{OHD1} - V_{OHD2}|$ or $|V_{OHD3} - V_{OHD4}|$.

DC ELECTRICAL CHARACTERISTICS *(Pin numbers refer to the DIP Package)
(Specifications apply over the recommended supply voltage and temperature range, [Notes 2, 3] unless otherwise noted.)

Characteristic	*Pins	Symbol	Min	Typ	Max	Unit
CLAMP DIODES						
Forward Voltage (I_D = 350 mA)	1, 2, 3, 14, 15	V_{DF}	—	2.5	3.0	Vdc
Leakage Current (Per Diode) (Pin 1 = 21 V; Outputs = 0 V; I_{BS} = 0 μA)		I_{DR}	—	—	100	μA
PHASE A OUTPUT						
Output Low Voltage (I_{OA} = 8.0 mA)	11	V_{OLA}	—	—	0.4	Vdc
Off State Leakage Current (V_{OHA} = 16.5 V)		I_{OHA}	—	—	100	μA
POWER SUPPLY						
Power Supply Current (I_{OD} = 0 μA, I_{BS} = – 300 μA)	16					mA
($L1 = V_{OHD}$, $L2 = V_{OLD}$, $L3 = V_{OHD}$, $L4 = V_{OLD}$)		I_{MW}	—	—	70	
($L1 = V_{OHD}$, $L2 = V_{OLD}$, L3 = Hi Z, L4 = Hi Z)		I_{MZ}	—	—	40	
($L1 = V_{OHD}$, $L2 = V_{OLD}$, $L3 = V_{OHD}$, $L4 = V_{OHD}$)		I_{MN}	—	—	75	
BIAS/SET CURRENT						
To Set Phase A	6	I_{BS}	– 5.0	—	—	μA

PACKAGE THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction–to–Ambient (No Heatsink)	$R_{\theta JA}$	—	45	—	°C/W

AC SWITCHING CHARACTERISTICS (T_A = + 25°C, V_M = 12 V) (See Figures 2, 3, 4)

Characteristic	*Pins	Symbol	Min	Typ	Max	Unit
Clock Frequency	7	f_{CK}	0	—	50	kHz
Clock Pulse Width (High)	7	PW_{CKH}	10	—	—	μs
Clock Pulse Width (Low)	7	PW_{CKL}	10	—	—	μs
Bias/Set Pulse Width	6	PW_{BS}	10	—	—	μs
Setup Time (CW/CCW and F/HS)	10–7 9–7	t_{su}	5.0	—	—	μs
Hold Time (CW/CCW and F/HS)	10–7 9–7	t_h	10	—	—	μs
Propagation Delay (Clk–to–Driver Output)		t_{PCD}	—	8.0	—	μs
Propagation Delay (Bias/Set–to–Driver Output)		t_{PBSD}	—	1.0	—	μs
Propagation Delay (Clk–to–Phase A Low)	7–11	t_{PHLA}	—	12	—	μs
Propagation Delay (Clk–to–Phase A High)	7–11	t_{PLHA}	—	5.0	—	μs

NOTES: 2. Algebraic convention rather than absolute values is used to designate limit values.
3. Current into a pin is designated as positive. Current out of a pin is designated as negative.

Figure 2. AC Test Circuit

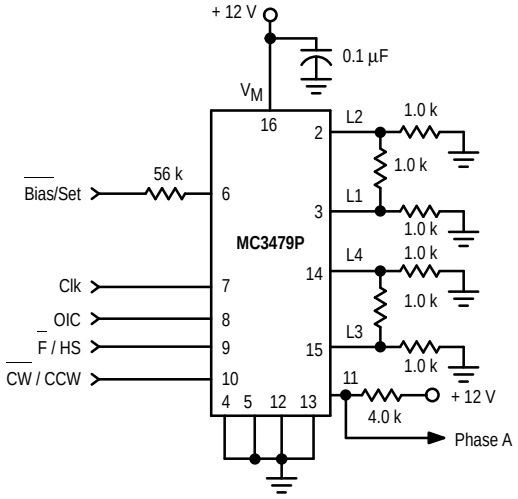
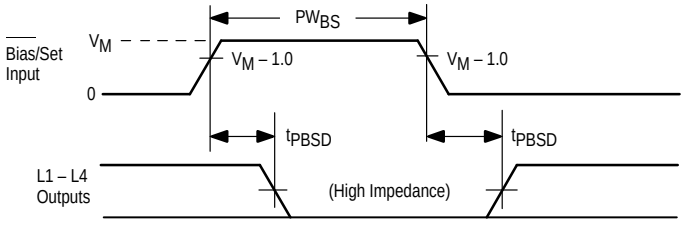


Figure 3. Bias/Set Timing (Refer to Figure 2)



Note: t_r, t_f (10% to 90%) for input signals are ⩽ 25 ns.

PIN FUNCTION DESCRIPTION

Pin No.				
20–Pin	16–Pin	Function	Symbol	Description
20	16	Power Supply	V_M	Power supply pin for both the logic circuit and the motor coil current. Voltage range is + 7.2 to + 16.5 volts.
4, 5, 6, 7, 14, 15, 16, 17	4, 5, 12, 13	Ground	Gnd	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins aids in dissipating heat from within the IC package.
1	1	Clamp Diode Voltage	V_D	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin 16. See Figure 11.
2, 3, 18, 19	2, 3, 14, 15	Driver Outputs	L1, L2 L3, L4	High current outputs for the motor coils. L1 and L2 are connected to one coil, and L3 and L4 to the other coil.
8	6	Bias/Set	B/S	This pin is typically 0.7 volts below V_M. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened (I_{BS} < 5.0 µA) the outputs assume a high impedance condition, while the internal logic presets to a Phase A condition.
9	7	Clock	Clk	The positive edge of the clock input switches the outputs to the next position. This input has no effect if Pin 6 is open.
11	9	Full/Half Step	F/HS	When low (Logic “0”), each clock input pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one–half step. See Figure 7 for sequence.
12	10	Clockwise/ Counterclockwise	CW/CCW	This input allows reversing the rotation of the motor. See Figure 7 for sequence.
10	8	Output Impedance Control	OIC	This input is relevant only in the half step mode (Pin 9 > 2.0 V). When low (Logic “0”), the two driver outputs of the non–energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance referenced to V_M. See Figure 7.
13	11	Phase A	Ph A	This open–collector output indicates (when low) that the driver outputs are in the Phase A condition (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}).

APPLICATION INFORMATION

General

The MC3479 integrated circuit is designed to drive a stepper positioning motor in applications such as disk drives and robotics. The outputs can provide up to 350 mA to each of two coils of a two–phase motor. The outputs change state with each low–to–high transition of the clock input, with the new output state depending on the previous state, as well as the input conditions at the logic controls.

Outputs

The outputs (L1–L4) are high current outputs (see Figure 5), which when connected to a two–phase motor, provide two full–bridge configurations (L3 and L4 are not shown in Figure 5). The polarities applied to the motor coils depend on which transistor (Q_H or Q_L) of each output is on, which in turn depends on the inputs and the decoding circuitry.

Figure 4. Clock Timing
(Refer to Figure 2)

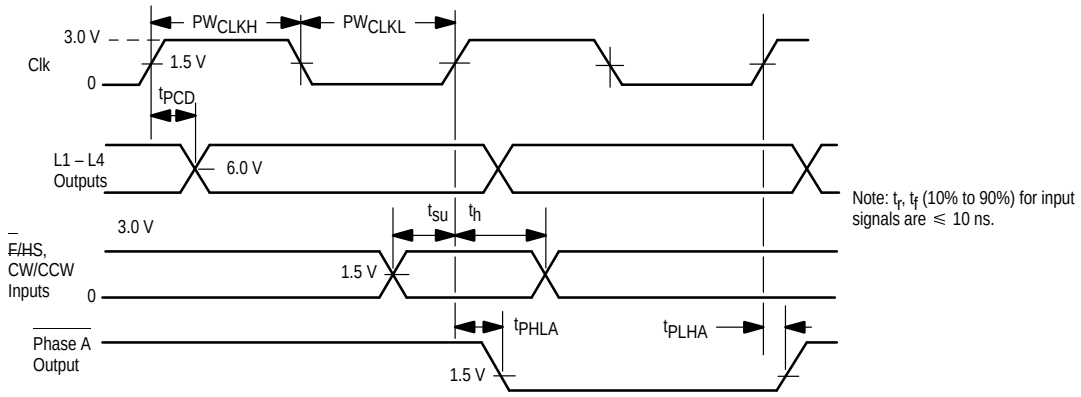
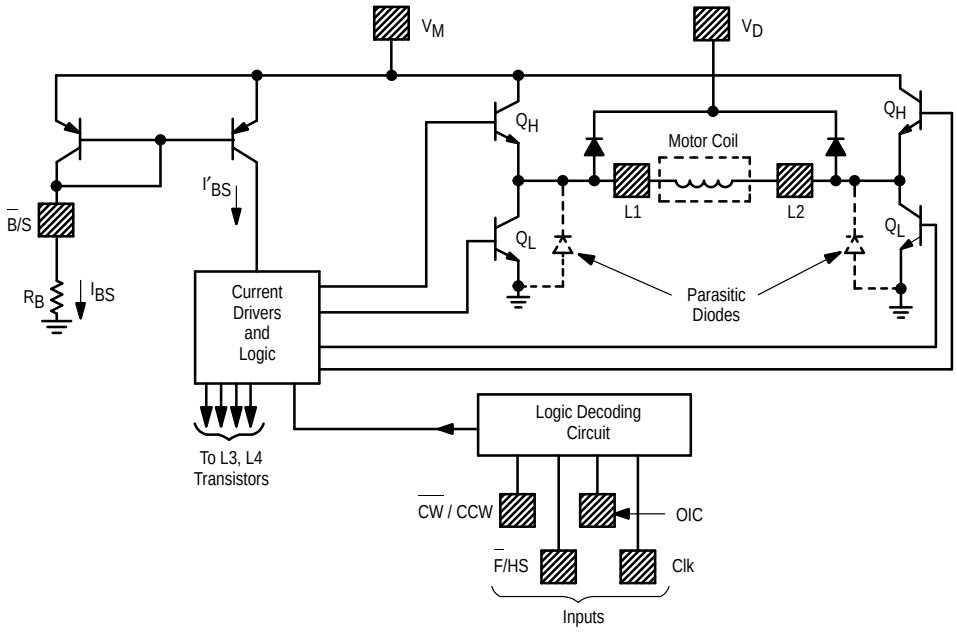


Figure 5. Output Stages

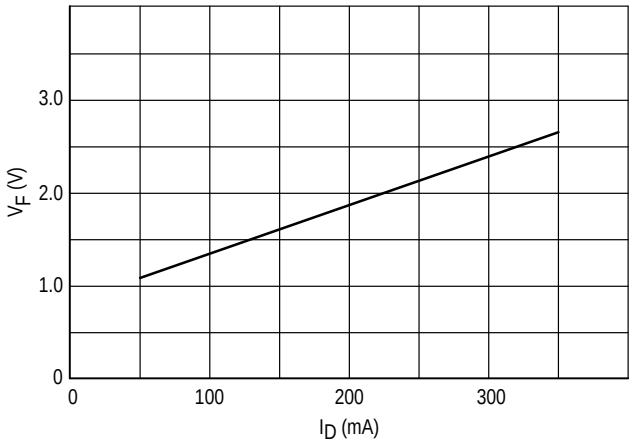


The maximum sink current available at the outputs is a function of the resistor connected between Pin 6 and ground (see section on Bias/Set operation). Whenever the outputs are to be in a high impedance state, both transistors (Q_H and Q_L of Figure 5) of each output are off.

V_D

This pin allows for provision of a current path for the motor coil current during switching, in order to suppress back–EMF voltage spikes. V_D is normally connected to V_M (Pin 16) through a diode (zener or regular), a resistor, or directly. The peaks instantaneous voltage at the outputs must not exceed V_M by more than 6.0 V. The voltage drop across the internal clamping diodes must be included in this portion of the design (see Figure 6). Note the parasitic diodes (Figure 5) across each Q_L of each output provide for a complete circuit path for the switched current.

Figure 6. Clamp Diode Characteristics



Full/Half Step

When this input is at a Logic “0” (<0.8 V), the outputs change a full step with each clock cycle, with the sequence direction depending on the CW/CCW input. There are four steps (Phase A, B, C, D) for each complete cycle of the sequencing logic. Current flows through both motor coils during each step, as shown in Figure 7.

When taken to a Logic “1” (>2.0 V), the outputs change a half step with each clock cycle, with the sequence direction depending on the CW/CCW input. Eight steps (Phase A to H) result for each complete cycle of the sequencing logic. Phase A, C, E and G correspond (in polarity) to Phase A, B, C, and D, respectively, of the full step sequence. Phase B, D, F and H provide current to one motor coil, while de–energizing the other coil. The condition of the outputs of the de–energized coil depends on the OIC input, see Figure 7 timing diagram.

OIC

The output impedance control input determines the output impedance to the de–energized coil when operating in the half–step mode. When the outputs are in Phase B, D, F or H (Figure 7) and this input is at a Logic “0” (<0.8 V), the two outputs to the de–energized coil are in a high impedance condition — Q_L and Q_H of both outputs (Figure 5) are off. When this input is at a Logic “1” (>2.0 V), a low impedance output is provided to the de–energized coil as both outputs have Q_H on (Q_L off). To complete the low impedance path requires connecting V_D to V_M as described elsewhere in this data sheet.

Bias/Set

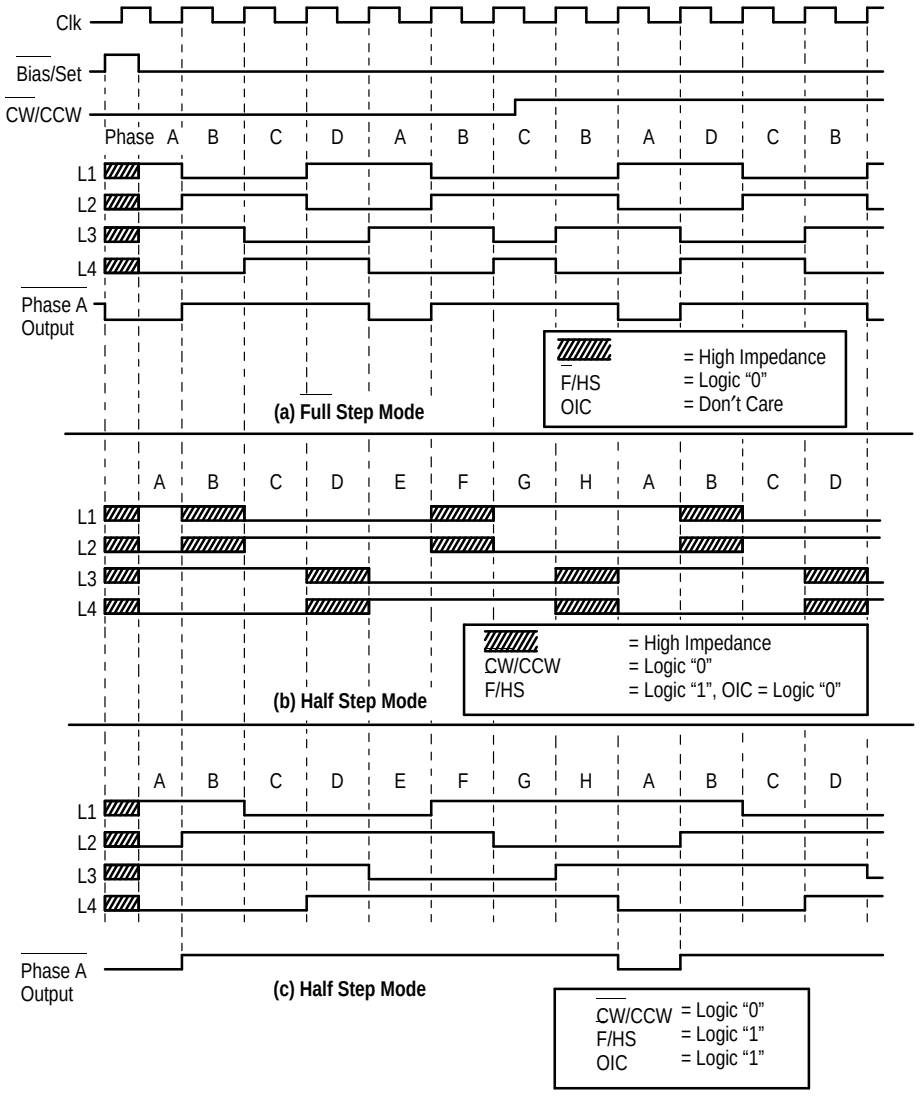
This pin can be used for three functions: a) determining the maximum output sink current; b) setting the internal logic to a known state; and c) reducing power consumption.

a) The maximum output sink current is determined by the base drive current supplied to the lower transistors (Q_Ls of Figure 5) of each output, which in turn, is a function of I_{BS}. The appropriate value of I_{BS} is determined by:

$$I_{BS} = I_{OD} \times 0.86$$

where I_{BS} is in microamps, and I_{OD} is the motor current/coil in milliamps.

Figure 7. Output Sequence



The value of R_B (between this pin and ground) is then determined by:

$$R_B = \frac{V_M - 0.7\ V}{I_{BS}}$$

b) When this pin is opened (raised to V_M) such that I_{BS} is <5.0 μA, the internal logic is set to the Phase A condition, and the four driver outputs are put into a high impedance state. The Phase A output (Pin 11) goes active (low), and input signals at the controls are ignored during this time. Upon re–establishing I_{BS}, the driver outputs become active, and will be in the Phase A position (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}). The circuit will then respond to the inputs at the controls.

The Set function (opening this pin) can be used as a power–up reset while supply voltages are settling. A CMOS logic gate (powered by V_M) can be used to control this pin as shown in Figure 11.

c) Whenever the motor is not being stepped, power dissipation in the IC and in the motor may be lowered by reducing I_{BS}, so as to reduce the output (motor) current. Setting I_{BS} to 75 μA will reduce the motor current, but will not reset the internal logic as described above. See Figure 12 for a suggested circuit.

Power Dissipation

The power dissipated by the MC3479 must be such that the junction temperature (T_J) does not exceed 150°C. The power dissipated can be expressed as:

$$P = (V_M \times I_M) + (2 \times I_{OD})\ [(V_M - V_{OHD}) + V_{OLD}]$$

where V_M = Supply voltage;
I_M = Supply current other than I_{OD};
I_{OD} = Output current to each motor coil;
V_{OHD} = Driver output high voltage;
V_{OLD} = Driver output low voltage.

The power supply current (I_M) is obtained from Figure 8. After the power dissipation is calculated, the junction temperature can be calculated using:

$$T_J = (P \times R_{\theta JA}) + T_A$$

where $R_{\theta JA}$ = Junction–to–ambient thermal resistance (52°C/W for the DIP, 72°C/W for the FN Package);
T_A = Ambient Temperature.

For example, assume an application where V_M = 12 V, the motor requires 200 mA/coil, operating at room temperature with no heatsink on the IC. I_{BS} is calculated:

$I_{BS} = 200 \times 0.86$
$I_{BS} = 172\ \mu A$

R_B is calculated:

$R_B = (12 - 0.7)\ V/172\ \mu A$
$R_B = 65.7\ k\Omega$

From Figure 8, I_M (max) is determined to be 40 mA. From Figure 9, V_{OLD} is 0.46 volts, and from Figure 10, ($V_M - V_{OHD}$) is 1.4 volts.

$P = (12 \times 0.040) + (2 \times 0.2)\ (1.4 + 0.46)$
$P = 1.22\ W$
$T_J = (1.22\ W \times 52°C/W) + 25°C$
$T_J = 88°C$

This temperature is well below the maximum limit. If the calculated T_J had been higher than 150°C, a heatsink such as the Staver Co. V–7 Series, Aavid #5802, or Thermalloy #6012 could be used to reduce $R_{\theta JA}$. In extreme cases, forced air cooling should be considered.

The above calculation, and $R_{\theta JA}$, assumes that a ground plane is provided under the MC3479 (either or both sides of the PC board) to aid in the heat dissipation. Single nominal width traces leading from the four ground pins should be avoided as this will increase T_J, as well as provide potentially disruptive ground noise and I_R drops when switching the motor current.

Figure 8. Power Supply Current

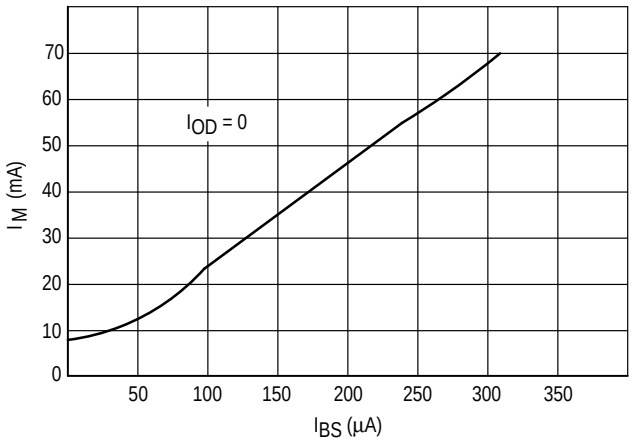


Figure 9. Maximum Saturation Voltage — Driver Output Low

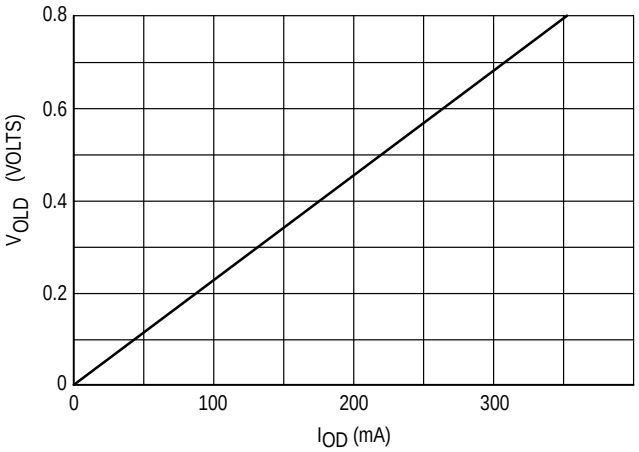


Figure 10. Maximum Saturation Voltage — Driver Output High

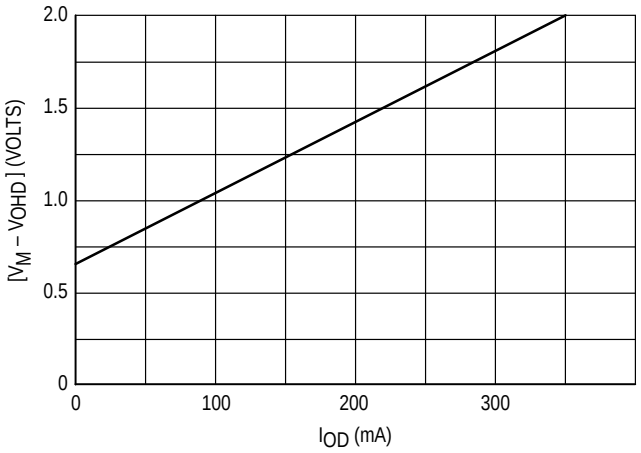


Figure 11. Typical Applications Circuit

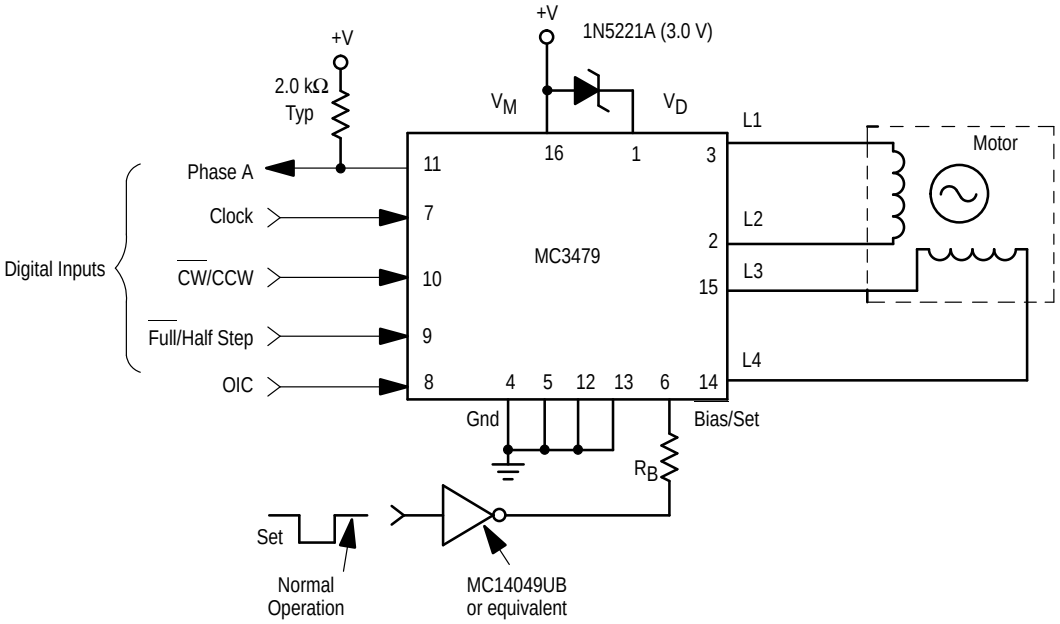
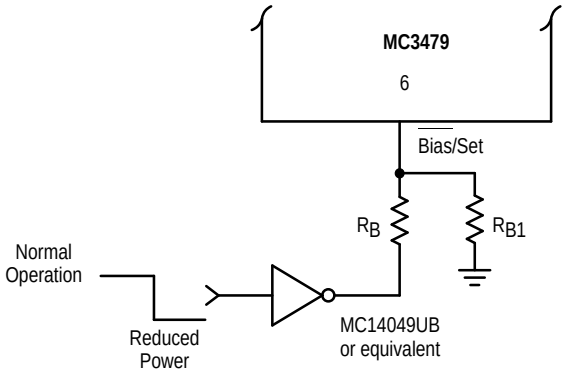


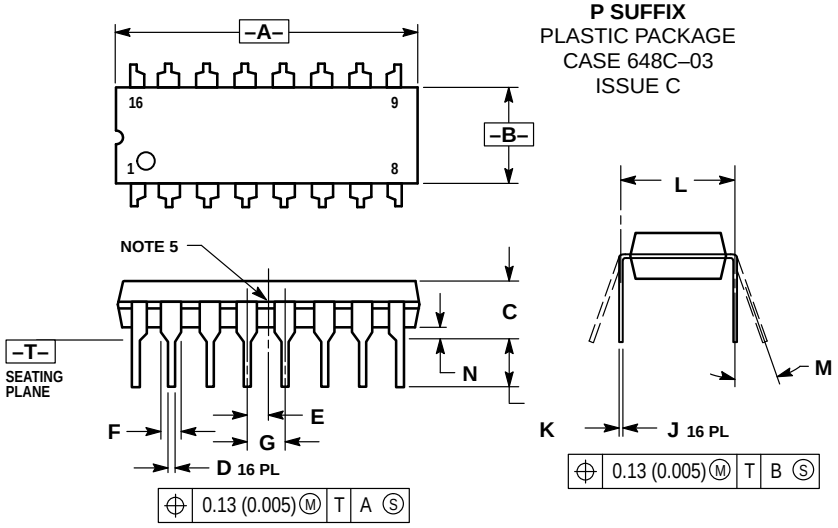
Figure 12. Power Reduction



— Suggested value for R_{B1} (V_M = 12 V) is 150 kΩ.
— R_B calculation (see text) must take into account the current through R_{B1}.

OUTLINE DIMENSIONS

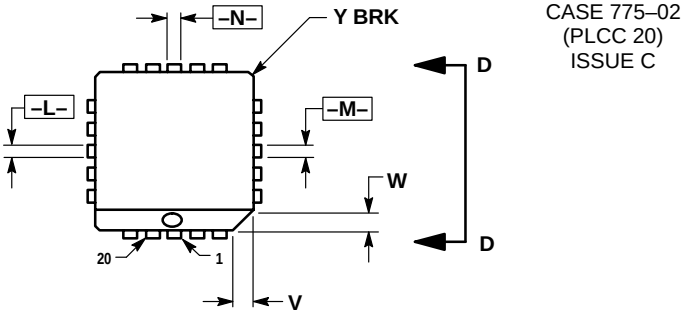
P SUFFIX
PLASTIC PACKAGE
CASE 648C–03
ISSUE C

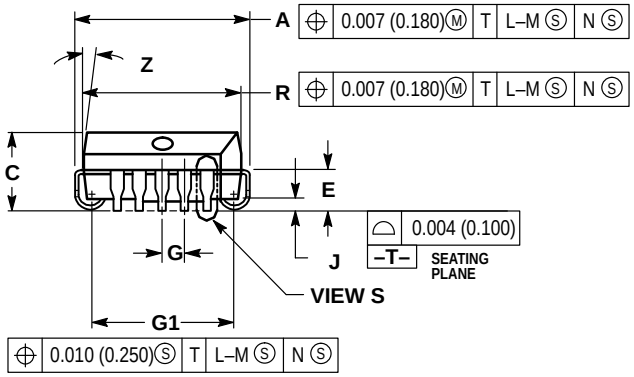


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. INTERNAL LEAD CONNECTION BETWEEN 4 AND 5, 12 AND 13.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.840	18.80	21.34
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
E	0.050 BSC		1.27 BSC	
F	0.040	0.70	1.02	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0 °	10 °	0 °	10 °
N	0.015	0.040	0.39	1.01

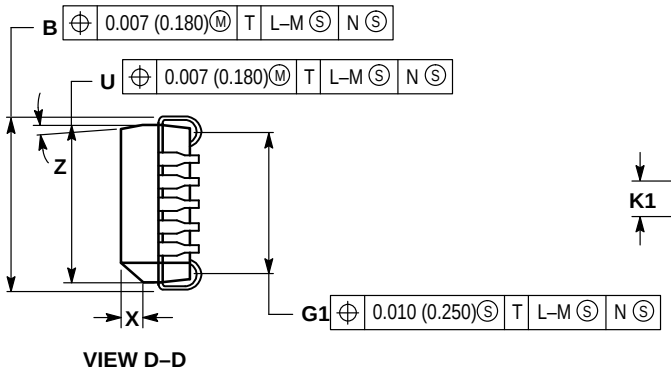
FN SUFFIX
PLASTIC PACKAGE
CASE 775–02
(PLCC 20)
ISSUE C

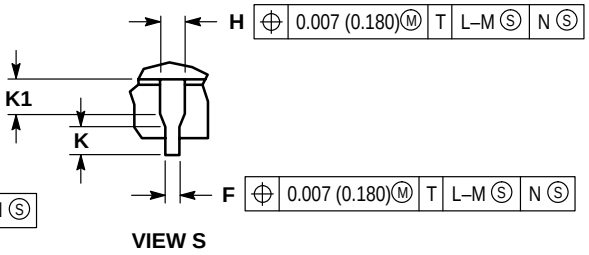




NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—





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