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MOTOROLA

# MC3450

# Quad MTTL Compatible Line Receivers

The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three–state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

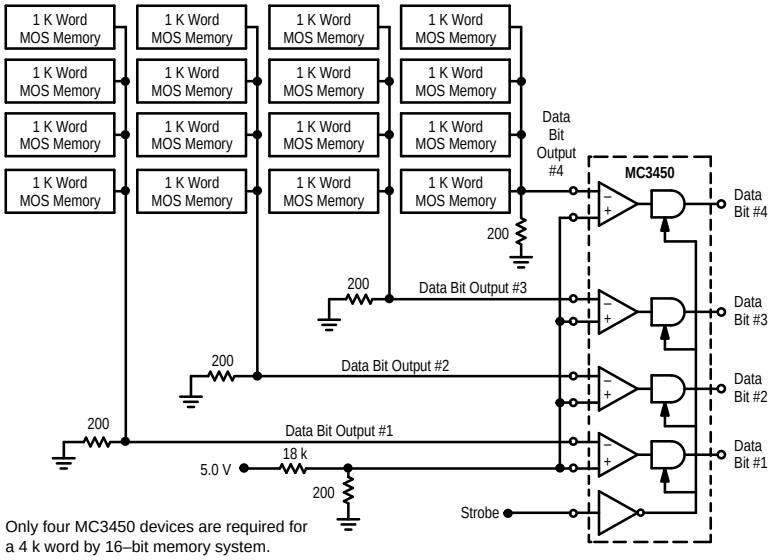
- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied “AND” Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier

**TRUTH TABLE**

| Input | Strobe | Output MC3450 |
|---|---|---|
| $V_{ID} \geq$ + 25 mV | L | H |
| | H | Z |
| – 25 mV $\leq V_{ID} \leq$ + 25 mV | L | I |
| | H | Z |
| $V_{ID} \leq$ – 25 mV | L | L |
| | H | Z |

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

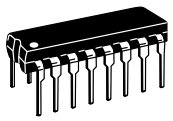
**Figure 1. A Typical MOS Memory Sensing Application for a 4 k Word by 4–Bit Memory Arrangement Employing 1103 Type Memory Devices**




Only four MC3450 devices are required for a 4 k word by 16–bit memory system.

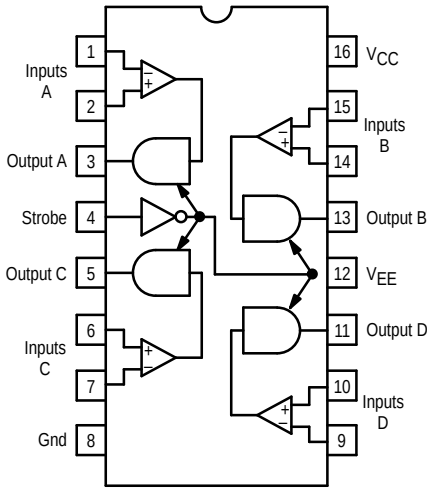
## QUAD LINE RECEIVERS WITH COMMON THREE–STATE STROBE INPUT

**SEMICONDUCTOR TECHNICAL DATA**



**P SUFFIX**
PLASTIC PACKAGE
CASE 648

**PIN CONNECTIONS**




**ORDERING INFORMATION**

| Device | Operating Temperature Range | Package |
|---|---|---|
| MC3450P | $T_A$ = 0 to +70°C | Plastic DIP |

**MAXIMUM RATINGS** ($T_A$ = 0 to +70°C, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages | $V_{CC}$, $V_{EE}$ | ±7.0 | Vdc |
| Differential Mode Input Signal Voltage Range | $V_{IDR}$ | ±6.0 | Vdc |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±5.0 | Vdc |
| Strobe Input Voltage | $V_{I(S)}$ | 5.5 | Vdc |
| Power Dissipation (Package Limitation)<br>Ceramic Dual In–Line Package<br>Derate above $T_A$ = 25°C<br>Plastic Dual In–Line Package<br>Derate above $T_A$ = 25°C | $P_D$ | <br>1000<br>6.6<br>1000<br>6.6 | <br>mW<br>mW/°C<br>mW<br>mW/°C |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |

**RECOMMENDED OPERATING CONDITIONS** ($T_A$ = 0 to +70°C, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +4.75<br>–4.75 | +5.0<br>–5.0 | +5.25<br>–5.25 | Vdc |
| Output Load Current | $I_{OL}$ | – | – | 16 | mA |
| Differential Mode Input Voltage Range | $V_{IDR}$ | –5.0 | – | +5.0 | Vdc |
| Common Mode Input Voltage Range | $V_{ICR}$ | –3.0 | – | +3.0 | Vdc |
| Input Voltage Range (any input to Ground) | $V_{IR}$ | –5.0 | – | +3.0 | Vdc |

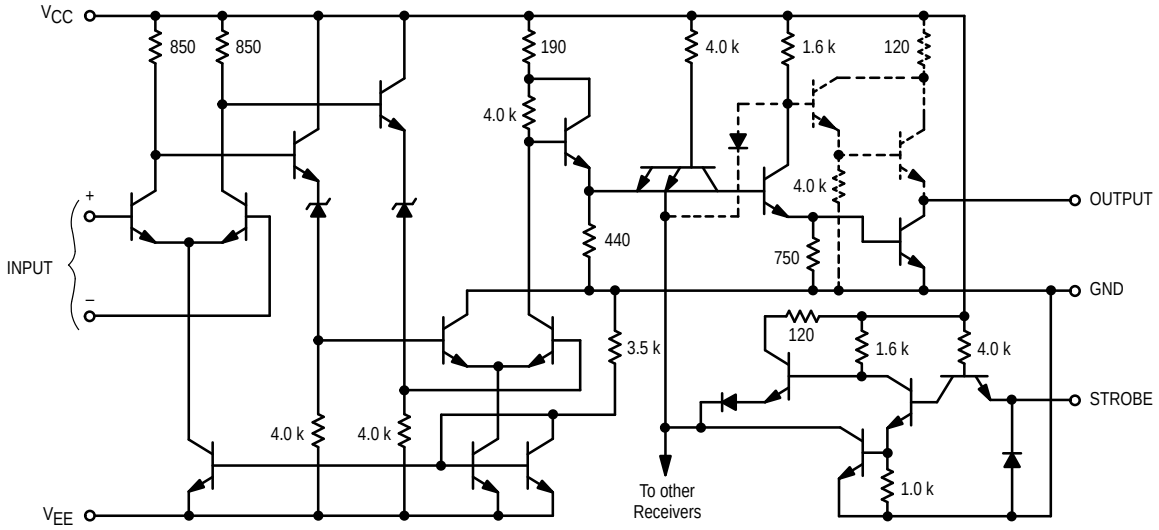
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = –5.0 Vdc, $T_A$ = 0 to +70°C, unless otherwise noted.)

| Characteristic | Symbol | MC3450 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| High Level Input Current to Receiver Input | $I_{IH(I)}$ | – | – | 75 | µA |
| Low Level Input Current to Receiver Input | $I_{IL(I)}$ | – | – | –10 | µA |
| High Level Input Current to Strobe Input<br>$V_{IH(S)}$ = 2.4 V<br>$V_{IH(S)}$ = 5.25 V | $I_{IH(S)}$ | <br>–<br>– | <br>–<br>– | <br>40<br>1.0 | <br>µA<br>mA |
| Low Level Input Current to Strobe Input<br>$V_{IL(S)}$ = 0.4 V | $I_{IL(S)}$ | – | – | –1.6 | mA |
| High Level Output Voltage | $V_{OH}$ | 2.4 | – | – | Vdc |
| High Level Output Leakage Current | $I_{CEX}$ | – | – | – | µA |
| Low Level Output Voltage | $V_{OL}$ | – | – | 0.5 | Vdc |
| Short–Circuit Output Current | $I_{OS}$ | –18 | – | –70 | mA |
| Output Disable Leakage Current | $I_{off}$ | – | – | 40 | µA |
| High Logic Level Supply Current from $V_{CC}$ | $I_{CCH}$ | – | 45 | 60 | mA |
| High Logic Level Supply Current from $V_{EE}$ | $I_{EEH}$ | – | –17 | –30 | mA |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = –5.0 Vdc, $T_A$ = +25°C, unless otherwise noted.)

| Characteristic | Symbol | MC3450 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| High to Low Logic Level Propagation Delay Time (Differential Inputs) | $t_{PHL(D)}$ | – | – | 25 | ns |
| Low to High Logic Level Propagation Delay Time (Differential Inputs) | $t_{PLH(D)}$ | – | – | 25 | ns |
| Open State to High Logic Level Propagation Delay Time (Strobe) | $t_{PZH(S)}$ | – | – | 21 | ns |
| High Logic Level to Open State Propagation Delay Time (Strobe) | $t_{PHZ(S)}$ | – | – | 18 | ns |
| Open State to Low Logic Level Propagation Delay Time (Strobe) | $t_{PZL(S)}$ | – | – | 27 | ns |
| Low Logic Level to Open State Propagation Delay Time (Strobe) | $t_{PLZ(S)}$ | – | – | 29 | ns |
| High Logic to Low Logic Level Propagation Delay Time (Strobe) | $t_{PHL(S)}$ | – | – | – | ns |
| Low Logic to High Logic Level Propagation Delay Time (Strobe) | $t_{PLH(S)}$ | – | – | – | ns |

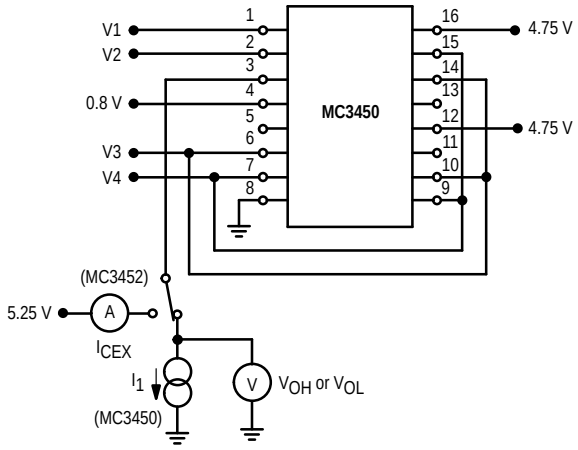
**Figure 2. Circuit Schematic**
(1/4 Circuit Shown)




Dashed components apply to the MC3450 circuit only.

## TEST CIRCUITS

**Figure 3. $I_{CEX}$, $V_{OH}$, and $V_{OL}$**




**TEST TABLE**

| | V1 | V2 | V3 | V4 | |
|---|---|---|---|---|---|
| | MC3450 | MC3450 | MC3450 | MC3450 | I1 |
| $V_{OH}$ | 2.975 V | 3.0 V | 3.0 V | GND | 0.4 mA |
| | –3.0 V | –2.975 V | GND | –3.0 V | |
| $I_{CEX}$ | | – | – | – | – |
| | | – | – | – | – |
| $V_{OL}$ | 3.0 V | 2.975 V | GND | 3.0 V | –16 mA |
| | –2.975 V | –3.0V | –3.0 V | GND | |

Channel A shown under test. Other channels are tested similarly.

**Figure 4. $I_{CCH}$ and $I_{EEH}$**

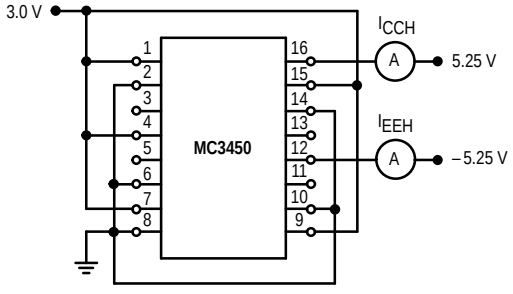
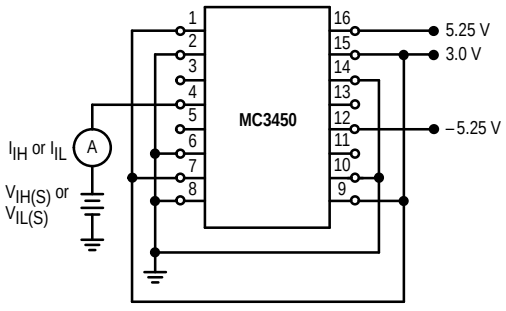
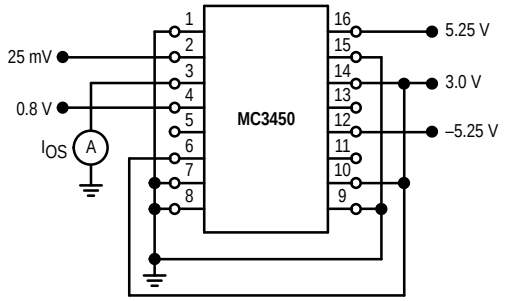



**Figure 5. $I_{IH(S)}$ and $I_{IL(S)}$**



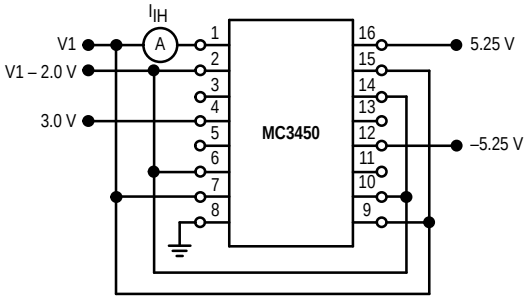
**TEST CIRCUITS** (continued)

**Figure 6. $I_{OS}$**



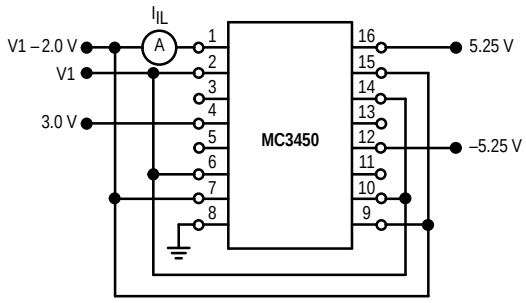

Channel A shown under test, other channels are tested similarly.
Only one output shorted at a time.

**Figure 7. $I_{IH}$**



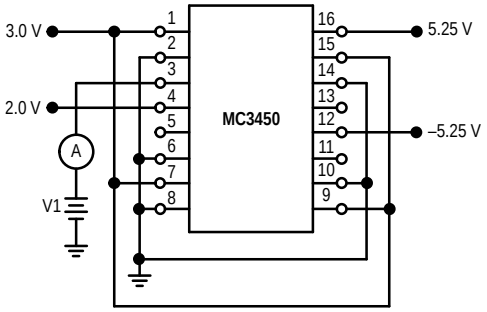

Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from 3.0 V to – 3.0 V.

**Figure 8. $I_{IL}$**



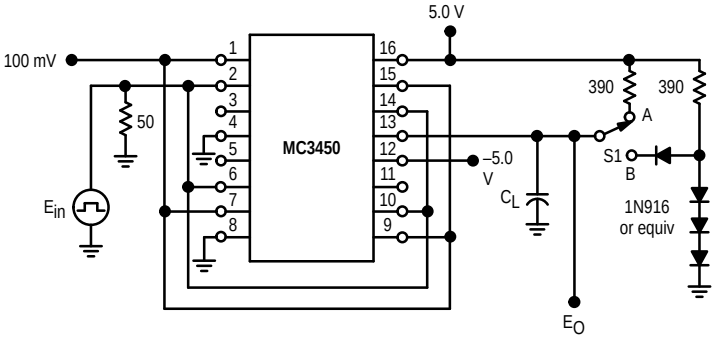

Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from 3.0 V to – 3.0 V.

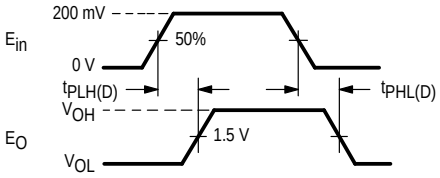
**Figure 9. $I_{off}$**




Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4 V and 2.4 V.

**Figure 10. Receiver Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$**



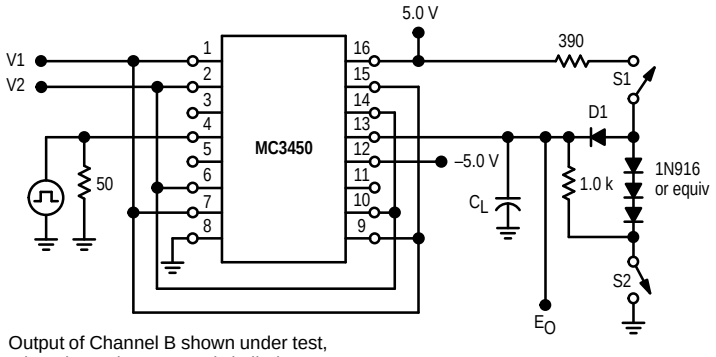




Output of Channel B shown under test, other channels are tested similarly.
S1 at “A” for MC3452
S1 at “B” for MC3450
$C_L$ = 15 pF total for MC3452
$C_L$ = 50 pF total for MC3450

$E_{in}$ waveform characteristics:
$t_{TLH}$ and $t_{THL}$ ⩽ 10 ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

**TEST CIRCUITS** (continued)

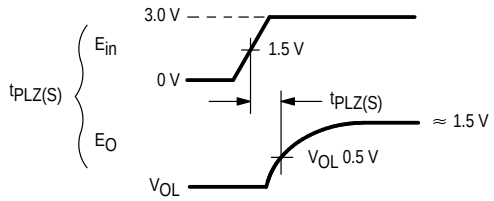
**Figure 11. Strobe Propagation Delay Times $t_{PLZ(S)}$ $t_{PZL(S)}$ $t_{PHZ(S)}$ and $t_{PZH(S)}$**

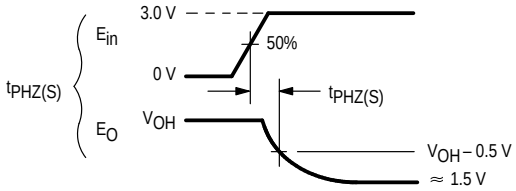


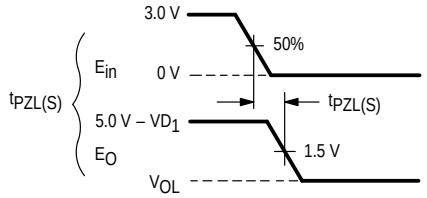

Output of Channel B shown under test,
other channels are tested similarly.

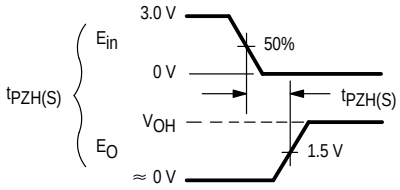
| | V1 | V2 | S1 | S2 | $C_L$ |
|---|---|---|---|---|---|
| $t_{PLZ(S)}$ | 100 mV | GND | Closed | Closed | 15 pF |
| $t_{PZL(S)}$ | 100 mV | GND | Closed | Open | 50 pF |
| $t_{PHZ(S)}$ | GND | 100 mV | Closed | Closed | 15 pF |
| $t_{PZH(S)}$ | GND | 100 mV | Open | Closed | 50 pF |

$C_L$ includes jig and probe capacitance.
$E_{in}$ waveform characteristics:
$t_{TLH}$ and $t_{THL}$ ≤ 10 ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%



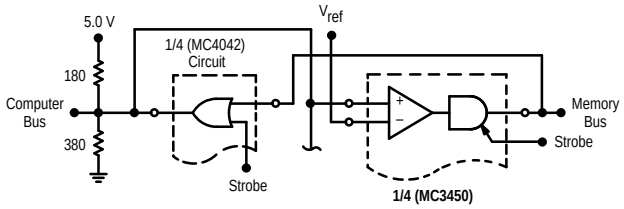



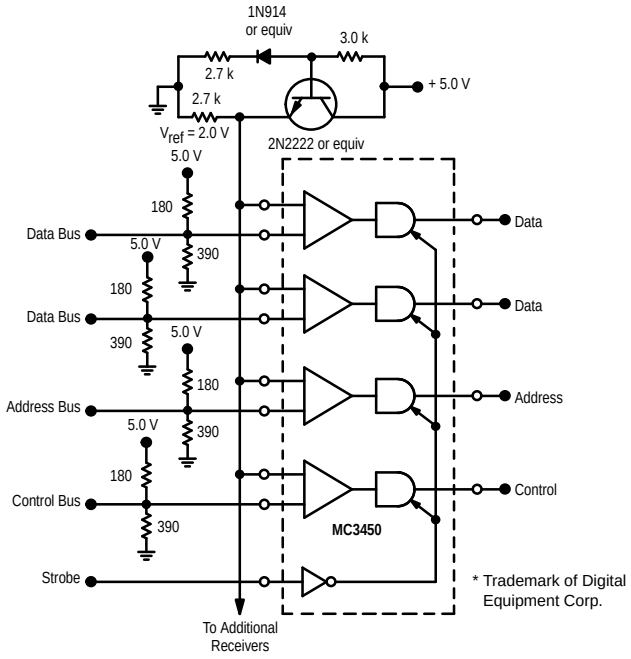
## APPLICATIONS INFORMATION

### Figure 12. Bidirectional Data Transmission




The three–state capability of the MC3450 permits bidirectional data transmission as illustrated.

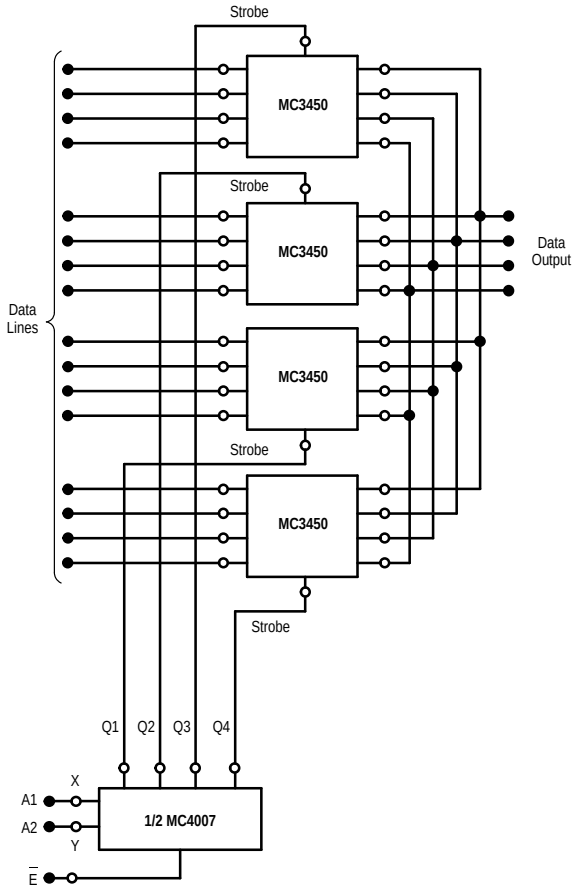
### Figure 13. Single–Ended Uni–Bus™ Line Receiver Application for Minicomputer




* Trademark of Digital Equipment Corp.

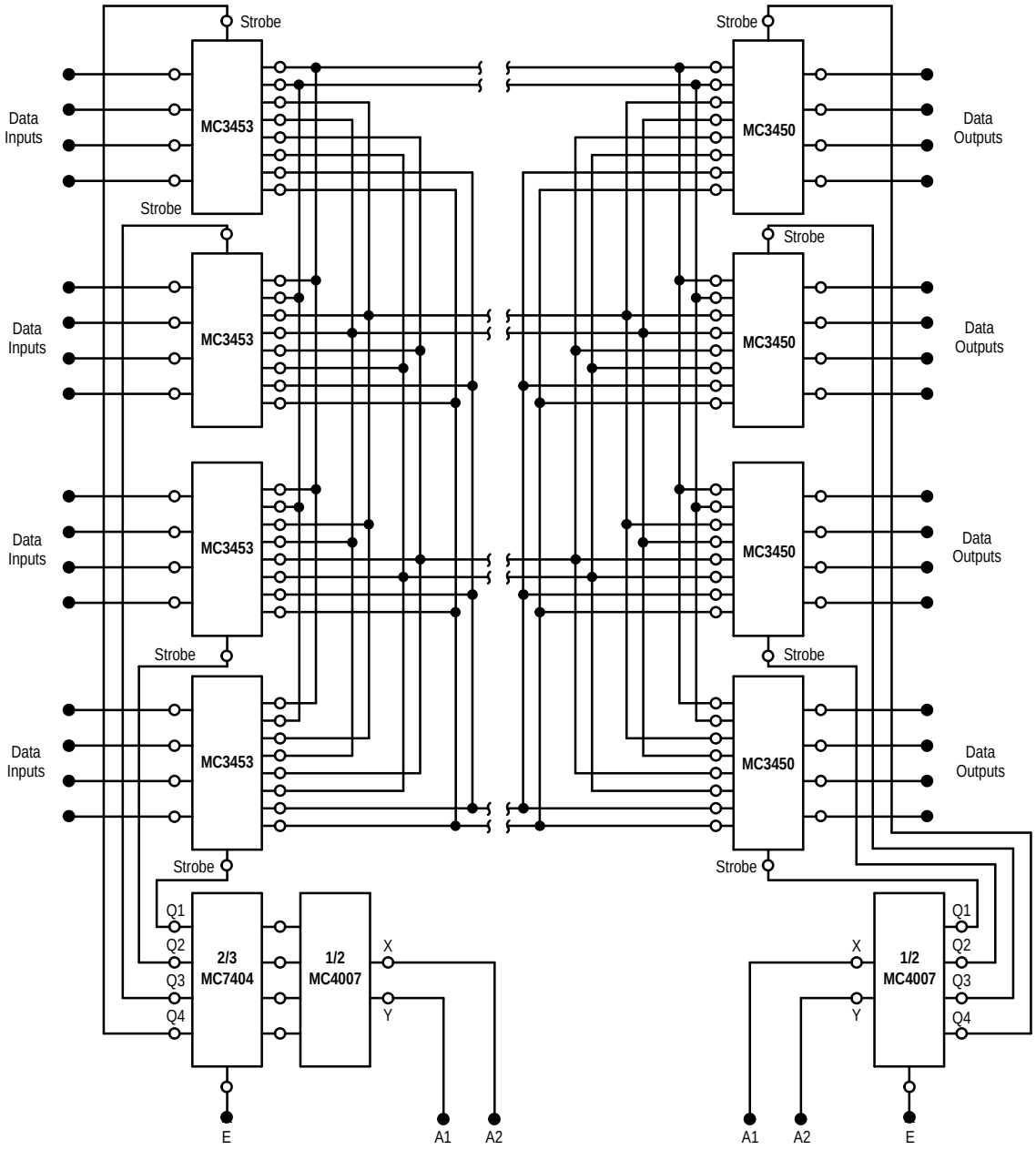
The MC3450 can be used for single–ended as well as differential line receiving. For single–ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used. The voltage source, which generates $V_{ref}$, should be designed so that the $V_{ref}$ voltage is halfway between $V_{OH}$(min) and $V_{OL}$(max). The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum. This low–input overdrive enhances differential noise immunity. Also the high–input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects.

### Figure 14. Wired "OR" Data Selection Using Three–State Logic



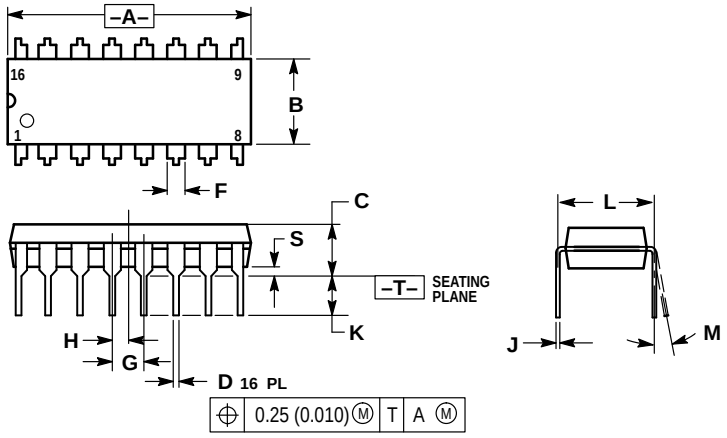
**APPLICATIONS INFORMATION** (continued)

**Figure 15. Party–Line Data Transmission System with Multiplex Decoding**



## OUTLINE DIMENSIONS

**P SUFFIX**
PLASTIC PACKAGE
CASE 648–08
ISSUE R




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |



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