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MOTOROLA

MC3430, MC3431

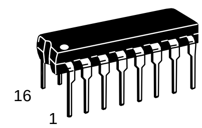
Quad, Differential Voltage Comparator/Sense Amplifiers

The MC3430 thru MC3433 high speed comparators are ideal for applications as sense amplifiers in MOS memory systems. They are specified in a unique way which combines the effects of input offset voltage, input offset current, voltage gain, temperature variations and input common mode range into a single functional parameter. This parameter, called Input Sensitivity, specifies a minimum differential input voltage which will guarantee a given logic state. Four variations are offered in the comparator series.

The MC3430 and MC3431 versions feature a three–state strobe input common to all four channels which can be used to place the four outputs in a high impedance state. These two devices use active pull–up MTTL compatible outputs. The MC3432 and MC3433 are open–collector types which permit the implied AND connection. The MC3430 and MC3432 versions are specified for a ±7.0 mV input sensitivity over the 0° to 70°C temperature range, while the MC3431 and MC3433 are specified for ±12 mV.

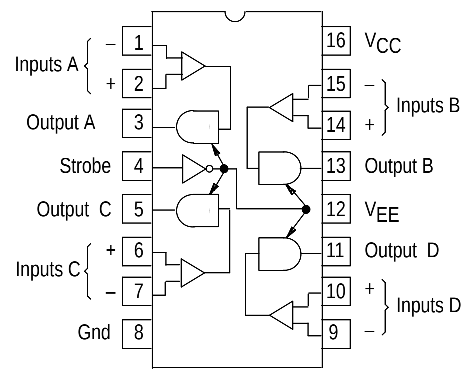
- Propagation Delay Time: 40 ns
- Outputs Specified for a Fanout of 10 (MC7400 Type Loads)
- Specified for All Conditions of ±5% Power Supply Variations, Operating Temperature Range, Input Common Mode Voltage Swing from: –3.0 V to +3.0 V, and $R_S \leq 200\ \Omega$.

QUAD HIGH SPEED VOLTAGE COMPARATORS



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS

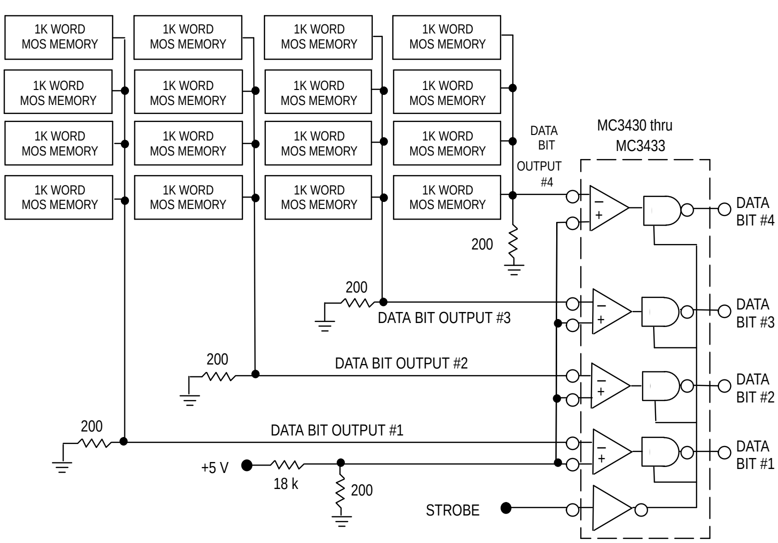


TRUTH TABLE

Input	Strobe	Output	Device
$V_{ID} \geq 7.0$ mV, $T_A = 0°$ to $70°C$	I	H	MC3430P
	H	Z	
	L	Off	
	H	Off	
$-7.0\ mV \leq V_{ID} \leq 7.0$ mV, $T_A = 0°$ to $70°C$	L	I	MC3430P
	H	Z	
	L	I	
	H	Off	
$V_{ID} \leq -7.0$ mV, $T_A = 0°$ to $70°C$	L	L	MC3430P
	H	Z	
	L	On	
	H	Off	
$V_{ID} \geq 12$ mV, $T_A = 0°$ to $70°C$	L	H	MC3431P
	H	Z	
	L	Off	
	H	Off	
$-12\ mV \leq V_{ID} \leq +12$ mV, $T_A = 0°$ to $70°C$	L	I	MC3431P
	H	Z	
	L	I	
	H	Off	
$V_{ID} \leq -12$ mV, $T_A = 0°$ to $70°C$	L	L	MC3431P
	H	Z	
	L	On	
	H	Off	

L = Low Logic State Z = Third (High Impedance)
H = High Logic State I = Indeterminate State
$R_S \leq 200\ \Omega$

Figure 1. A Typical MOS Memory Sensing Application for a 4K Word by 4–Bit Memory Arrangement Employing 1103 Type Memory Devices



Only four devices are required for a 4k word by 4–bit memory system.

MAXIMUM RATINGS (T_A = 0° to +70°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±7.0	Vdc
Differential Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Output Voltage (MC3432, MC3433)	V_O	±7.0	Vdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0° to +70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	±4.75 –4.75	±5.0 –5.0	±5.25 –5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential Mode Input Voltage Range	V_{IDR}	–5.0	–	+5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	–3.0	–	+3.0	Vdc
Input Voltage Range (any Input to Ground)	V_{IR}	–5.0	–	+3.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = –5.0 Vdc, T_A = 0° to +70°C, typical values are measured at T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3430, MC3431			MC3432, MC3433			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Sensitivity (See Discussion on next page) (R_S ≤ 200 Ω) (Common Mode Voltage Range = –3.0 V ≤ V_{in} ≤ 3.0 V)	V_{IS}							mV
4.75 ≤ V_{CC} ≤ 5.25 V, T_A = 25°C; MC3430, MC3432		–	–	±6.0	–	–	±6.0	
–4.75 ≥ V_{EE} ≥ –5.25 V, T_A = 25°C; MC3431, MC3433		–	–	±10	–	–	±10	
(Common Mode Voltage Range = –3.0 V ≤ V_{in} ≤ 3.0 V) 4.75 ≤ V_{CC} ≤ 5.25 V, T_A = 0° to 70°C; MC3430, MC3432		–	–	±7.0	–	–	±7.0	
–4.75 ≥ V_{EE} ≥ –5.25 V, T_A = 0° to 70°C; MC3431, MC3433		–	–	±12	–	–	±12	
Input Offset Voltage (R_S ≤ 200 Ω)	V_{IO}	–	2.0	–	–	2.0	–	mV
Input Bias Current	I_B							µA
(V_{CC} = 5.25 V, V_{EE} = –5.25 V) MC3430, MC3432		–	20	40	–	20	40	
MC3431, MC3433		–	20	40	–	20	40	
Input Offset Current	I_{IO}	–	1.0	–	–	1.0	–	µA
Voltage Gain	A_{VOL}	–	1200	–	–	1200	–	V/V
Strobe Input Voltage (Low State)	$V_{IL(S)}$	–	–	0.8	–	–	0.8	V
Strobe Input Voltage (High State)	$V_{IH(S)}$	2.0	–	–	2.0	–	–	V
Strobe Current (Low State) (V_{CC} = 5.25 V, V_{EE} = –5.25 V, V_{in} = 0.4 V)	$I_{IL(S)}$	–	–	–1.6	–	–	–1.6	mA
Strobe Current (High State)	$I_{IH(S)}$							
(V_{CC} = 5.25 V, V_{EE} = –5.25 V, V_{in} = 2.4 V)		–	–	40	–	–	40	µA
(V_{CC} = 5.25 V, V_{EE} = –5.25 V, V_{in} = 5.25 V)		–	–	1.0	–	–	1.0	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = –5.0 Vdc, T_A = 0° to +70°C, typical values are measured at T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3430, MC3431			MC3432, MC3433			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (High State) (I_O = –400 μA, V_{CC} = 4.75 V, V_{EE} = –4.75 V)	V_{OH}	2.4	–	–	–	–	–	V
Output Voltage (Low State) (I_O = 16 mA, V_{CC} = 4.75 V, V_{EE} = 4.75 V)	V_{OL}	–	–	0.4	–	–	0.4	V
Output Leakage Current (V_{CC} = 4.75 V, V_{EE} = –4.75 V, V_O = 5.25 V)	I_{CEX}	–	–	–	–	–	250	μA
Output Current Short Circuit (V_{CC} = 5.25 V, V_{EE} = –5.25 V)	I_{SC}	–18	–	–70	–	–	–	mA
Output Disable Leakage Current (V_{CC} = 5.25 V, V_{EE} = –5.25 V)	I_{off}	–	–	40	–	–	–	μA
High Logic Level Supply Currents (V_{CC} = 5.25 V, V_{EE} = –5.25 V)	I_{CC} I_{EE}	– –	+45 –17	+60 –30	– –	+45 –17	+60 –20	mA mA

A UNIQUE FUNCTIONAL PARAMETER FOR COMPARATORS

A unique approach is used in specifying the MC3430 to MC3433 quad comparators. Previously, comparators have been specified as analog devices with common operational amplifier type parameters such as voltage gain (A_{VOL}), input offset voltage (V_{IO}), input offset current (I_{IO}) and common mode rejection (CMR). This is true despite the fact that most comparators are seldom operated in their analog region because it is difficult to hold a high gain comparator in this narrow region. Comparators are normally used to "detect" when an unknown voltage level exceeds a given reference voltage.

The most desirable comparator parameter is what minimum differential input voltage is required at the comparator's input terminals to guarantee a given output logic state. This new and important parameter has been called input sensitivity (V_{IS}) and is analogous to the input threshold voltage specification on a core memory sense amplifier. The input sensitivity specification includes the effects of voltage gain, input offset voltage and input offset current and eliminates the need for specifying these three parameters.

In order to make this parameter as inclusive as possible on the MC3430 to MC3433 series quad comparators, the input sensitivity is specified within the following conditions:

Commercial temperature range: 0° to 70°C
Power supply variations: ±5% (all conditions)
Input source resistance: ≤ 200 Ω
Common mode voltage range: –3.0 V to +3.0 V

Note: Typical values have been included on the omitted parameters for applications where the offset voltages are externally nulled.

Voltage gain is defined as the ratio of the resulting ΔV_O to a change in the V_{IDR} using conditions at which the V_{IO} and I_{IO} are nulled. Thus, for worst case MTTL logic levels, the required output voltage change is 2.0 V [V_{OH}(min) – V_{OL}(max) = 2.4 V – 0.4 V]. If 2.0 mV are required at the input terminals to induce this change in logic state, the voltage gain would be 1000 V/V.

Gain, however, is not the only factor affecting the logic transition. Normally, input offset voltages that are not externally nulled can add an appreciable error that drastically overshadows the comparator gain. Therefore, the 2.0 mV required to cause the logic transition, for example, is often masked. An input offset voltage of up to 7.5 mV might be required to reach the analog region. A further consideration is the input offset current of up to ±10 μA flowing through the matched 200 Ω source resistors at the input terminals which can create an additional error of ±2.0 mV. In order to determine a worst case input sensitivity, it must be assumed that minimum specified gain and maximum specified offset voltage and current conditions exist. Also, it must be assumed that these three factors are cumulative, requiring a worst case input of:

Logic transition = 2.0 mV
V_{IO} = 7.5 mV
I_{IO} of ±10 μA thru 200 Ω resistor = 2.0 mV
Therefore, 2 + 7.5 + 2 = 11.5 mV.

The effects of power supply voltage variations, temperature changes and common mode input voltage conditions have not been considered, as they are not present in the gain and offset specifications on most comparators.

Thus, the input sensitivity specification greatly reduces the effort required in determining the worst case differential voltage required by a given comparator type.

Table 1 compares the worst case input sensitivity of three popular comparator types at both room temperature and over the specified commercial temperature range (0° to 70°C). This sensitivity was computed from the specified voltage gain, offset voltage and offset current limits.

Table 1. Worst Case Comparisons

Device	T_A = 25°C						T_A = 0° to 70°C					
	V_{IO} (mV) Max	A_{VOL}* V/V Typ	V_{ID} Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω (μA) Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity (mV)	V_{IO} (mV) Max	A_{VOL}* V/V Typ	V_{ID} Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω (μA) Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity (mV)
MC3430 MC3432	–	–	–	–	–	6.0	–	–	–	–	–	7.0
MC3431 MC3433	–	–	–	–	–	10	–	–	–	–	–	12
MC1711C	5.0	1500	2.0 mV	15	3.0 mV	10	5.0	1000	3.0 mV	25	5.0 mV	13
LM311	7.5	200 k	0.015 mV	6.0**	0.0012 mV	7.516	10	100 k	0.030 mV	70**	0.014 mV	10.04

* Typical values given, as minimum gain not always specified.

** I_{IO} measured in nA.

Figure 2. Guaranteed Output State versus Differential Input Voltage

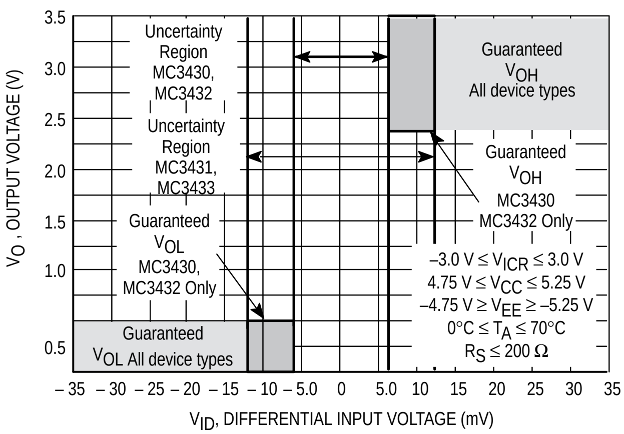
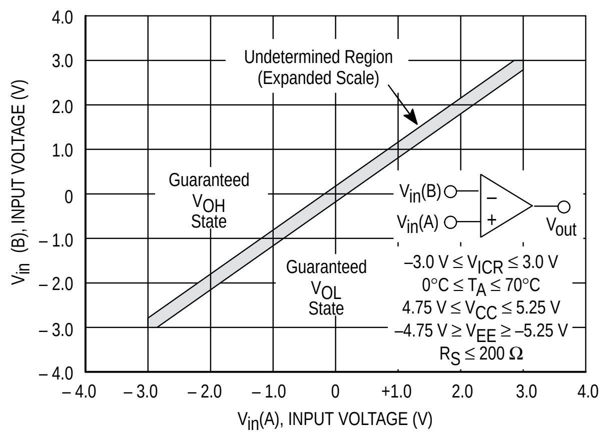


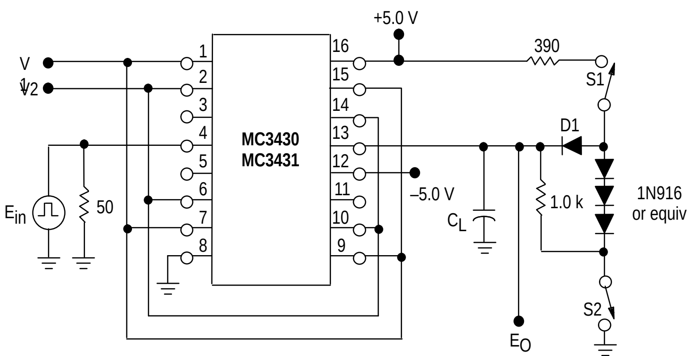
Figure 3. Guaranteed Output State versus Input Voltage



SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = –5.0 Vdc, T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3430, MC3431			MC3432, MC3433			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV $+V_{IS}$	$t_{PHL(D)}$	6,8–11	–	20	45	–	27	50	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV $+V_{IS}$	$t_{PLH(D)}$	6,8–11	–	33	55	–	40	65	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	4	–	–	35	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	4	–	–	35	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	4	–	–	40	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	4	–	–	35	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	5	–	–	–	–	–	40	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	5	–	–	–	–	–	35	ns

Figure 4. Strobe Propagation Delay Times $t_{PLZ(S)}$, $t_{PZL(S)}$, $t_{PHZ(S)}$, and $t_{PZH(S)}$



Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{in} waveform characteristics.
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

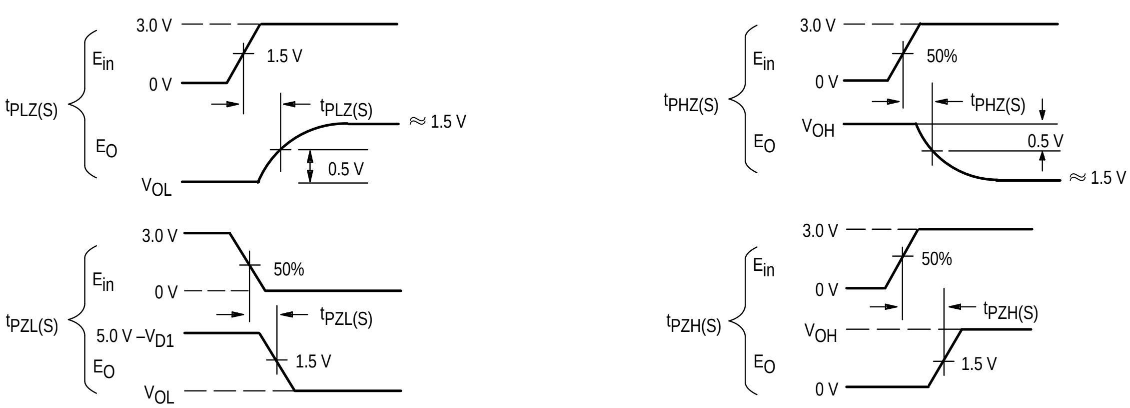
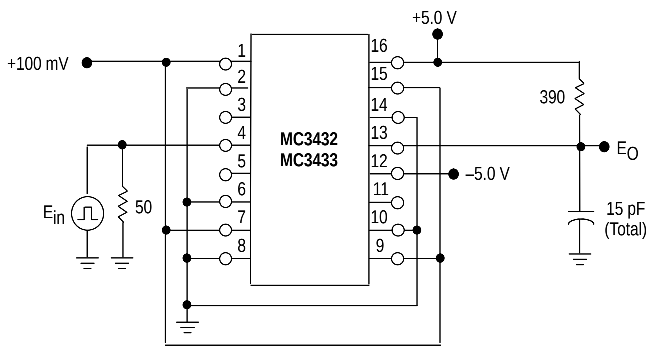
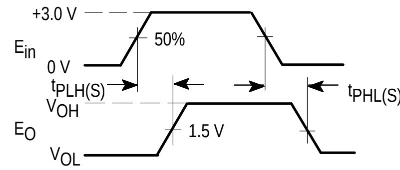


Figure 5. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

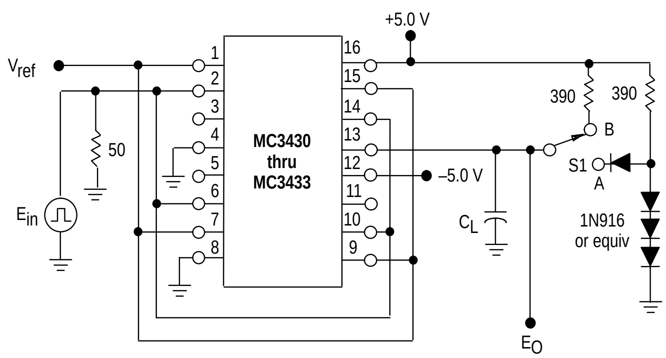


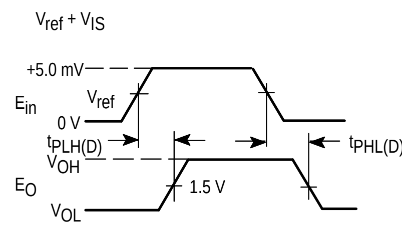


Output of Channel B shown under test, other channels are tested similarly.

E_{in} waveform characteristics.
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

Figure 6. Differential Input Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$





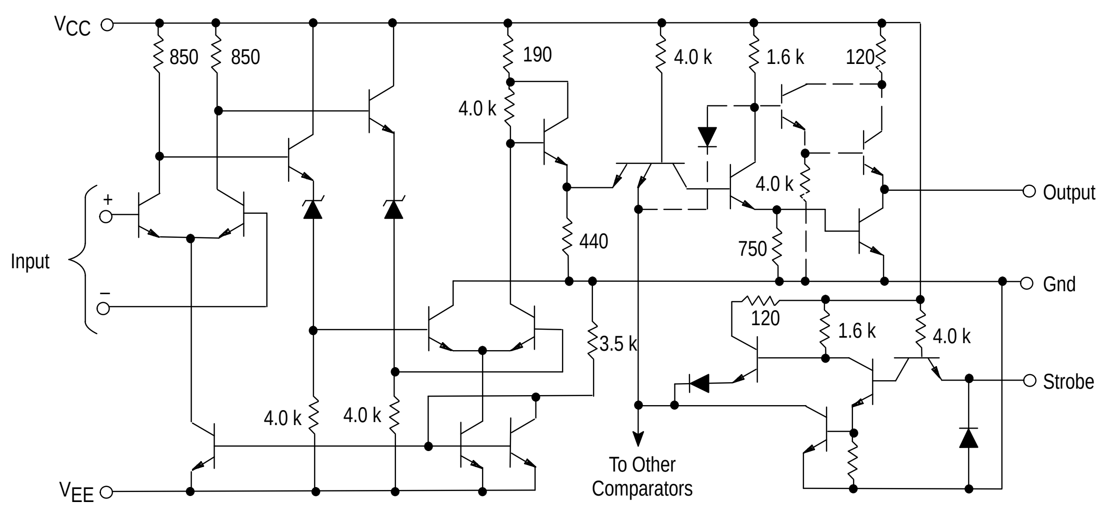
E_{in} waveform characteristics.
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

Output of Channel B shown under test, other channels are tested similarly.

S1 at “A” for MC3430, MC3431
S1 at “B” for MC3432, MC3433
C_L = 50 pF total for MC3430, MC3431
C_L = 15 pF total for MC3432, MC3433

Device	V_{ref}
MC3430	11 mV
MC3431	15 mV
MC3432	11 mV
MC3433	15 mV

Figure 7. Circuit Schematic
(1/4 Circuit Shown)



Dashed components apply to the MC3430 and MC3431 circuits only.

Response Time versus Overdrive – MC3430, MC3431

Figure 8. Output Low–to–High

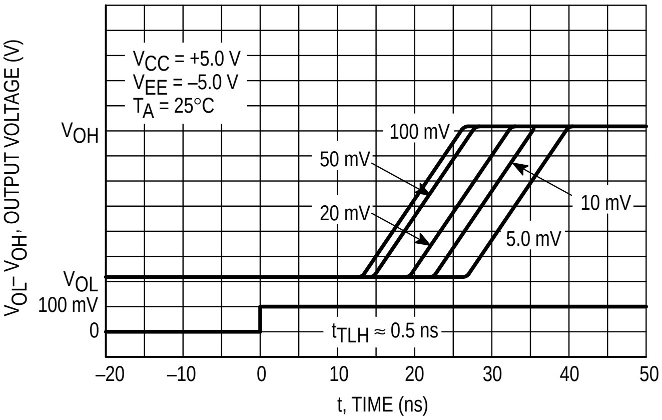
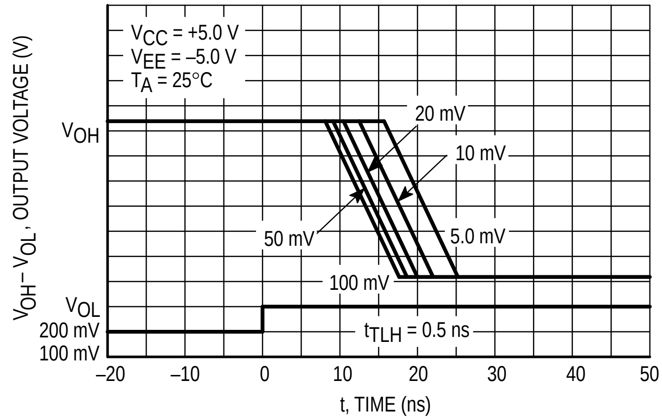


Figure 9. Output High–to–Low



Response Time versus Overdrive – MC3432, MC3433

Figure 10. Output Low–to–High

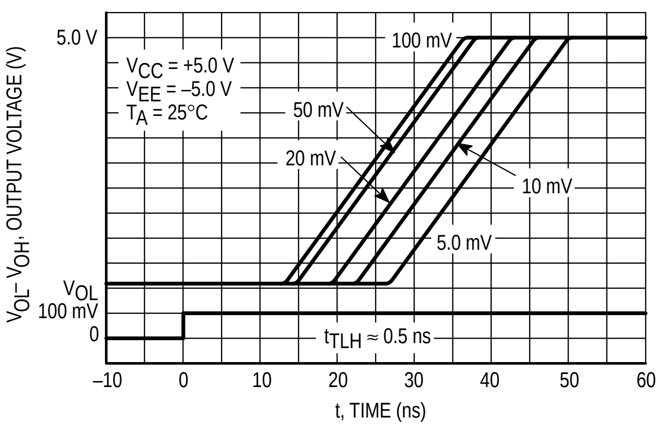


Figure 11. Output High–to–Low

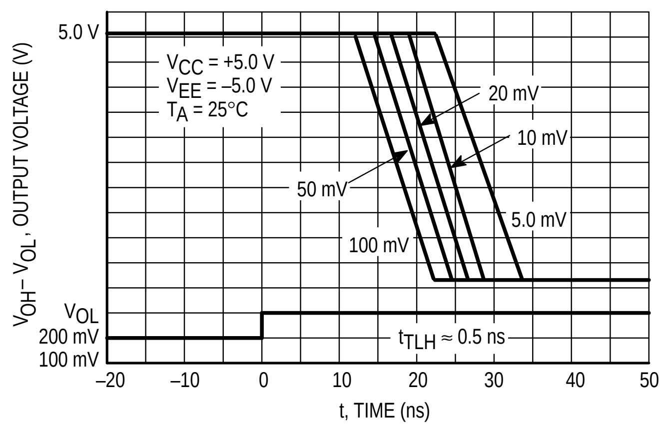


Figure 12. Average Input Offset Voltage versus Temperature

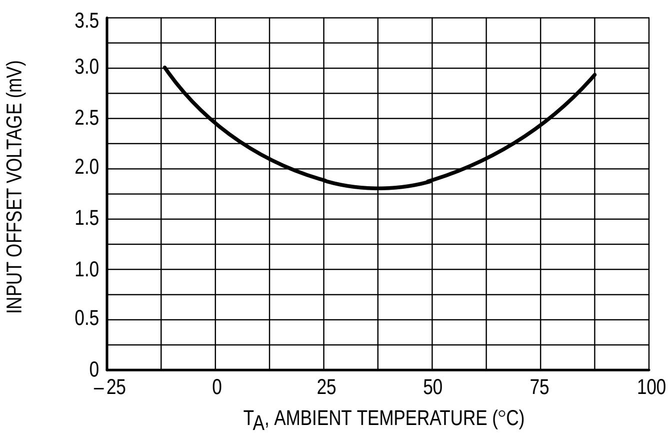


Figure 13. Response Time versus Temperature

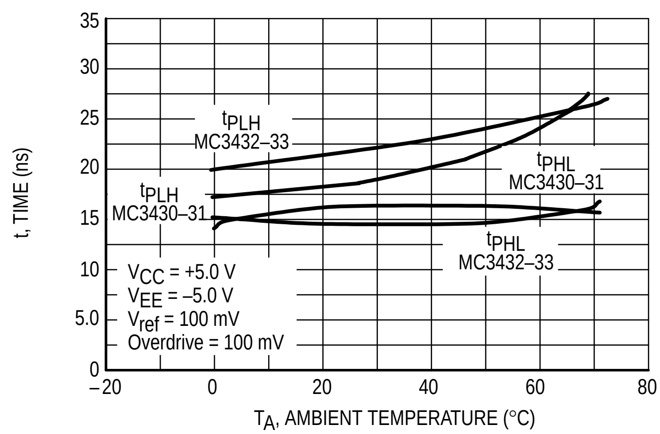
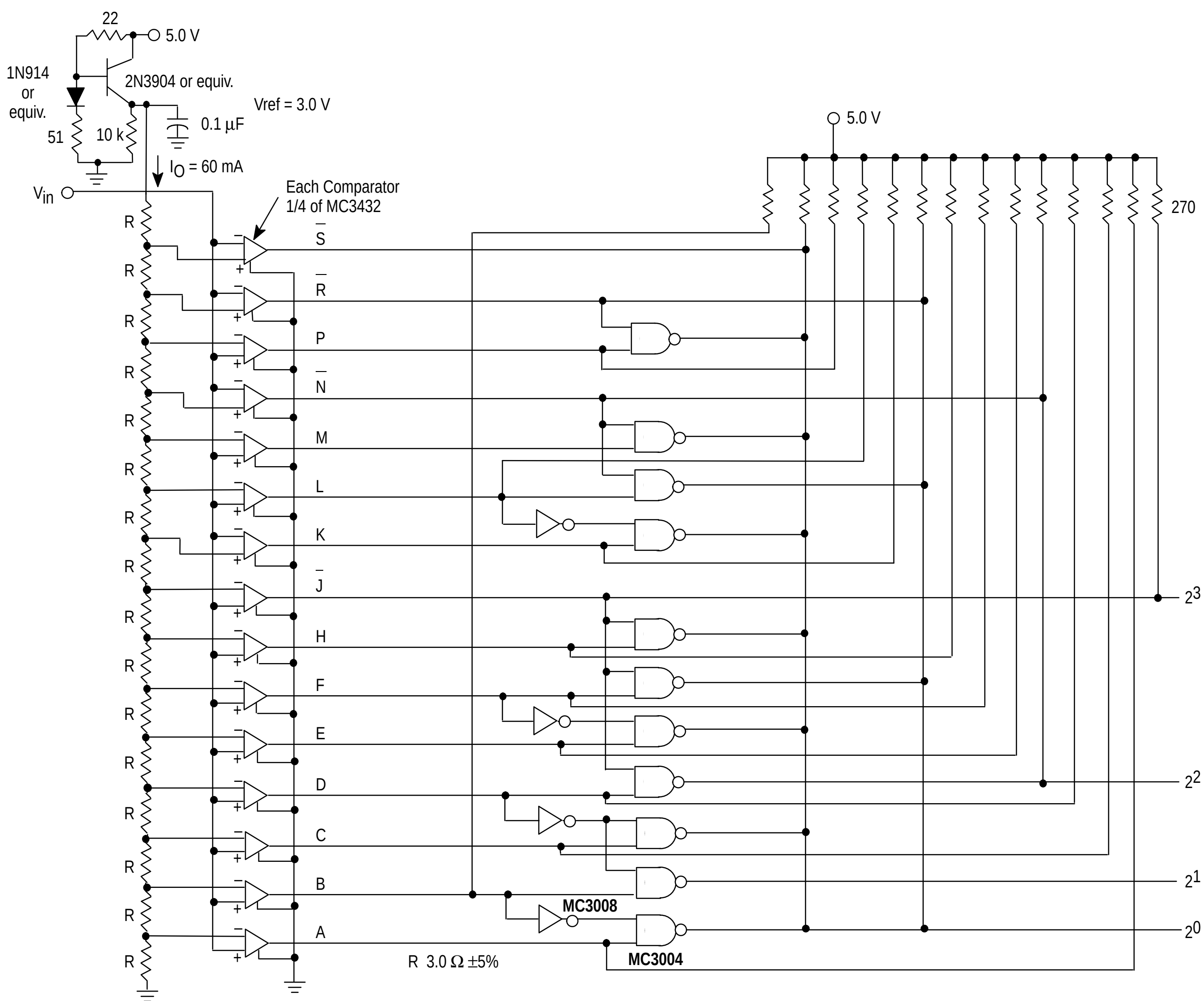


Figure 14. 4–Bit Parallel A/D Converter



$\overline{2^0} = (\overline{A} + B)\,(\overline{C} + D)\,(\overline{E} + F)\,(\overline{H} + J)\,(\overline{K} + L)\,(\overline{M} + N)\,(\overline{P} + R)\,(S)$

$\overline{2^1} = (\overline{B} + D)\,(\overline{F} + J)\,(\overline{L} + N)\,(\overline{R})$

$\overline{2^2} = (\overline{D} + J)\,(\overline{N})$

$\overline{2^3} = \overline{J}$

Conversion Time ≅ 50 ns

Figure 15. Level Detector with Hysteresis

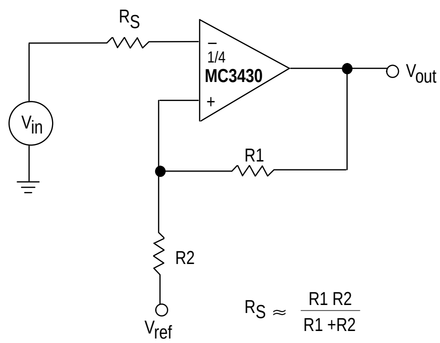
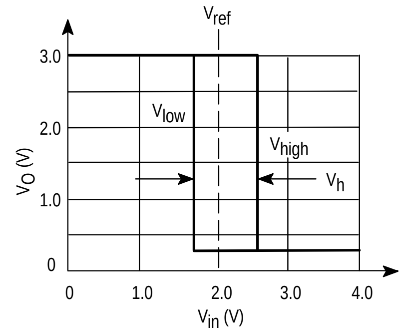


Figure 16. Transfer Characteristics and Equations for Figure 15



$$V_{high} = V_{ref} + \frac{R2\,[V_{O(max)} - V_{ref}]}{R1 + R2}$$

$$V_{low} = V_{ref} + \frac{R2\,[V_{O(min)} - V_{ref}]}{R1 + R2}$$

Hysteresis Loop (V_h):

$$V_h = V_{high} - V_{low} = \frac{R2}{R1 + R2}\,[V_{O(max)} - V_{O(min)}]$$

Figure 17. Double–Ended Limit Detector

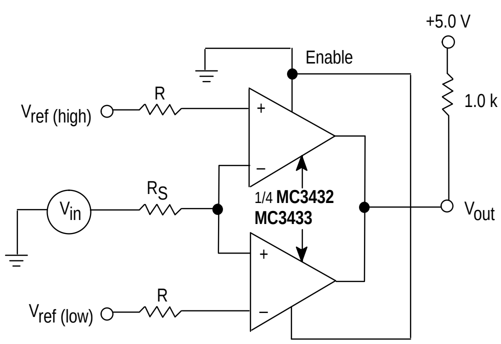
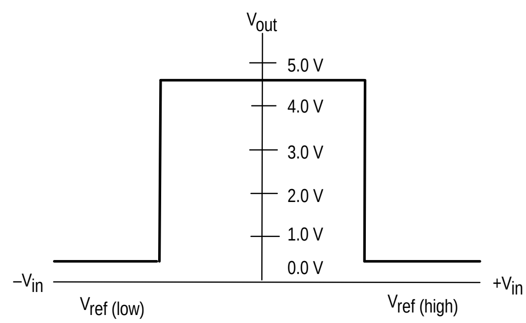
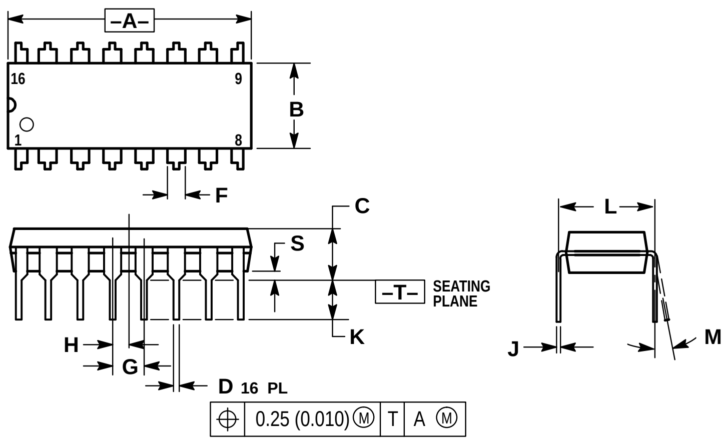


Figure 18. Voltage Transfer Function



OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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