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MOTOROLA

MC34270
MC34271

Advance Information

Liquid Crystal Display and Backlight Integrated Controller

LIQUID CRYSTAL DISPLAY AND BACKLIGHT INTEGRATED CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

The MC34270 and MC34271 are low power dual switching voltage regulators, specifically designed for handheld and laptop applications, to provide several regulated output voltages using a minimum of external parts. Two uncommitted switching regulators feature a very low standby bias current of 5.0 µA, and an operating current of 7.0 mA capable of supplying output currents in excess of 200 mA.

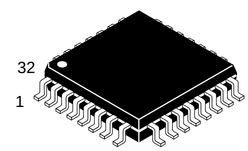
Both devices have three additional features. The first is an ELD Output that can be used to drive a backlight or a liquid crystal display. The ELD output frequency is the clock divided by 256. The second feature allows four additional output bias voltages, in specific proportions to V_B, one of the switching regulated output voltages. It allows use of mixed logic circuitry and provides a voltage bias for N–Channel load control MOSFETs™. The third feature is an Enable input that allows a logic level signal to turn–“off” or turn–“on” both switching regulators.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC34270 and MC34271 Features:

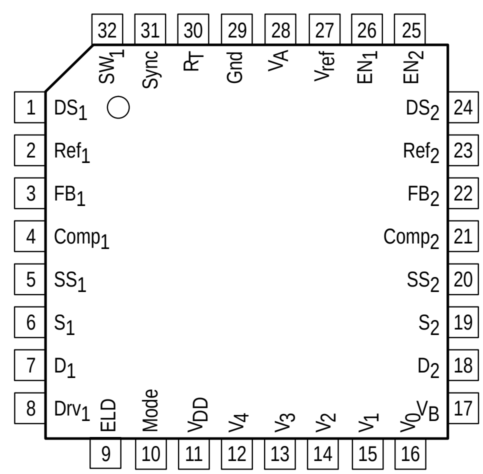
- Low Standby Bias Current of 5.0 µA
- Uncommitted Switching Regulators Allow Both Positive and Negative Supply Voltages
- Logic Enable Allows Microprocessor Control of All Outputs
- Synchronizable to External Clock
- Mode Commandable for ELD and LCD Interface
- Frequency Synchronizable
- Auxiliary Output Bias Voltages Enable Load Control via N–Channel FETs

MOSFET is a trademark of Motorola, Inc.



FB SUFFIX
PLASTIC PACKAGE
CASE 873

PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

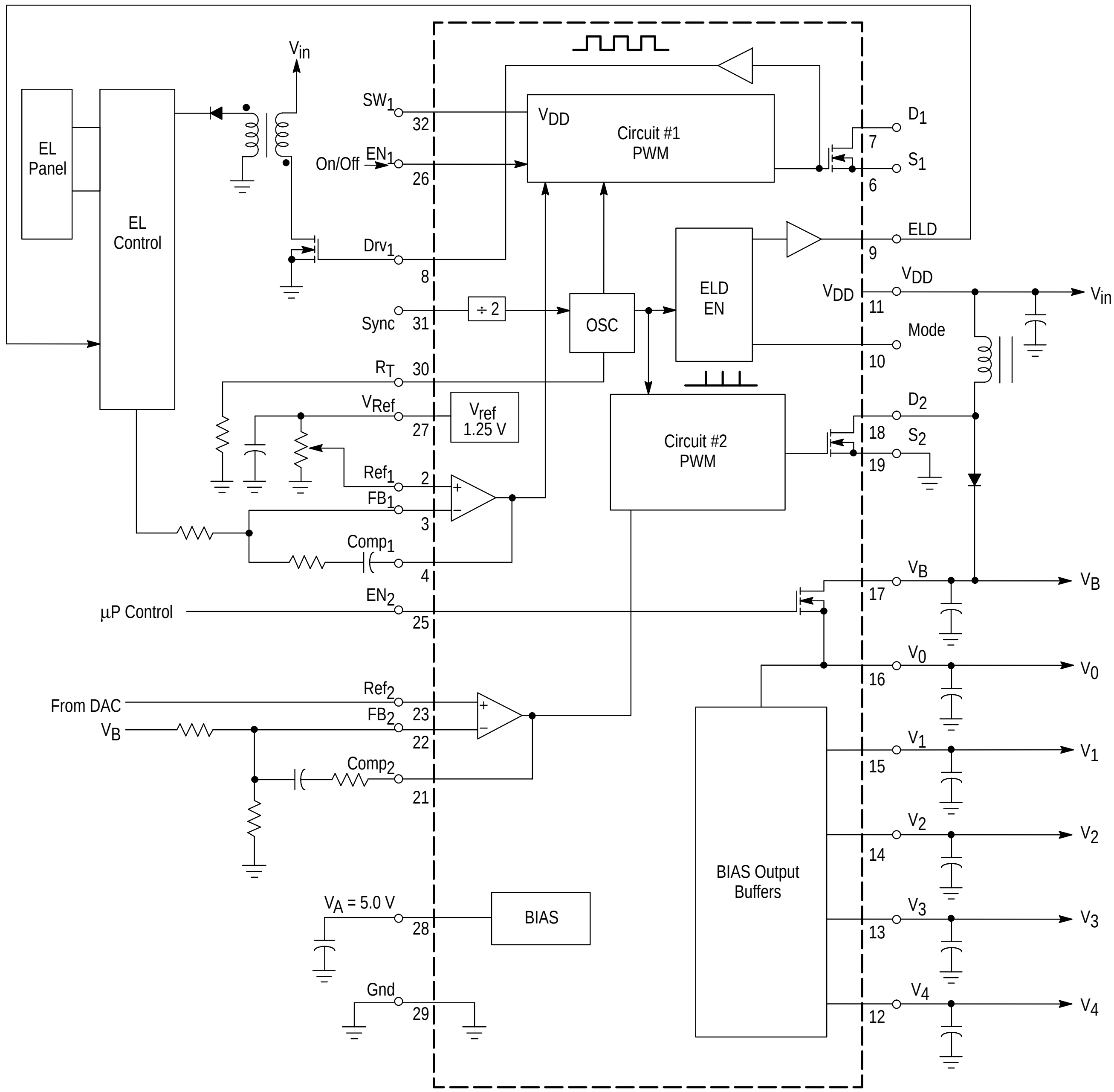
Rating	Symbol	Value	Unit
Input Voltage	V_{DD}	16	Vdc
Power Dissipation and Thermal Characteristics Maximum Power Dissipation Case 873 Thermal Resistance Junction–to–Ambient Thermal Resistance Junction–to–Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$	 1.43 100 60	 W °C/W °C/W
Output #1 and #2 Switch Current	I_{SL} & I_{SB}	500	mA
Output #1 and #2 “Off”–State Voltage	V_{SL}	60	Vdc
Feedback Enable MOSFETs “Off”–State Voltage	V_{LF}	20	Vdc
Operating Junction Temperature	T_J	125	°C
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC34270FB	T_A = 0° to +70°C	QFP–32
MC34271FB		QFP–32

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Representative Block Diagram



This device contains 350 active transistors.

ELECTRICAL CHARACTERISTICS (V_{DD} = 6.0 V, for typical values T_A = Low to High [Note 1], for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (T_J = 25°C)	V_{ref}	1.225	1.250	1.275	V
Line Regulation (V_{DD} = 5.0 V to 12.5 V)	Reg_{line}	–	2.0	10	mV
Load Regulation (I_O = 0 to 120 μA)	Reg_{load}	–	2.0	10	mV
Total Variation (Line, Load and Temperature)	V_{ref}	1.215	–	1.285	V
ERROR AMPLIFIERS					
Input Offset Voltage (V_{CM} = 1.25 V)	V_{IO}	–	1.0	10	mV
Input Bias Current (V_{CM} = 1.25 V)	I_{IB}	–	120	600	nA
Open–Loop Voltage Gain (V_{CM} = 1.25 V, V_{COMP} = 2.0 V)	A_{VOL}	80	100	–	dB
Output Voltage Swing High State (I_{OH} = –100 μA) Low State (I_{OL} = 100 μA)	 Ve_{OH} Ve_{OL}	 V_A–1.5 0	 4.0 –	 5.5 1.0	V
BIAS VOLTAGE					
Voltage (V_{DD} = 5.0 V to 12.5 V, I_O = 0)	V_A	4.6	5.0	5.4	V
OSCILLATOR AND PWM SECTIONS					
Total Frequency Variation Over Line and Temperature V_{DD} = 5.0 V to 10 V, T_A = 0° to 70°C, R_T = 169 k	f_{OSC}	 90	 115	 140	kHz
Duty Cycle at Each Output Maximum Minimum	 DC_{max} DC_{min}	 92 –	 95 –	 – 0	%
Sync Input Input Resistance (V_{sync} = 3.5 V) Minimum Sync Pulse Width	 R_{sync} T_p	 25 –	 50 1.0	 100 –	 kΩ μs
OUTPUT MOSFETs					
Output Voltage – “On”–State (I_{sink} = 200 mA)	V_{OL}	–	150	250	mV
Output Current – “Off”–State (V_{OH} = 40 V)	I_{OH}	–	0.1	1.0	μA
Rise and Fall Times	t_r, t_f	–	50	–	ns
EL DISCHARGE OUTPUT (ELD) AND DRV_1					
Output Voltage – “On”–State (I_{sink} = 100 μA)	V_{OL}	–	30	100	mV
Output Voltage – “On”–State (I_{sink} = 50 mA)	V_{OL}	–	2.0	2.5	V
Output Voltage – “Off”–State (I_{source} = –100 μA)	V_{OH}	V_{DD}–0.5	5.9	–	V
Output Voltage – “Off”–State (I_{source} = –50 mA)	V_{OH}	V_{DD}–3.5	3.3	–	V
FEEDBACK ENABLE SWITCHES (DS_1, DS_2)					
Output Voltage – “Low”–State (I_{sink} = 1.0 mA)	Vfe_{OL}	–	10	100	mV
Output Current – “Off”–State (V_{OH} = 12.5 V)	Ife_{OH}	–	0.6	1.0	μA
SWITCHED V_{DD} OUTPUT (SW_1)					
Output Voltage Switch “On” (EN_1 = 1, I_{source} = 100 μA) Switch “Off” (EN_1 = 0, I_{sink} = 100 μA)	 Vsw_{OH} Vsw_{OL}	 5.5 0	 5.9 0.1	 6.0 0.2	V
AUXILIARY VOLTAGE OUTPUTS					
V_0 Enable Switch “On”–Resistance: V_B to V_0 “Off”–State Leakage Current (V_B = 10 V) V_0 Voltage (V_B = 30 V, I_{source} = 0 mA) V_0 Resistance (I_{source} = 4.0 mA)	 Rds I_{lkg} V_0 R_0	 0 0 29.5 20	 2.0 0.1 29.9 40	 10 2.0 30 60	 Ω μA V Ω

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 6.0 V, for typical values T_A = Low to High [Note 1], for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
AUXILIARY VOLTAGE OUTPUTS					
V_1, V_2, V_3, V_4 Outputs					
$1–V_1/V_0$ Ratio: MC34270		0.0565	0.0580	0.0595	
MC34271		0.0500	0.0520	0.0535	
$1–V_2/V_0$ Ratio: MC34270		0.1135	0.1160	0.1185	
MC34271		0.1010	0.1035	0.1065	
V_3/V_0 Ratio: MC34270		0.1135	0.1160	0.1185	
MC34271		0.1010	0.1035	0.1065	
V_4/V_0 Ratio: MC34270		0.0565	0.0580	0.0595	
MC34271		0.0500	0.0520	0.0535	
Output Resistance (I_{source} = 4.0 mA)	R_o	20	40	60	Ω
Output Short Circuit Current	I_{SS}	5.0	10	20	mA
LOGIC INPUTS (EN_1, EN_2, MODE)					
Input Low State	V_{IL}	0	–	0.8	V
Input High State	V_{IH}	2.0	–	6.0	V
Input Impedance	R_{in}	25	50	100	kΩ
SOFT START CONTROL (SS_1,SS_2)					
Charge Current (Capacitor Voltage = 1.0 V to 4.0 V)	I_{chg}	0.5	1.0	2.5	µA
Discharge Current (Capacitor Voltage = 1.0 V)	I_{dschg}	250	650	–	µA
TOTAL SUPPLY CURRENT					
V_{DD} Current Standby Mode (EN_1 = EN_2 = 0) V_{DD} = 6.0 V	I_{CC}	–	2.0	5.0	µA
V_{DD} = 16 V		–	3.0	15	
V_{DD} Current Backlight "On" (EN_1 = 1; EN_2 = 0)	I_{CC}	–	0.7	3.0	mA
V_{DD} Current LCD "On" (No Inductor) (EN_1 = 0; EN_2 = 1)	I_{CC}	–	0.9	2.0	mA
V_B Current (V_0 = 35 V)	I_O	–	1.2	3.0	mA

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Switch Output Duty Cycle versus Compensation Voltage

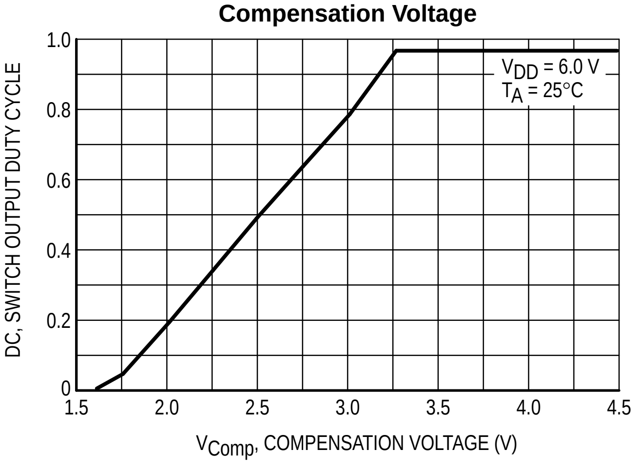


Figure 2. Error Amp Open–Loop Gain and Phase versus Frequency

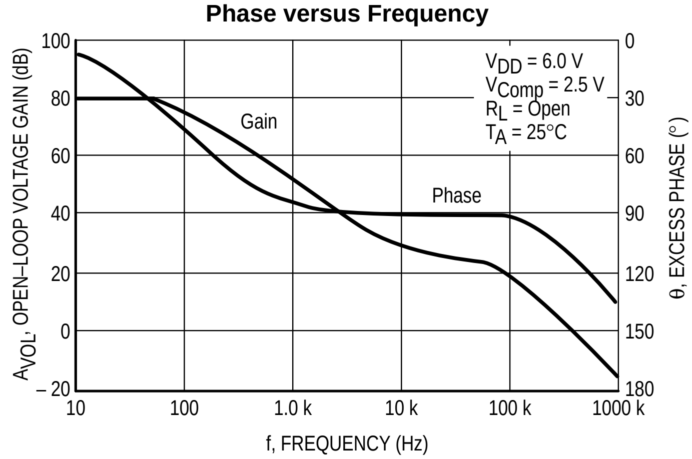


Figure 3. Reference Voltage Change versus Reference Current

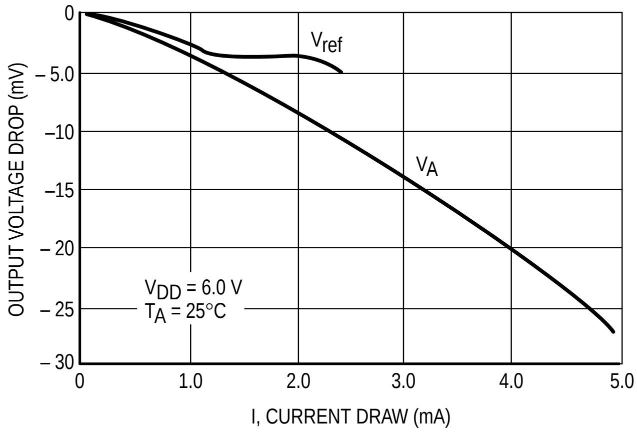


Figure 4. Quiescent Current versus Supply Voltage

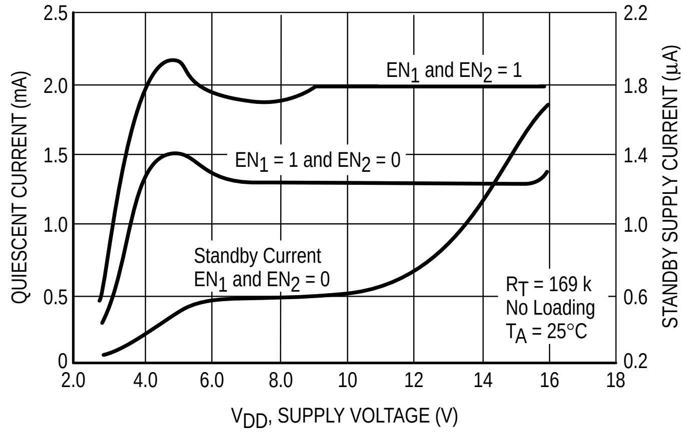


Figure 5. FET Drain Voltage versus Sink Current

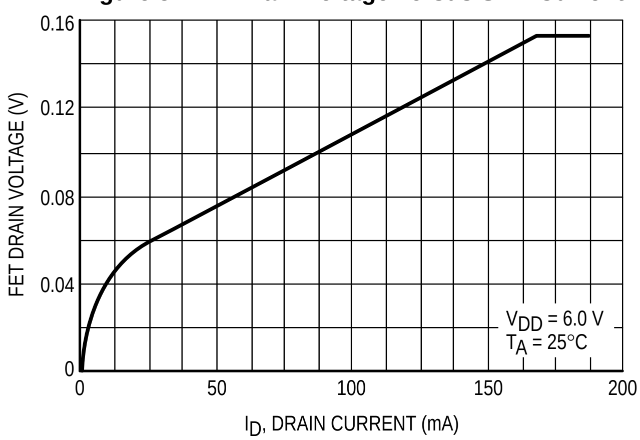


Figure 6. ELD and DRV1 Switch Output Source and Sink Saturation versus Current

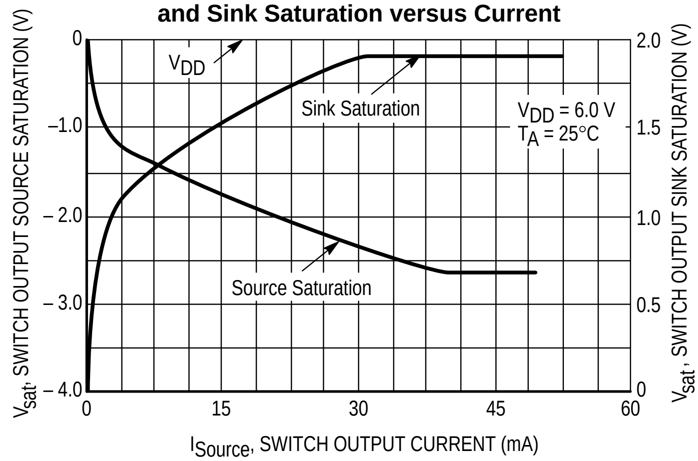


Figure 7. V_{ref} and V_A Variation versus Temperature

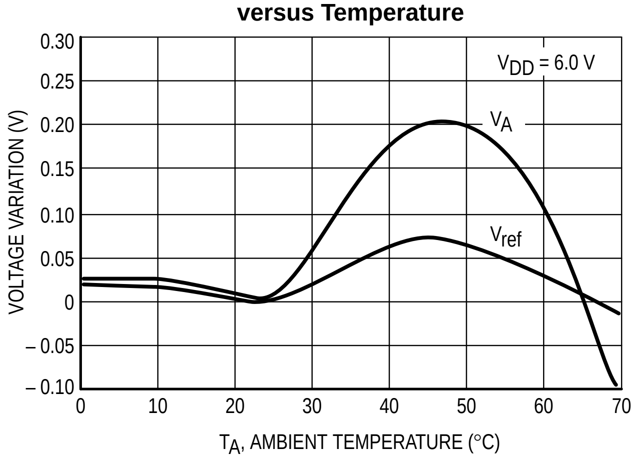


Figure 8. Oscillator Frequency Variation versus Temperature

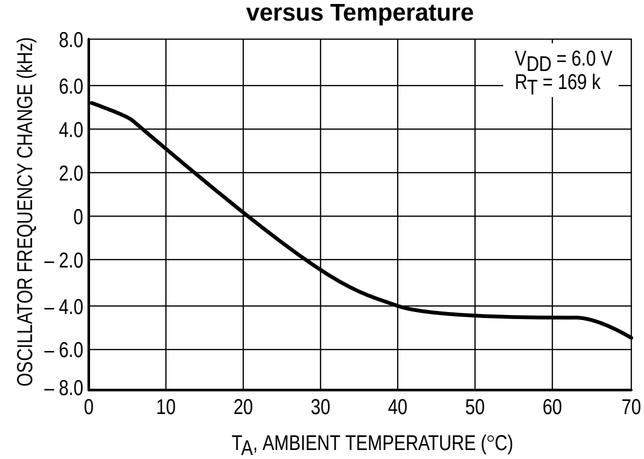


Figure 9. Frequency versus Timing

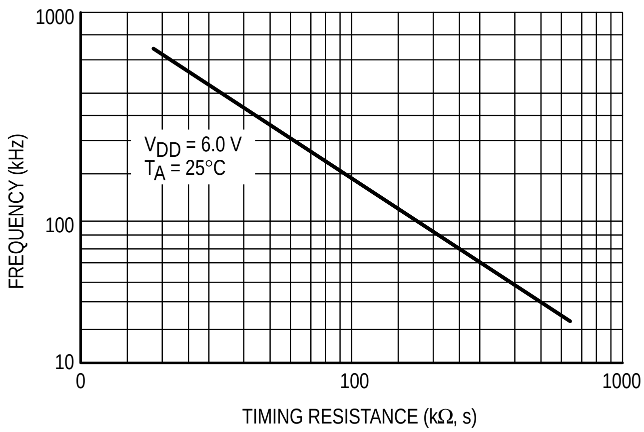
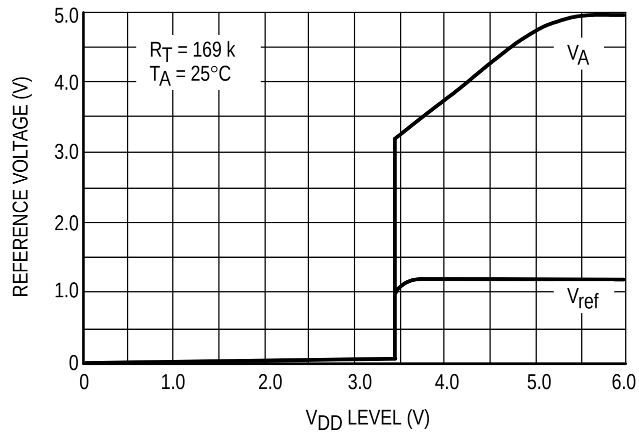


Figure 10. V_A, V_{ref} versus V_{DD}



OPERATING DESCRIPTION

The MC34270 and MC34271 series are monolithic, fixed frequency power switching regulators specifically designed for DC to DC converter and battery powered applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step–up, step–down and voltage inverting converters with a minimum number of external components. Potential markets include battery powered, handheld, automotive, computer, industrial and cost sensitive consumer products. A description of each section is given below with the representative block diagram shown in Figure 9.

Oscillator

The oscillator frequency is programmed by resistor R_T. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the switch outputs. During the fall time of the internal sawtooth waveform, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gates high, disabling the output switching MOSFETs. The internal sawtooth waveform has a nominal peak voltage of 3.3 V and a valley voltage of 1.7 V.

Pulse Width Modulators

Both pulse width modulators consist of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied to the inverting input. A third input to the comparator has a 0.5 mA typical current source that can be used to implement soft start. Output switch conduction is initiated when the ramp waveform is discharged to the valley voltage. As the ramp voltage increases to a voltage that exceeds the error amplifer output, the latch resets, terminating output MOSFET conduction for the duration of the oscillator ramp. This PWM/latch combination prevents multiple output pulses during a given oscillator cycle.

Each PWM circuit is enabled by a logic input. When disabled, the entire block is turned off, drawing only leakage current from the power source. Shared circuits, like the reference and oscillator, can be activated by either EN_1 or EN_2.

Circuit #1 has an ELD output which may be used to drive an LCD or backlight. Its output frequency is the oscillator frequency divided by 1024.

Error Amplifiers and Reference

Each error amplifier is provided with access to both inverting and noninverting inputs, and the output. The Error Amplifiers' Common Mode Input Range is 0 to 2.5 V. The amplifiers have a minimum DC voltage gain of 60 dB. The 1.25 V reference has an accuracy of ±4.0% at room temperature.

External loop compensation is required for converter stability. A simple low–pass filter is formed by connecting a resistive divider from the output to the error amplifier inverting input, and a series resistor–capacitor from the error amplifier output also to the to the inverting input. The step down converter is easiest to compensate for stability. The step–up and voltage inverting configurations, when operated as continuous conduction boost or flyback converters, are more difficult to compensate, and may require a lower loop design bandwidth.

MOSFET Switch Outputs

The output MOSFETs are designed to switch a maximum of 60 V, with a peak drain current capability of 500 mA. In circuit #1 an additional DRV_1 output is provided for interfacing with an external MOSFET.The gates of the MOSFETs are held low when the circuit is disabled.

Auxiliary Output Voltages

Output voltages V_0 through V_4 are provided for use as references or bias voltages. V_0 is the circuit #2 output voltage, when an internal FET switch is activated. The other auxiliary output voltages are proportional to V_B. The amplifiers for V_1 and V_2 are powered from V_0, while the amplifiers for V_3 and V_4 are powered from V_{DD}.

Figure 11. Representative Block Diagram Electroluminescent Backlight Configuration

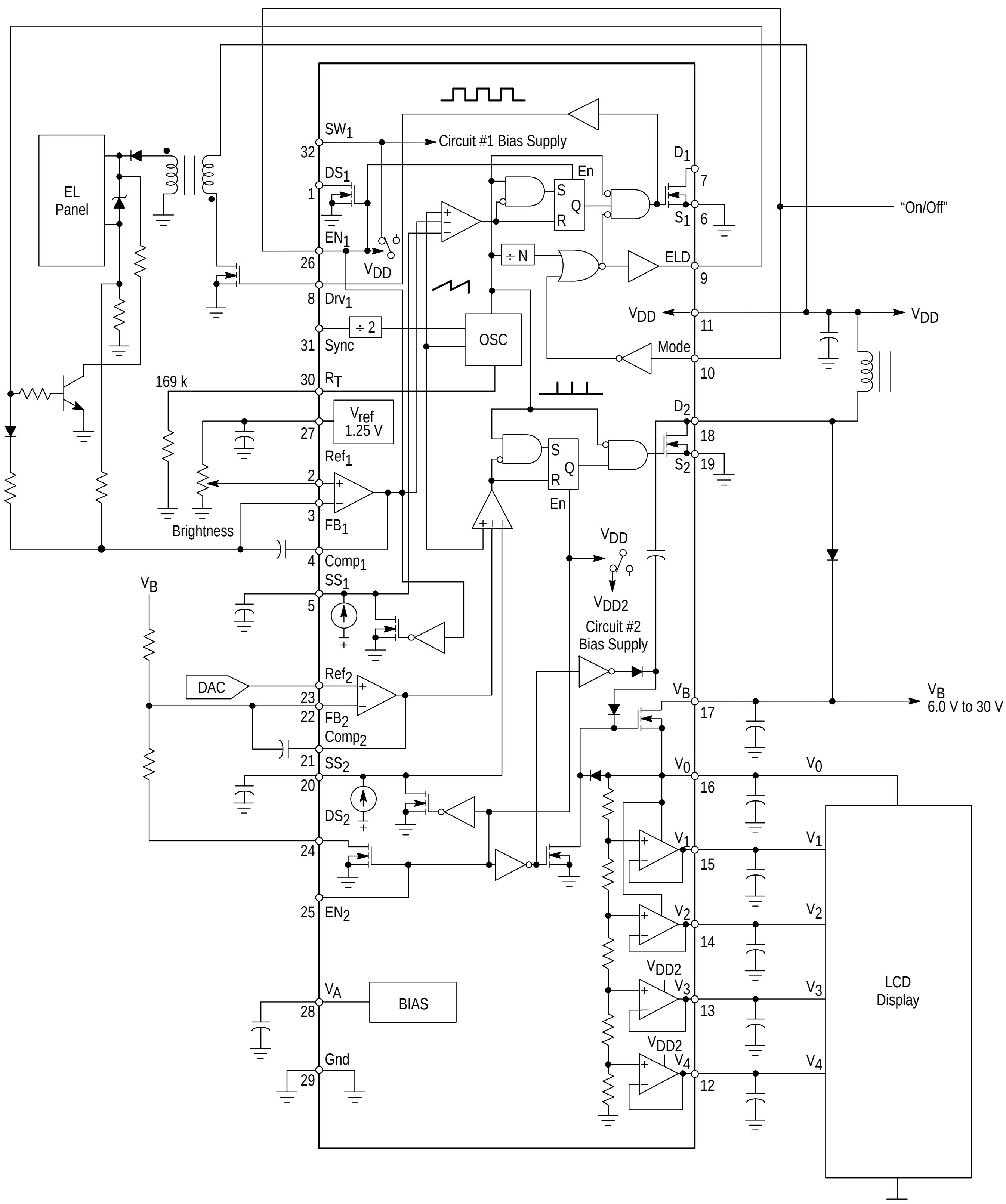


Figure 12. Auxiliary Supply Configuration

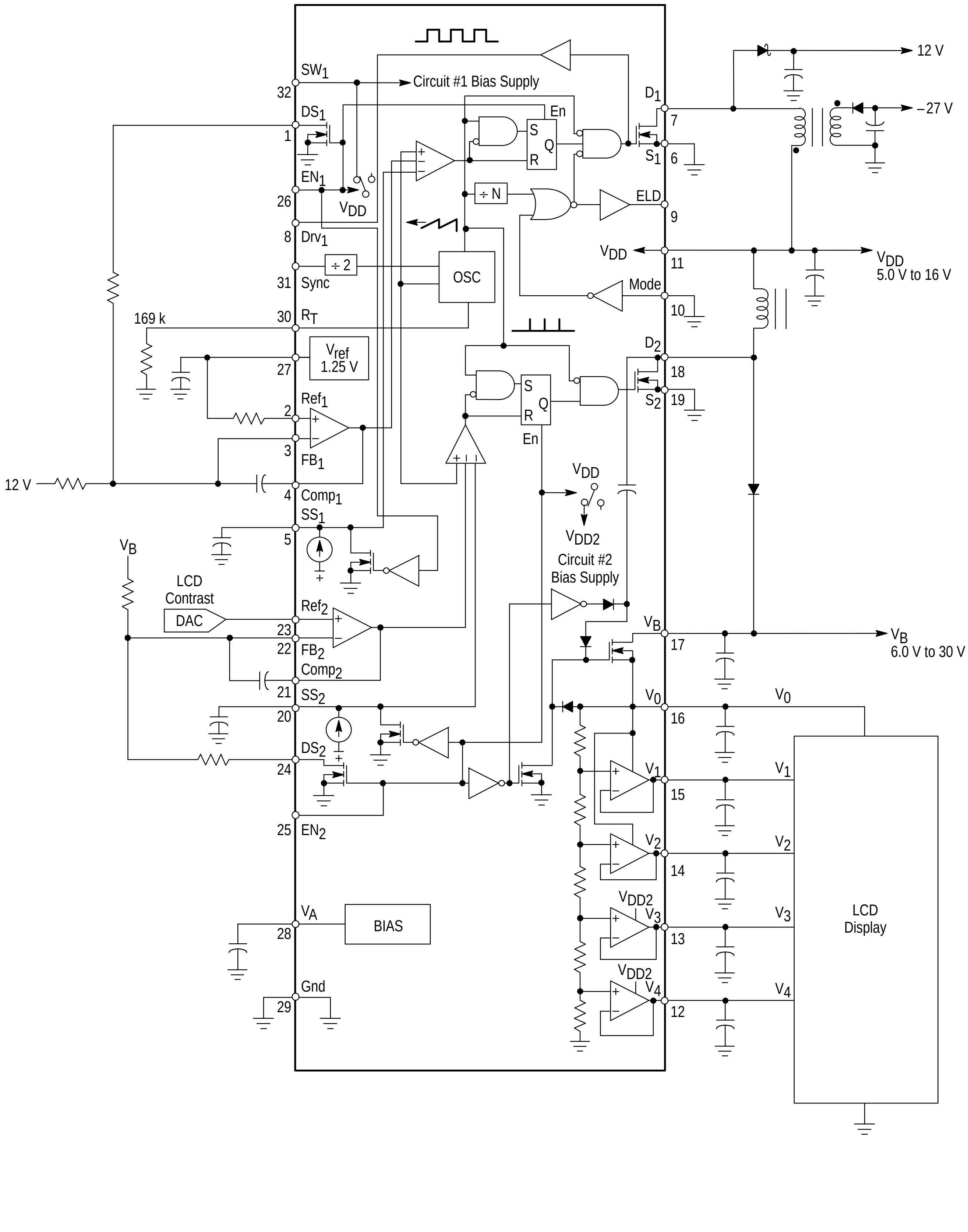


Figure 13. MC34270 Incandescent Backlight Configuration

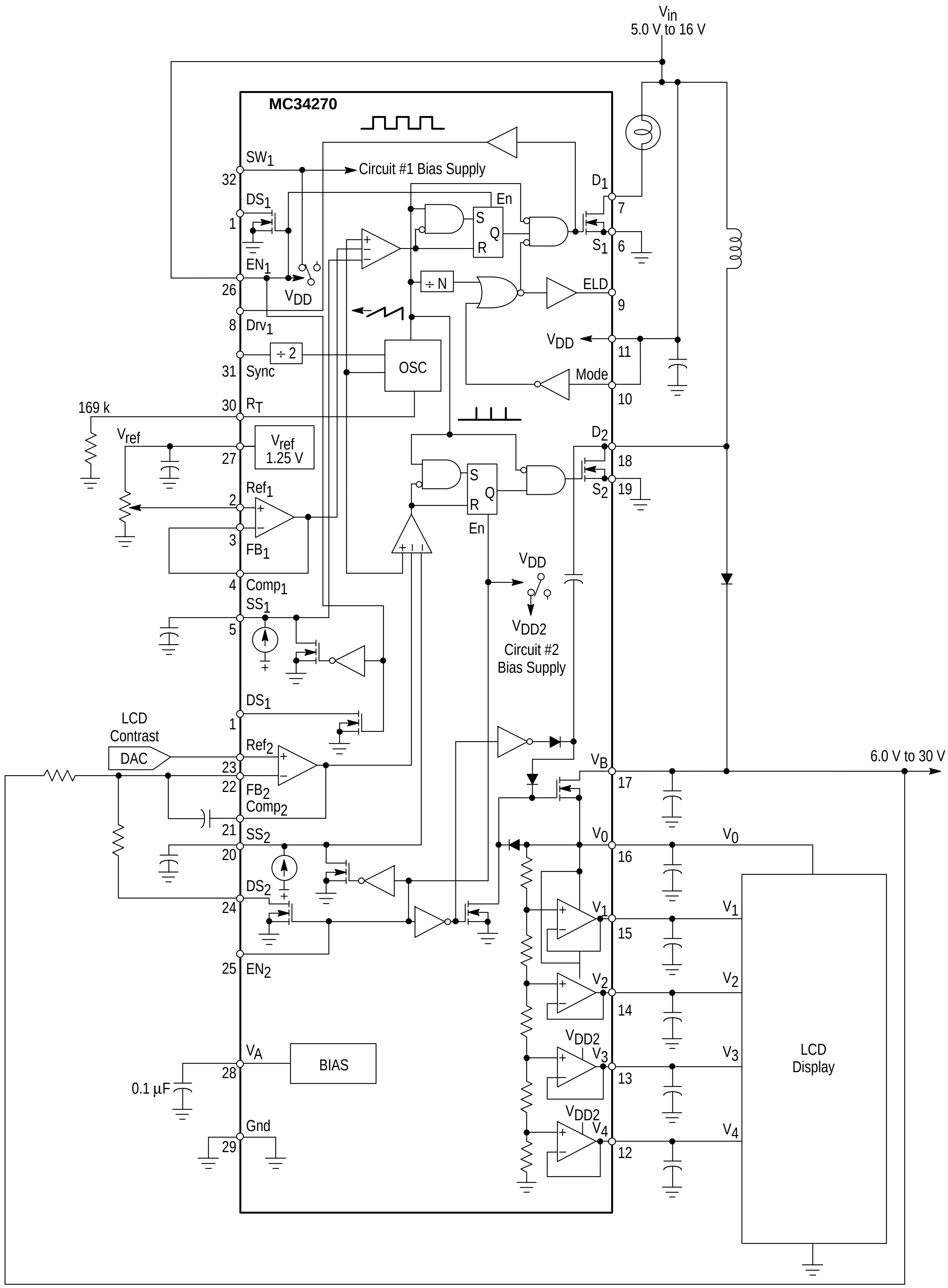
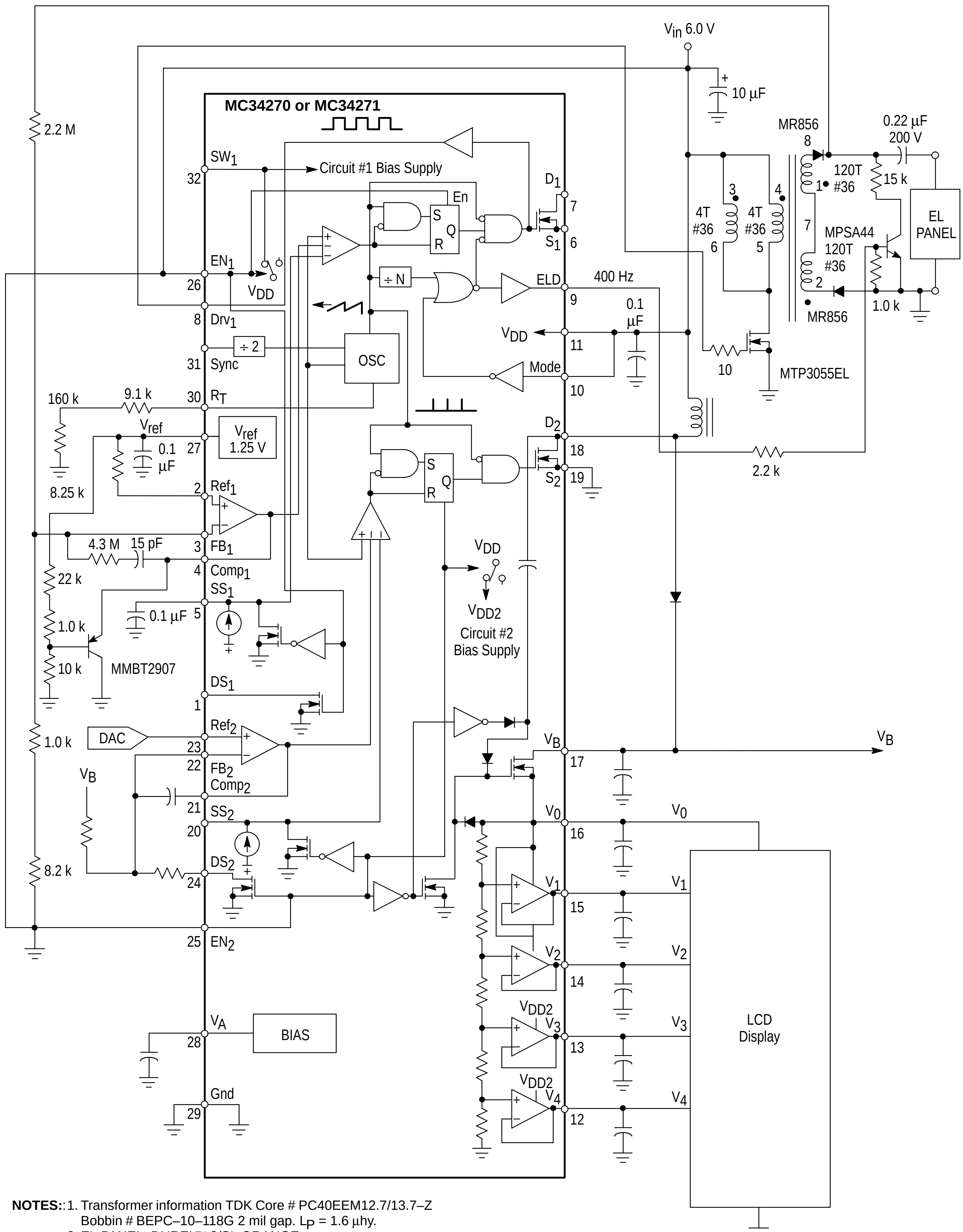


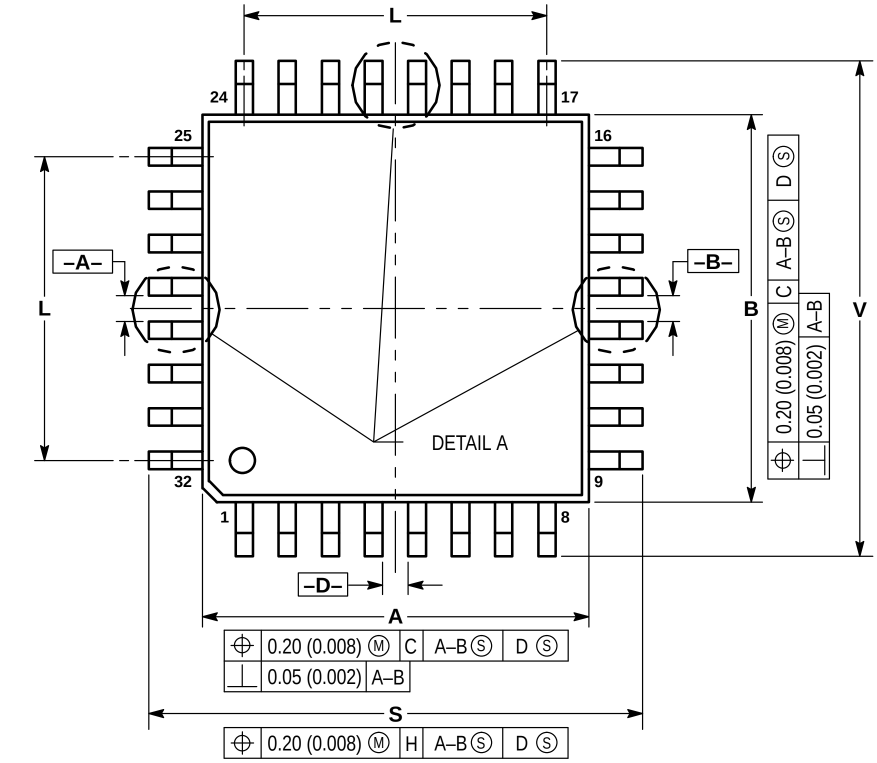
Figure 14. EL PANEL Drive Circuit

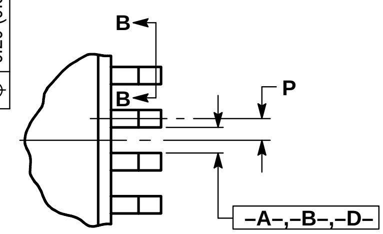


NOTES: 1. Transformer information TDK Core # PC40EEM12.7/13.7–Z
Bobbin # BEPC–10–118G 2 mil gap. L_P = 1.6 µhy.
2. EL PANEL: DUREL™ 3/SL ORANGE

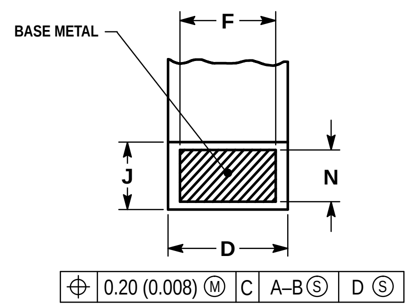
OUTLINE DIMENSIONS

FB SUFFIX
PLASTIC PACKAGE
CASE 873–01

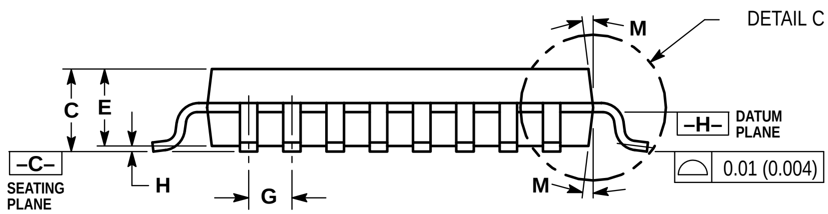


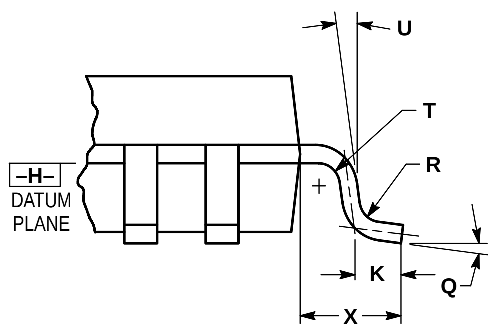


DETAIL A



SECTION B–B
VIEW ROTATED 90° CLOCKWISE





DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	–	0.010	–
G	0.80 BSC		0.031 BSC	
H	–	0.20	–	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

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