



MC34250

Product Preview

5.0 V, 200 M-Bit/Sec PR-IV Hard Disk Drive Read Channel

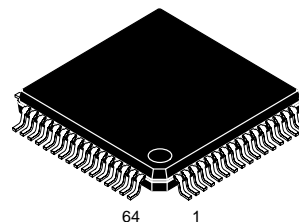
The Motorola MC34250 is a fully integrated partial response maximum likelihood disk drive read/write channel for use in zoned recording applications. This device integrates the AGC, active filter, 7 tap equalizer, Viterbi detector, frequency synthesizer, servo demodulator, 8/9 rate (0,4/4) Encoder/Decoder with write precompensation and power management in a single 64 pin 10 mm x 10 mm TQFP package.

FEATURES:

- 50 to 200 MBPS Programmable Data Rate
- 800 mW at 200 MBPS and 5.0 V
- Channel Monitor Output
- Programmable AGC Charge Pump Currents with Different Values for Data and Servo Envelope Modes and Gain Gradient Mode
- Programmable AGC Peak Detector Droop Currents with Different Values for Data and Servo Envelope Modes
- Separate AGC Charge Pump Outputs for Data and Servo Modes
- Programmable Dual Threshold Qualifier or Hysteresis Comparator Type Pulse Detector for Servo Data Detection.
- ERD and Polarity Outputs for Servo Timing and Raw Encoded Data
- Integrated 7 pole 0.05° Equiripple Linear Phase Filter with Programmable Bandwidth from 5.0 MHz to 80 MHz and Different Values for Both Data and Servo Modes
- Programmable Symmetrical Boost from 0 to 10 dB and Different Values for Data and Servo Modes
- Programmable Asymmetrical Boost of Up to $\pm 40\%$ of Nominal Filter Group Delay in Both Data and Servo Modes
- 7 Tap Continuous Time Transversal Equalizer with 8 Bit Programmable Tap Weights and Integrated Decision Directed Sign-Sign Least Mean Squared Adaptation
- Internal Offset Cancellation Loops
- Fast Acquisition Data Phase Locked Loop with Zero Phase Restart
- Programmable Data Phase Locked Loop Charge Pump Current
- Integrated Soft Decision Viterbi Detectors with Programmable Merge References
- Integrated 8/9 Rate (0,4/4) Encoder and Decoder with Code Scrambler and Descrambler
- Programmable 2/4/8 Bit NRZ Data Interface
- Programmable Write Precompensation Delays Locked to the Frequency Synthesizer
- Differential PECL Write Data Outputs
- External Write Data Path for DC Erase or Other Non-Encoded Data
- Integrated Write Current DAC
- Programmable Power Management
- Bi-Directional Serial Microprocessor Interface
- Various Test Modes Controlled Via the Serial Microprocessor Interface

HARD DISK DRIVE READ CHANNEL

SEMICONDUCTOR TECHNICAL DATA

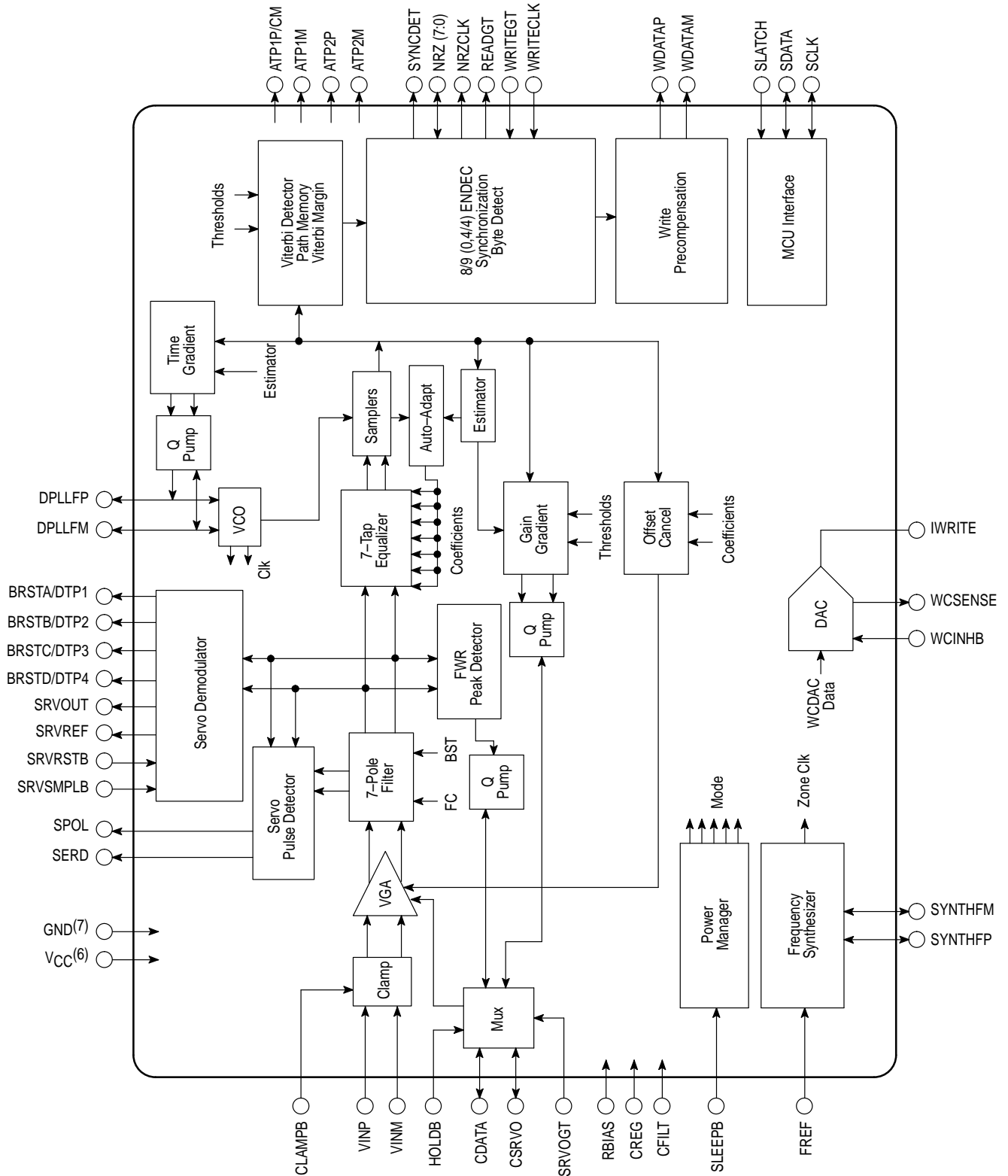


FTA SUFFIX
PLASTIC PACKAGE
CASE 840F-01
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34250FTA	$T_A = 0^\circ \text{ to } +70^\circ \text{C}$	TQFP-64


Simplified Block Diagram



This device contains 80,000 active transistors.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.950	10.050	0.392	0.396
B	9.950	10.050	0.392	0.396
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.550	0.018	0.022
L	7.500 BSC		0.295 BSC	
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.100	0.200	0.004	0.008
S	11.900	12.100	0.469	0.476
V	11.900	12.100	0.469	0.476
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	
Y	12° REF		12° REF	

MC34250

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MC34250/D

