MOTOROLA

MC34165
MC33165

Power Switching Regulators

The MC34165 series are monolithic power switching regulators that contain the primary functions required for DC–to–DC converters. This series is specifically designed to be incorporated in step–up, step–down, and voltage–inverting applications with a minimum number of external components.

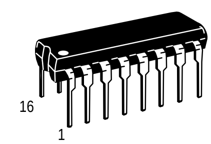
These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle–by–cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.

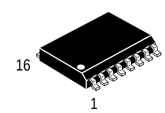
- Output Switch Current in Excess of 1.5 A
- Operation from 3.0 V to 65 V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle–by–Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package

POWER SWITCHING REGULATORS

SEMICONDUCTOR TECHNICAL DATA

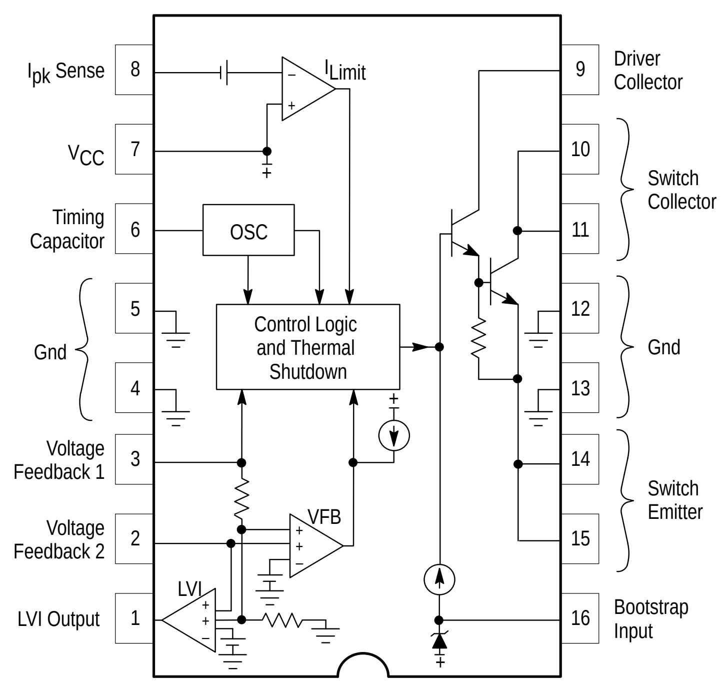


P SUFFIX
PLASTIC PACKAGE
CASE 648C
(DIP–16)



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

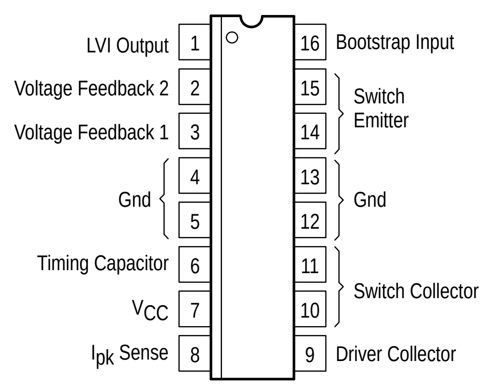
Representative Block Diagram



(Bottom View)

This device contains 114 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC34165DW	T_A = 0° to +70°C	SOP–16L
MC34165P		DIP–16
MC33165DW	T_A = – 40° to +85°C	SOP–16L
MC33165P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	65	V
Switch Collector Voltage Range	$V_{C(switch)}$	–1.0 to + 65	V
Switch Emitter Voltage Range	$V_{E(switch)}$	– 2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	65	V
Switch Current (Note 1)	I_{SW}	1.5	A
Driver Collector Voltage	$V_{C(driver)}$	–1.0 to +65	V
Driver Collector Current	$I_{C(driver)}$	70	mA
Bootstrap Input Current Range (Note 1)	I_{BS}	–100 to +100	mA
Current Sense Input Voltage Range	$V_{Ipk(Sense)}$	(V_{CC}–7.0) to (V_{CC}+1.0)	V
Feedback and Timing Capacitor Input Voltage Range	V_{in}	–1.0 to + 7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	–1.0 to + 65	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Thermal Characteristics			°C/W
P Suffix, Dual In Line Case 648C			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Surface Mount Case 751G			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	94	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	18	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3)	T_A		°C
MC34165		0 to +70	
MC33165		– 40 to + 85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency	f_{OSC}				kHz
T_A = 25°C		46	50	54	
Total Variation over V_{CC} = 3.0 V to 65 V, and Temperature		45	–	55	
Charge Current	I_{chg}	–	225	–	µA
Discharge Current	I_{dischg}	–	25	–	µA
Charge to Discharge Current Ratio	I_{chg}/I_{dischg}	7.5	9.0	10	–
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	1.25	–	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	–	0.55	–	V
FEEDBACK COMPARATOR 1					
Threshold Voltage	$V_{th(FB1)}$				
T_A = 25°C		4.9	5.05	5.2	V
Line Regulation (V_{CC} = 3.0 V to 65 V, T_A = 25°C)		–	0.008	0.03	%/V
Total Variation over Line, and Temperature		4.85	–	5.25	V
Input Bias Current (V_{FB1} = 5.05 V)	$I_{IB(FB1)}$	–	100	200	µA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34165 T_{high} = + 70°C for MC34165
= – 40°C for MC33165 = + 85°C for MC33165
4. The Low Voltage Indicator threshold tracks $V_{th(FB2)}$ and is expressed as a percent of the $V_{th(FB2)}$ threshold.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FEEDBACK COMPARATOR 2					
Threshold Voltage	$V_{th(FB2)}$				
T_A = 25°C		1.225	1.25	1.275	V
Line Regulation (V_{CC} = 3.0 V to 65 V, T_A = 25°C)		–	0.008	0.03	%/V
Total Variation over Line, and Temperature		1.220	–	1.280	V
Input Bias Current (V_{FB2} = 1.25 V)	$I_{IB(FB2)}$	– 0.4	0	0.4	µA
CURRENT LIMIT COMPARATOR					
Threshold Voltage	$V_{th(Ipk\ Sense)}$				mV
T_A = 25°C		–	245	–	
Total Variation over V_{CC} = 3.0 V to 65 V, and Temperature		225	–	270	
Input Bias Current ($V_{Ipk\ (Sense)}$ = 15 V)	$I_{IB(sense)}$	–	1.0	5.0	µA
DRIVER AND OUTPUT SWITCH (Note 2)					
Sink Saturation Voltage (I_{SW} = 1.0 A, Pins 14, 15 grounded)	$V_{CE(sat)}$				V
Non–Darlington Connection ($R_{Pin\ 9}$ = 110 Ω to V_{CC}, I_{SW}/I_{DRV} ≈ 8)		–	0.3	0.7	
Darlington Connection (Pins 9, 10, 11 connected)		–	1.1	1.4	
Collector Off–State Leakage Current (V_{CE} = 65 V)	$I_{C(off)}$	–	0.02	100	µA
Bootstrap Input Current Source (V_{BS} = V_{CC} + 5.0 V)	$I_{source(DRV)}$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage (I_Z = 25 mA)	V_Z	V_{CC} + 6.0	V_{CC} + 7.0	V_{CC} + 9.0	V
LOW VOLTAGE INDICATOR					
LVI Threshold (Percent of V_{FB}, Note 4)	$V_{th(LVI)}$				%
V_{FB2} Decreasing		87	88.3	90	
V_{FB2} Increasing		88	89.9	92	
Hysteresis	V_H	–	20	–	mV
Output Sink Saturation Voltage (I_{sink} = 0.5 mA)	$V_{OL(LVI)}$	–	0.15	0.4	V
Output Off–State Leakage Current (V_{OH} = 15 V)	I_{OH}	–	0.01	1.0	µA
TOTAL DEVICE					
Standby Supply Current (V_{CC} = 3.0 V to 65 V, Pin 8 = V_{CC}, Pins 6, 14, 15 = Gnd, remaining pins open)	I_{CC}	–	6.0	10	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain as close to ambient as possible.
3. T_{low} = 0°C for MC34165 T_{high} = + 70°C for MC34165
= – 40°C for MC33165 = + 85°C for MC33165
4. The Low Voltage Indicator threshold tracks $V_{th(FB2)}$ and is expressed as a percent of the V_{FB2} threshold.

Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

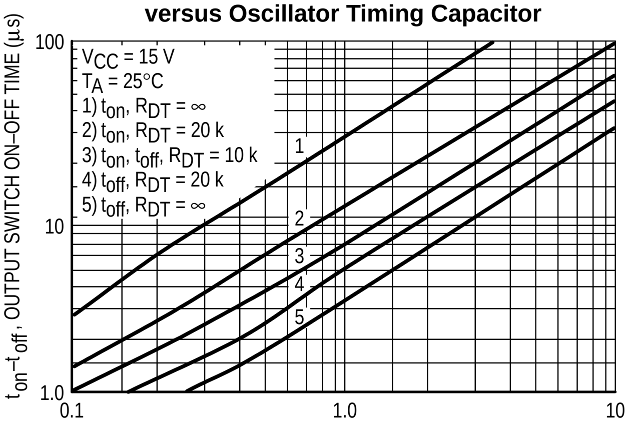
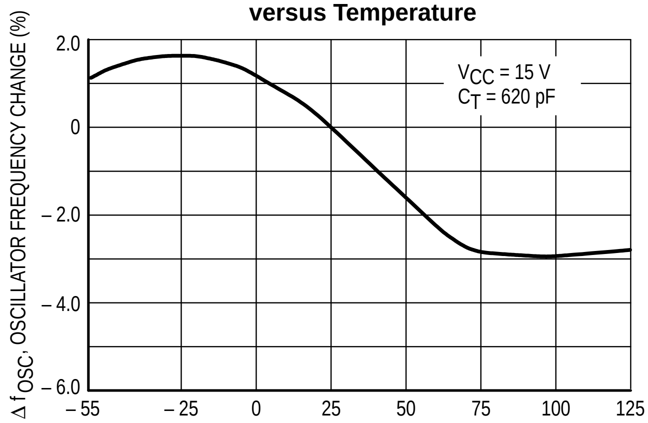


Figure 2. Oscillator Frequency Change versus Temperature



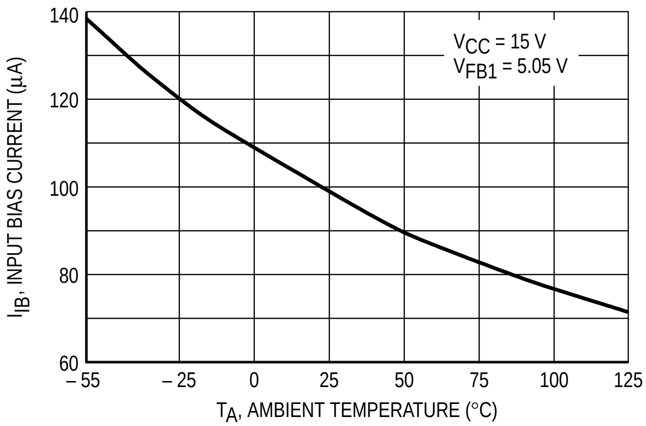


Figure 3. Feedback Comparator 1 Input Bias Current versus Temperature

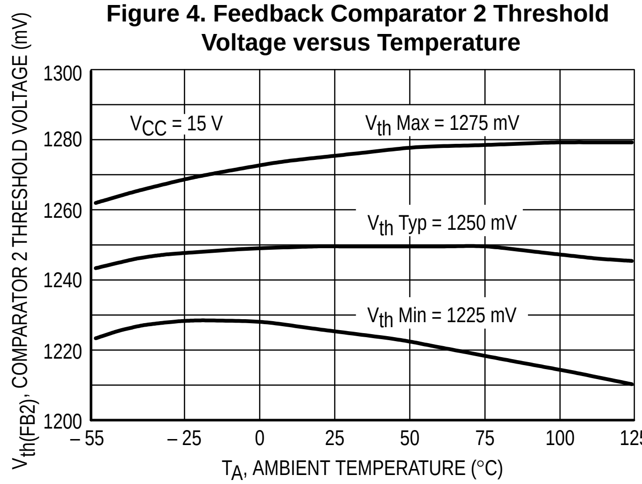


Figure 4. Feedback Comparator 2 Threshold Voltage versus Temperature

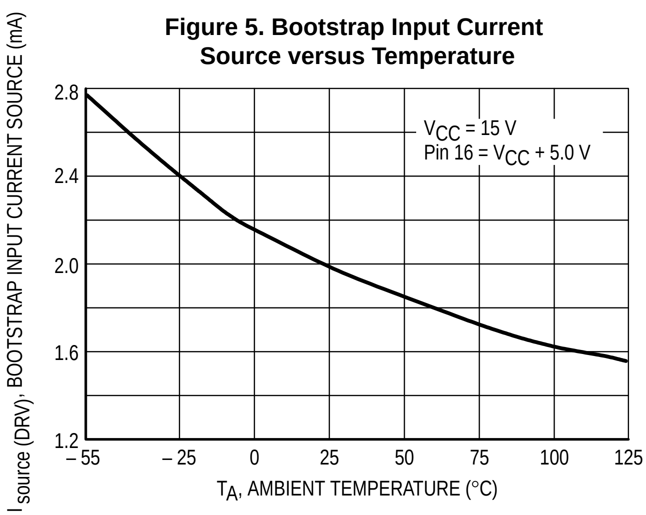


Figure 5. Bootstrap Input Current Source versus Temperature

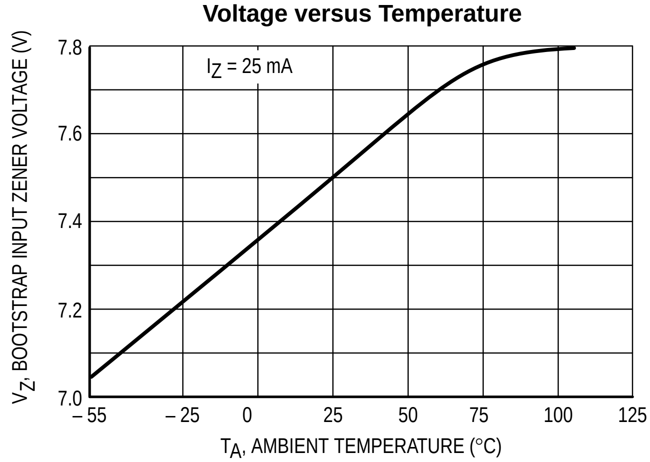


Figure 6. Bootstrap Input Zener Clamp Voltage versus Temperature

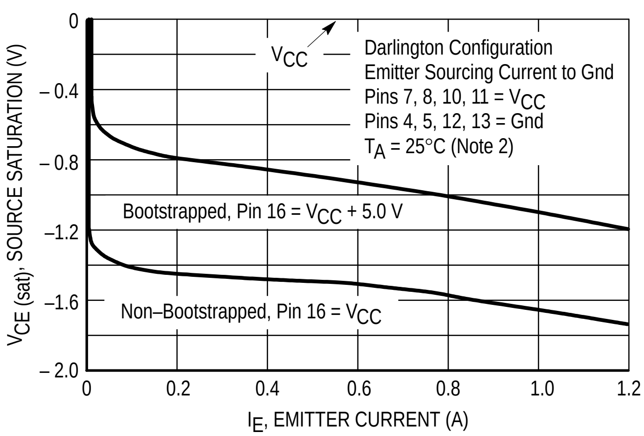


Figure 7. Output Switch Source Saturation versus Emitter Current

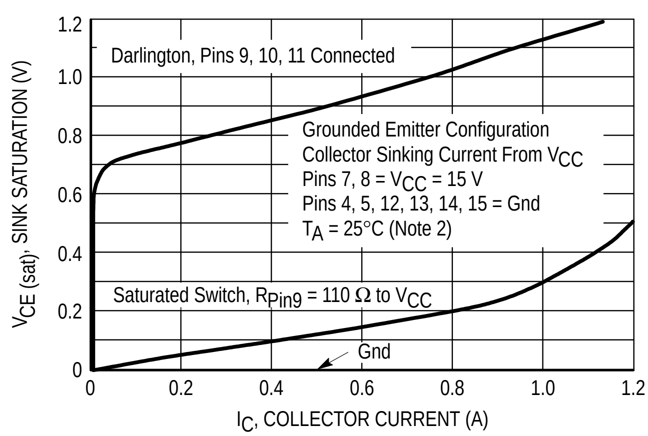


Figure 8. Output Switch Sink Saturation versus Collector Current

Figure 9. Output Switch Negative Emitter Voltage versus Temperature

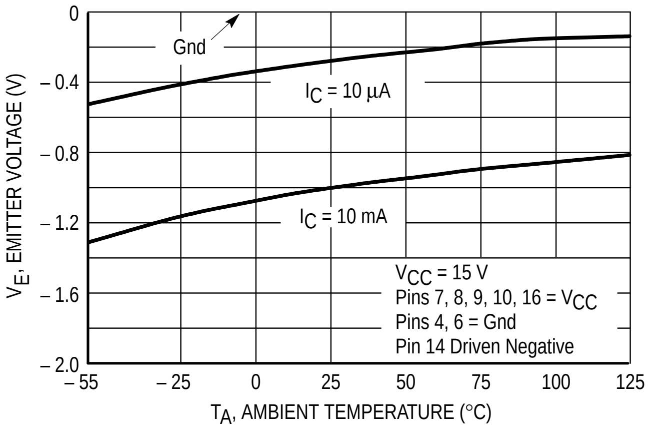


Figure 10. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

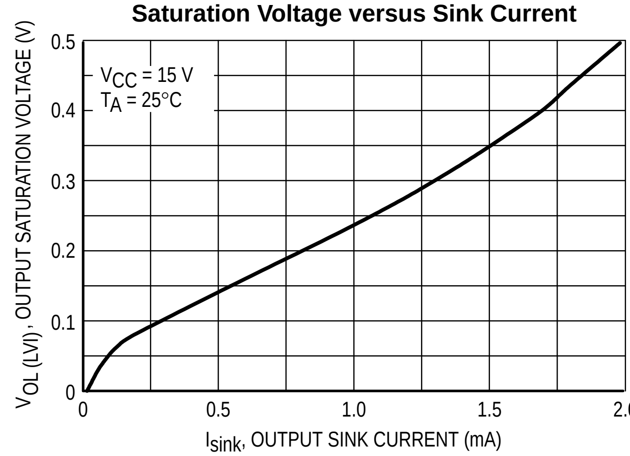


Figure 11. Current Limit Comparator Threshold Voltage versus Temperature

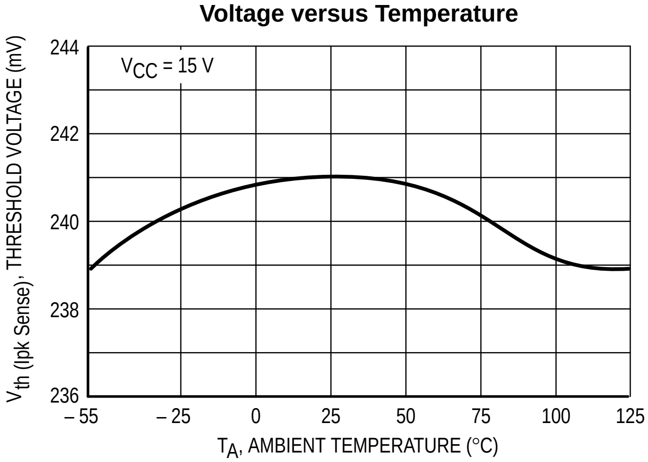


Figure 12. Current Limit Comparator Input Bias Current versus Temperature

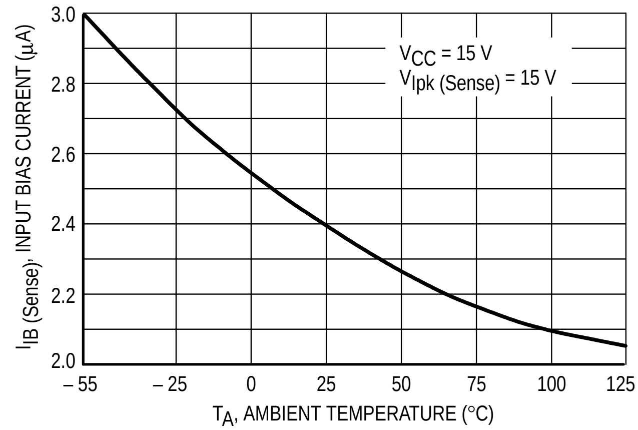


Figure 13. Standby Supply Current versus Supply Voltage

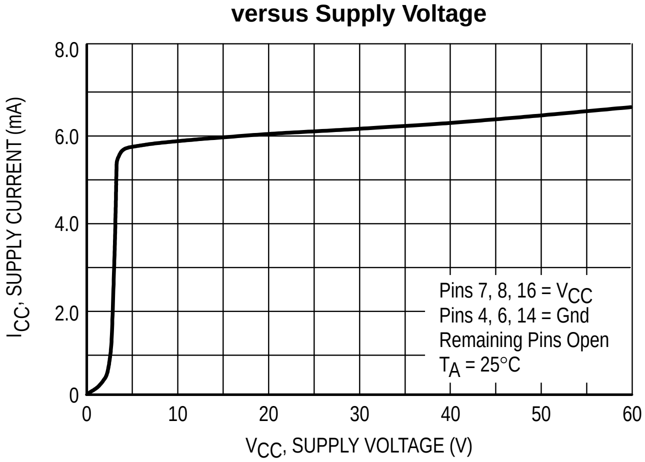


Figure 14. Standby Supply Current versus Temperature

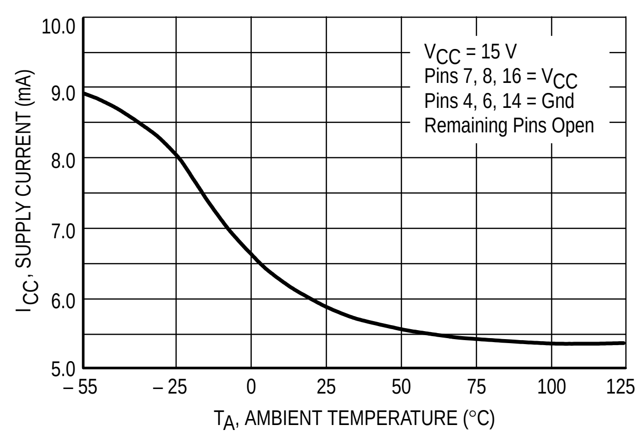


Figure 15. Minimum Operating Supply Voltage versus Temperature

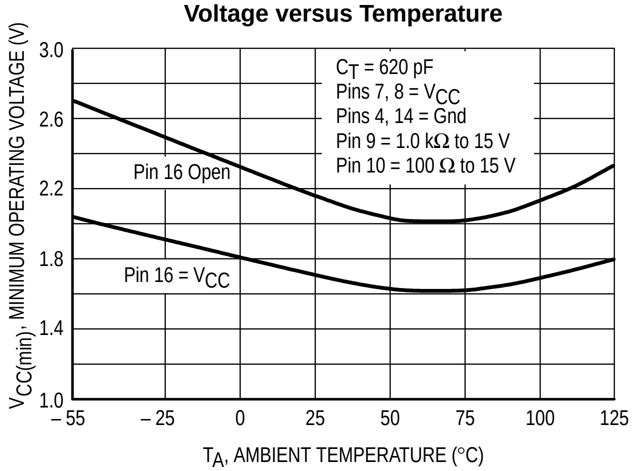


Figure 16. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

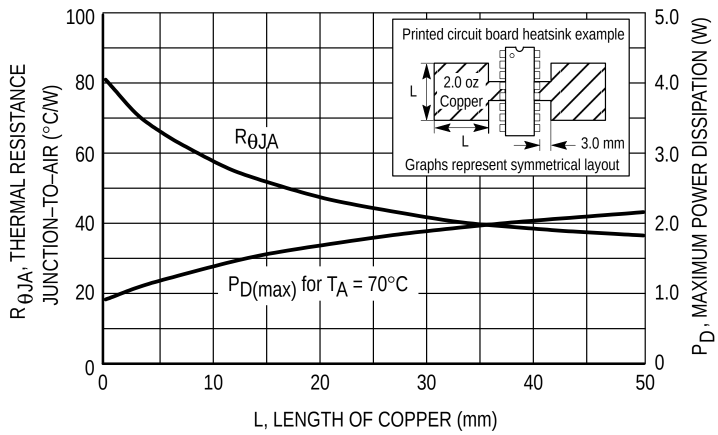


Figure 17. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

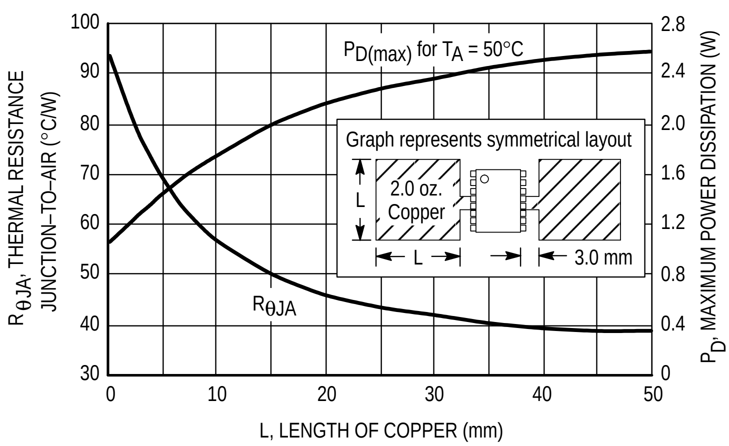


Figure 18. Representative Block Diagram

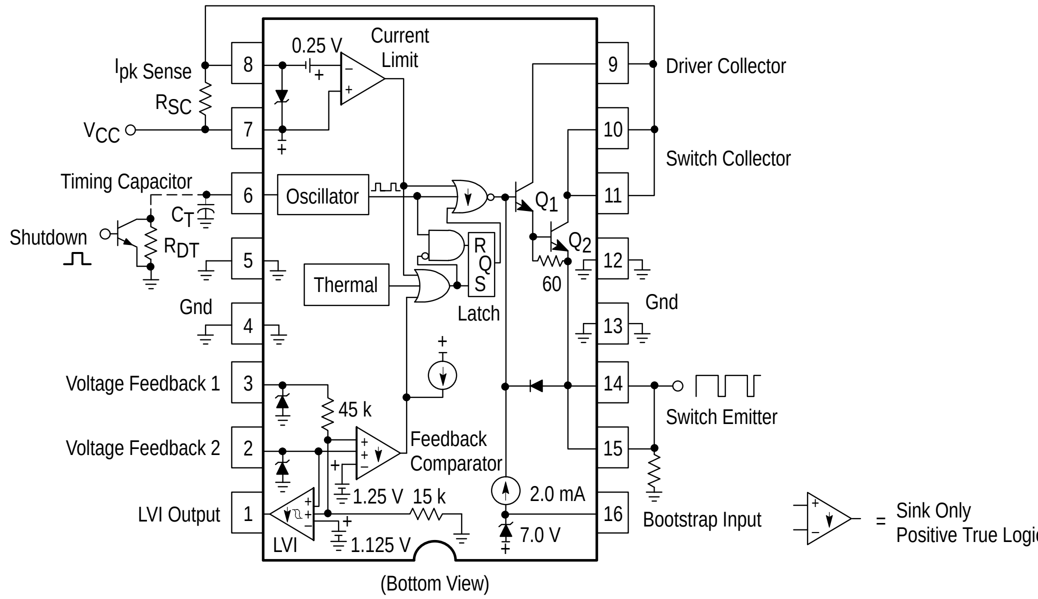
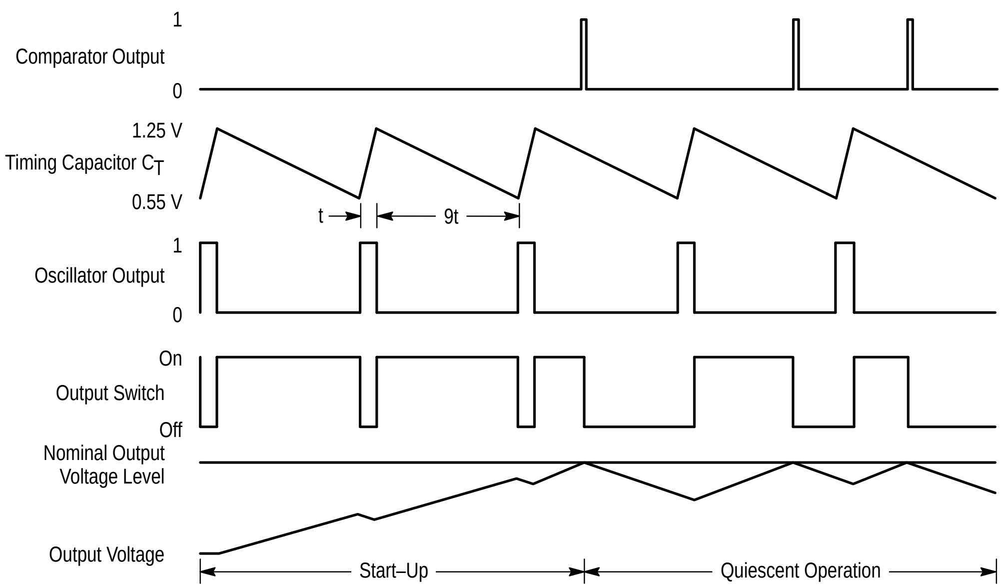


Figure 19. Typical Operating Waveforms



INTRODUCTION

The MC34165 series are monolithic power switching regulators optimized for DC–to–DC converter applications. The combination of features in this series enables the system designer to directly implement step–up, step–down, and voltage–inverting converters with a minimum number of external components. This series is constructed on a special high voltage process making it ideal for telecommunication applications. Other potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. The Representative Block Diagram is shown in Figure NO TAG.

OPERATING DESCRIPTION

The MC34165 operates as a fixed on–time, variable off–time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure NO TAG. The output voltage waveform shown is for a step–down converter, with the ripple and phasing exaggerated for clarity. During initial converter start–up, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on–time of the output switch are programmed by the value selected for timing capacitor C_T. Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp–up and can be enabled by the comparator output only at the start of ramp–down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 µA and a discharge current of 25 µA, yielding a maximum on–time duty cycle of 90%. Since the MC34165 is a ripple mode regulator, the switch frequency will vary with line and load. The value selected for C_T will set the maximum switching frequency of the converter. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external dead–time resistor (R_{DT}) placed across C_T. The resistor increases the discharge current which reduces the on–time of the output switch. A graph of the Output Switch On–Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 1. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small–signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is ±0.4 µA, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor–based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The open collector output is capable of sinking in excess of 1.5 mA (see Figure 10). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold. Refer to Figure NO TAG.

$$t_{DLY} = R_{LVI}\, C_{DLY} \ln\left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}}\right)$$

Current Limit Comparator, Latch and Thermal Shutdown

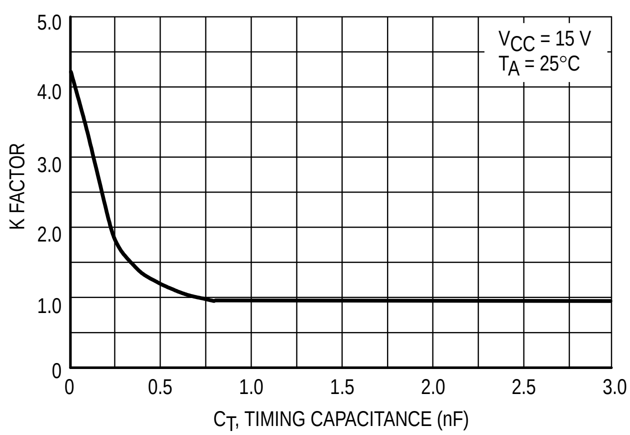
With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and output switch transistor Q_2. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle–by–cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on–time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25\ V \cdot K}{I_{pk\,(Switch)}}$$

The K factor was added to the previous equation in order to account for a 200 ns propagation delay that occurs from the Current Limit comparator input to the output switch. This propagation delay can cause the actual peak switch current to rise above the calculated peak switch current for small values of C_T. The following figure shows the relationship of the ratio $I_{pk(actual)}/I_{pk\ (Switch)}$, expressed as K versus C_T. Note the ratio rises above 1.0 for C_T values less than 1.0 nF.

Figure 20. K Factor versus Timing Capacitance



When analyzing a design, the actual short circuit current must be measured to verify that it is less than the maximum rating of the device.

Figures 11 and 12 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 μA. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the "Set" state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch is designed to switch a maximum of 65 V collector to emitter, with up to 1.5 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC(min)} = \frac{0.25\ V}{1.5\ A} = 0.166\ \Omega$$

When configured for step–down or voltage–inverting applications, as in Figures NO TAG and 24, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn–on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency.

Figure 9 shows that by clamping the emitter to less than 0.5 V, the collector current will be in the range 10 μA over temperature. A MBR160 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step–down and voltage–inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC}. An internal zener limits the bootstrap input voltage to V_{CC} +7.0 V. The capacitor's equivalent series resistance may be large enough to limit the zener current to less than the maximum 100 mA rating. However, in most high voltage applications, an additional series resistor will probably be required. It is recommended that this resistor limit the zener current to approximately 25 mA for optimal performance. The circuit can be optimized by adjusting the zener current (R_B) during operation, while observing the circuit's efficiency. The value of the series resistor can be calculated as follows:

$$R_B \approx \frac{V_{in(max)}}{I_Z}$$

The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(min)} = I\,\frac{\Delta t}{\Delta V} = 4.0\ mA\,\frac{t_{on}}{4.0\ V} = 0.001\ t_{on}$$

Parametric operation of the MC34165 is guaranteed over a supply voltage range of 3.0 V to 65 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC}. Figure 15 shows that non–parametric operation down to 1.7 V at room temperature is possible.

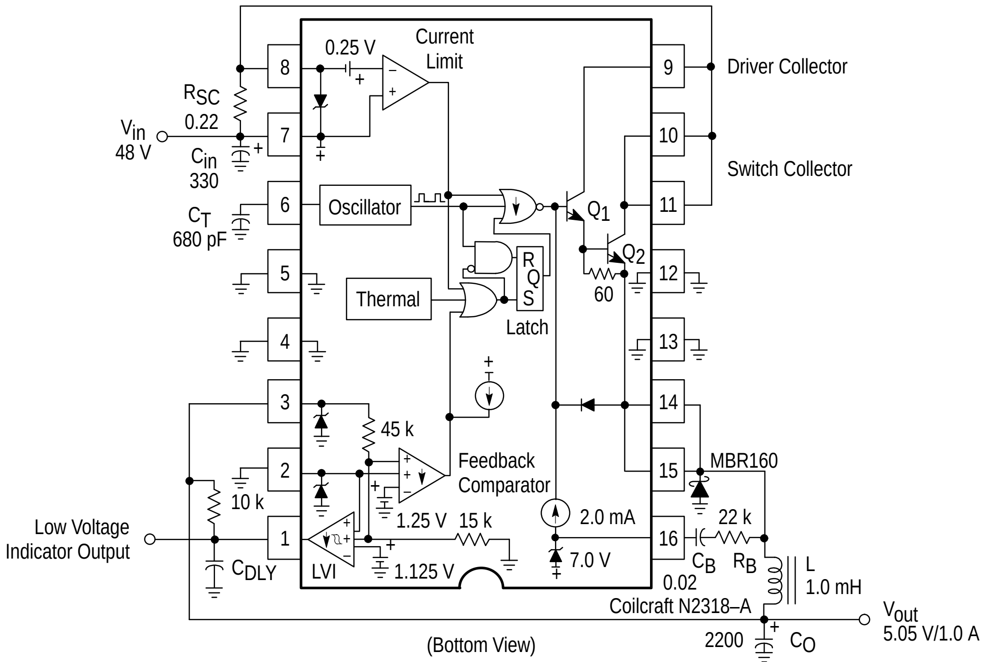
Package

The MC34165 is contained in a heatsinkable 16–lead plastic dual–in–line power package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 16 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction–to–air thermal resistance. These examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 21. Step–Down Converter



Test	Condition	Results
Line Regulation	V_{in} = 12 V to 56 V, I_O = 1.0 A	9.0 mV = ± 0.049%
Load Regulation	V_{in} = 48 V, I_O = 0.1 A to 1.0 A	9.0 mV = ± 0.049%
Output Ripple	V_{in} = 48 V, I_O = 1.0 A	20 mVp–p
Short Circuit Current	V_{in} = 48 V, R_L = 0.1 Ω	1.23 A
Efficiency, Without Bootstrap	V_{in} = 48 V, I_O = 1.0 A	74.9%
Efficiency, With Bootstrap	V_{in} = 48 V, I_O = 1.0 A	75.5%

L = 65 turns of # 18 AWG on Magenetics Inc. 55345–A2 core.

Figure 22. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 1.5 A

Figure 22A. External NPN Switch

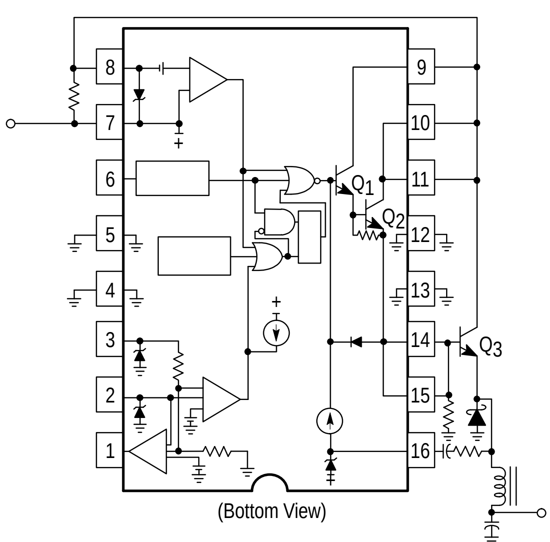


Figure 22B. External PNP Saturated Switch

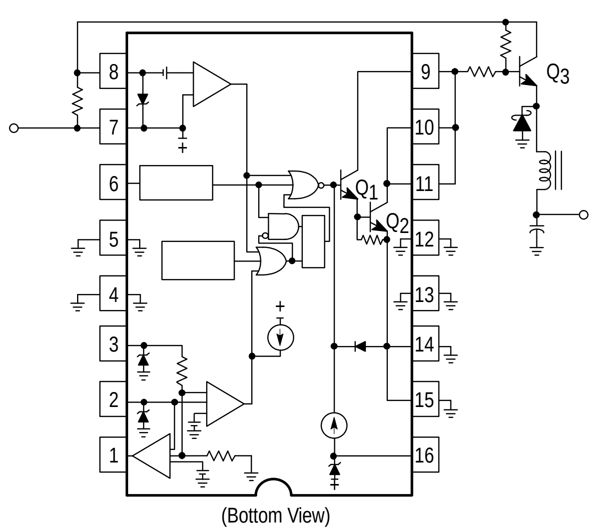
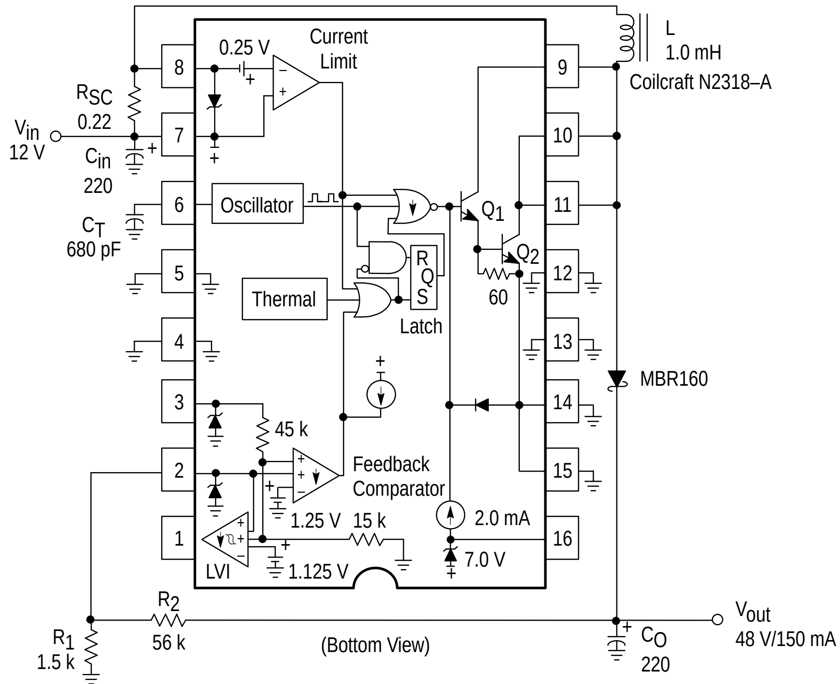


Figure 23. Step–Up Converter



Test	Condition	Results
Line Regulation	V_{in} = 10 V to 20 V, I_O = 150 mA	11 mV = ± 0.11%
Load Regulation	V_{in} = 12 V, I_O = 15 mA to 150 mA	9.0 mV = ± 0.09%
Output Ripple	V_{in} = 12 V, I_O = 150 mA	125 mVp–p
Efficiency	V_{in} = 12 V, I_O = 150 mA	85.8%

L = 65 turns of # 18 AWG on Magenetics Inc. 55345–A2 core.

Figure 24. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 1.5 A

Figure 24A. External NPN Switch

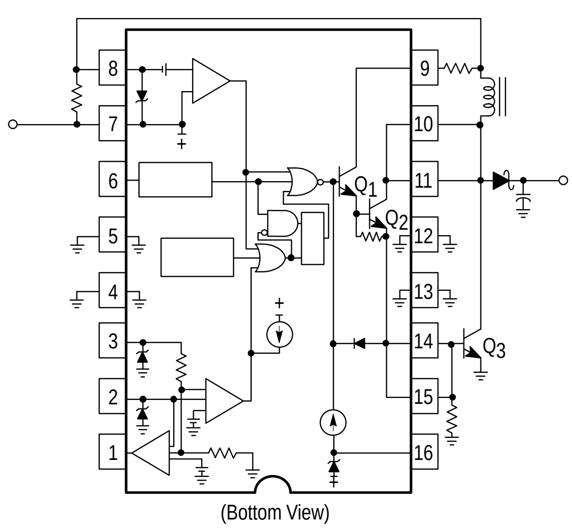


Figure 24B. External NPN Saturated Switch

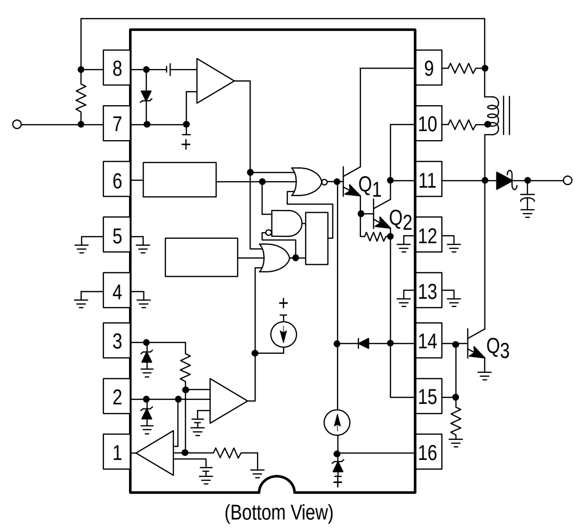
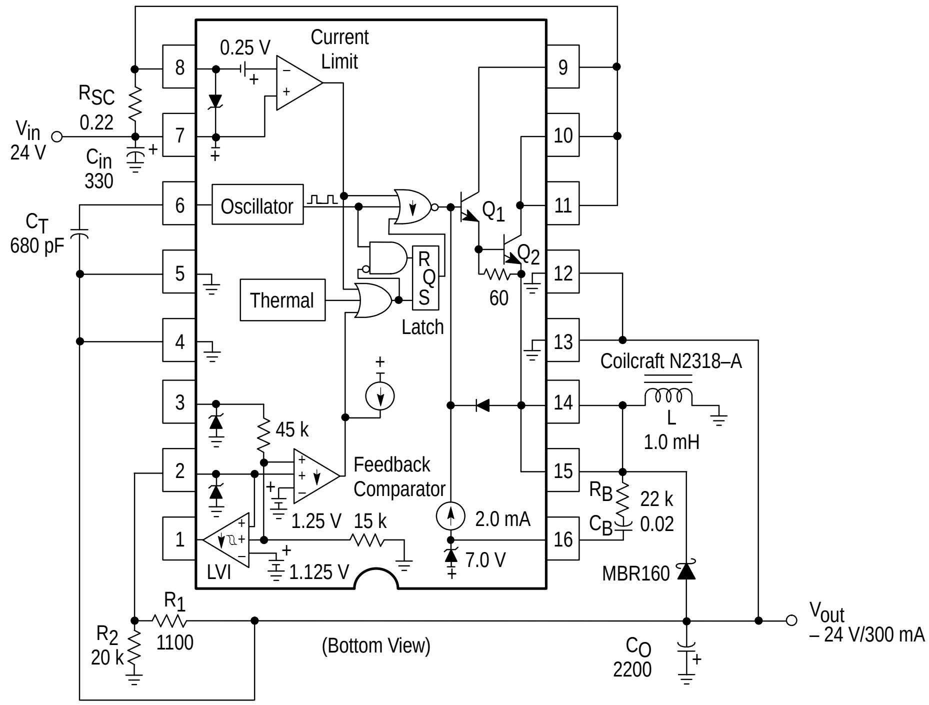


Figure 25. Voltage–Inverting Converter



Test	Condition	Results
Line Regulation	V_{in} = 15 V to 30 V, I_O = 300 mA	3.0 mV = ± 0.06%
Load Regulation	V_{in} = 24 V, I_O = 30 mA to 300 mA	1.0 mV = ± 0.02%
Output Ripple	V_{in} = 24 V, I_O = 300 mA	50 mVp–p
Short Circuit Current	V_{in} = 24 V, R_L = 0.1 Ω	1.12 A
Efficiency, Without Bootstrap	V_{in} = 24 V, I_O = 300 mA	81.3%
Efficiency, With Bootstrap	V_{in} = 24 V, I_O = 300 mA	82.7%

L = 65 turns of # 18 AWG on Magenetics Inc. 55345–A2 core.

Figure 26. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 1.5 A

Figure 26A. External NPN Switch

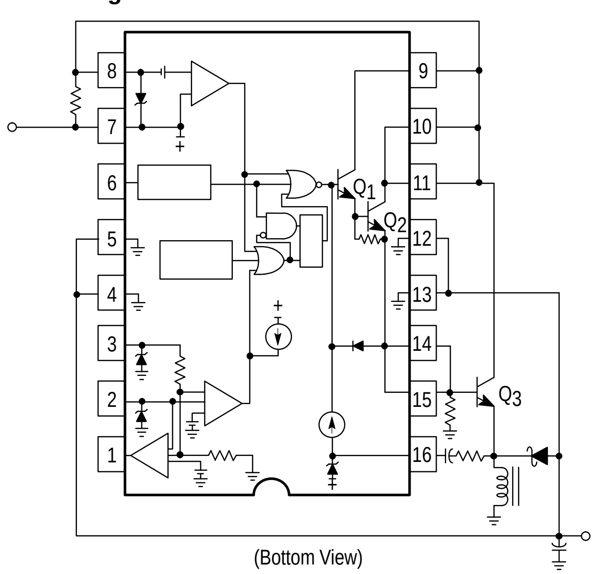


Figure 26B. External PNP Saturated Switch

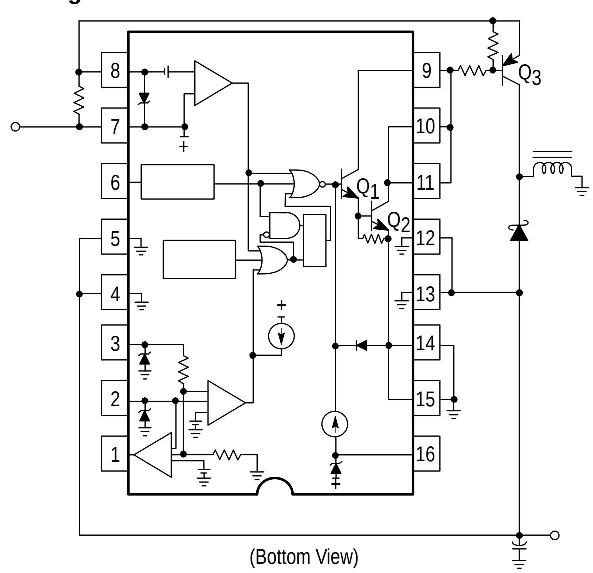
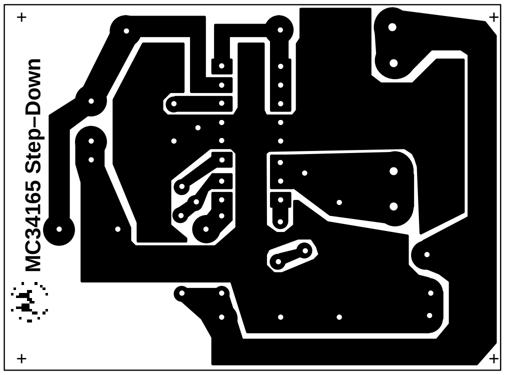
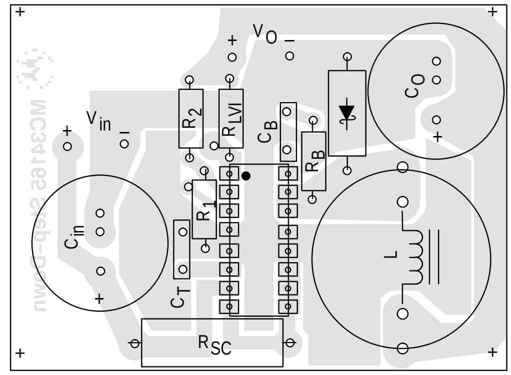


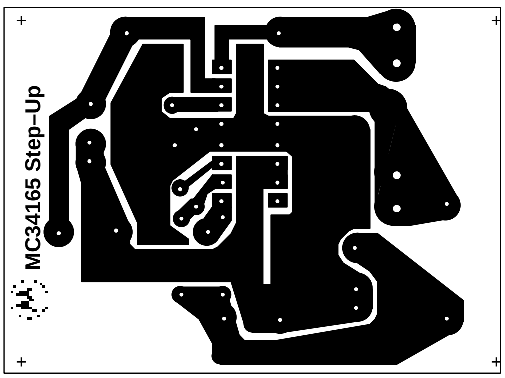
Figure 27. Printed Circuit Board and Component Layout
(Circuits of Figures 21, 23, 25)



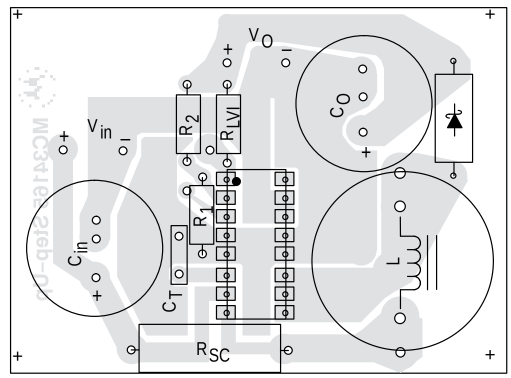
Bottom View



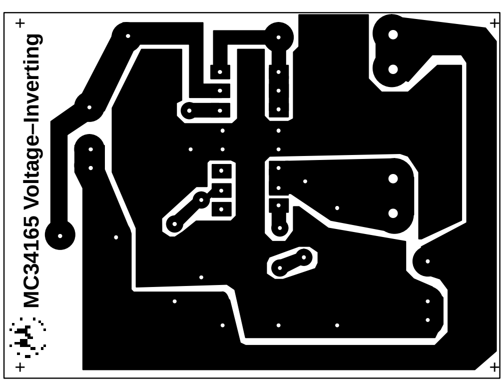
Top View



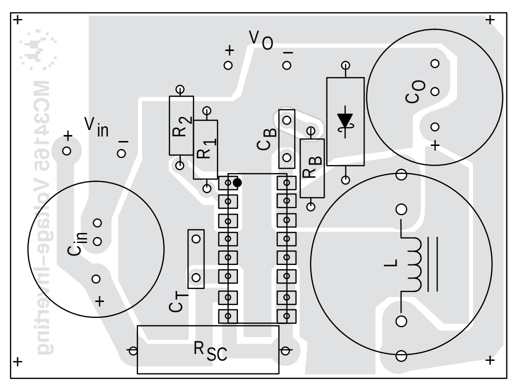
Bottom View



Top View



Bottom View



Top View

All printed circuit boards are 2.58" in width by 1.9" in height.

Table 1. Design Equations

Calculation	Step–Down	Step–Up	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2, 3)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
I_{pk} (Switch)	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.25 \cdot K}{I_{pk\,(Switch)}}$	$\frac{0.25 \cdot K}{I_{pk\,(Switch)}}$	$\frac{0.25 \cdot K}{I_{pk\,(Switch)}}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$
$V_{ripple(p–p)}$	$\Delta I_L \sqrt{\left(\frac{1}{8f\,C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on}\,I_{out}}{C_O}$	$\approx \frac{t_{on}\,I_{out}}{C_O}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

The following Converter Characteristics must be chosen:

V_{in} – Nominal operating input voltage.

V_{out} – Desired output voltage.

I_{out} – Desired output current.

ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current, it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\,(Switch)}$ from reaching the current threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.

f – Maximum output switch frequency.

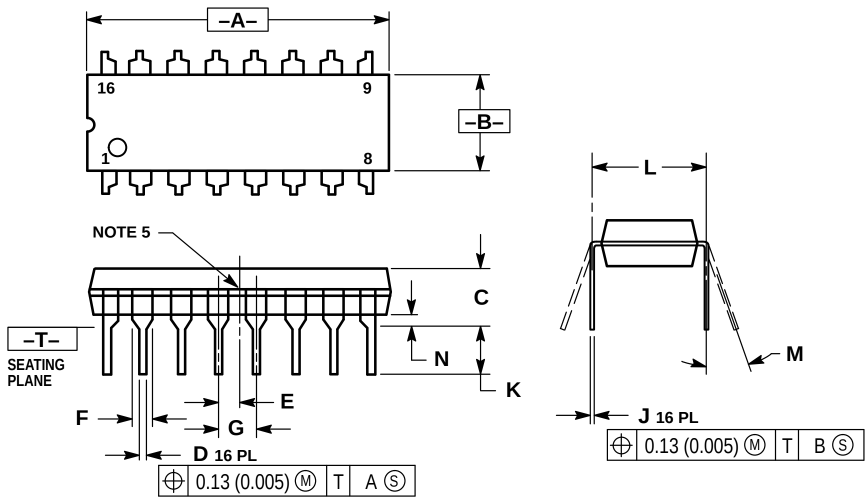
$V_{ripple(p–p)}$ – Desired peak–to–peak output ripple voltage. For best performance, the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

K – Multiplier number as determined by Figure 20, for determining the appropriate value for R_{SC}.

NOTES: 1. V_{sat} – Saturation voltage of the output switch, refer to Figures 7 and 8.
2. V_F – Output rectifier forward voltage drop. Typical value for MBR160 Schottky barrier rectifier is 0.6 V.
3. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

OUTLINE DIMENSIONS

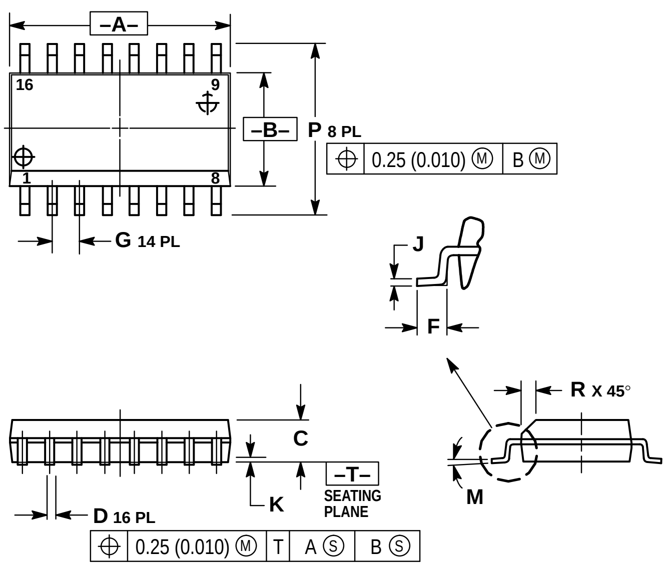
P SUFFIX
PLASTIC PACKAGE
CASE 648C–03
(DIP–16)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. INTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.840	18.80	21.34
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
E	0.050 BSC		1.27 BSC	
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.040	0.39	1.01

DW SUFFIX
PLASTIC PACKAGE
CASE 751G–02
(SOP–16L)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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