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MOTOROLA

MC26S10

Quad Open-Collector Bus Transceiver

This quad transceiver is designed to mate Schottky TTL or NMOS logic to a low impedance bus. The Enable and Driver inputs are PNP buffered to ensure low input loading. The Driver (Bus) output is open–collector and can sink up to 100 mA at 0.8 V, thus the bus can drive impedances as low as 100 Ω. The receiver output is active pull–up and can drive ten Schottky TTL loads.

An active–low $\overline{\text{Enable}}$ controls all four drivers allowing the outputs of different device drivers to be connected together for party–line operation. The line can be terminated at both ends and still give considerable noise margin at the receiver. Typical receiver threshold is 2.0 V.

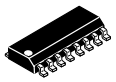
Advanced Schottky processing is utilized to assure fast propagation delay times. Two ground pins are provided to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both ground pins should be tied to the ground bus external to the package.

- Driver Can Sink 100 mA at 0.8 V (Maximum)
- PNP Inputs for Low–Logic Loading
- Typical Driver Delay = 10 ns
- Typical Receiver Delay = 10 ns
- Schottky Processing for High Speed
- Inverting Driver

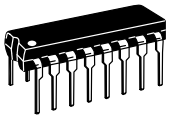
QUAD OPEN–COLLECTOR BUS TRANSCEIVER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



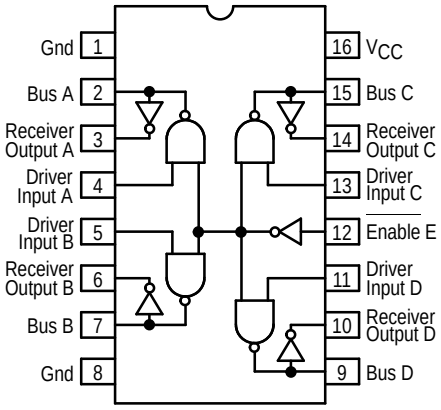
P SUFFIX
PLASTIC PACKAGE
CASE 648



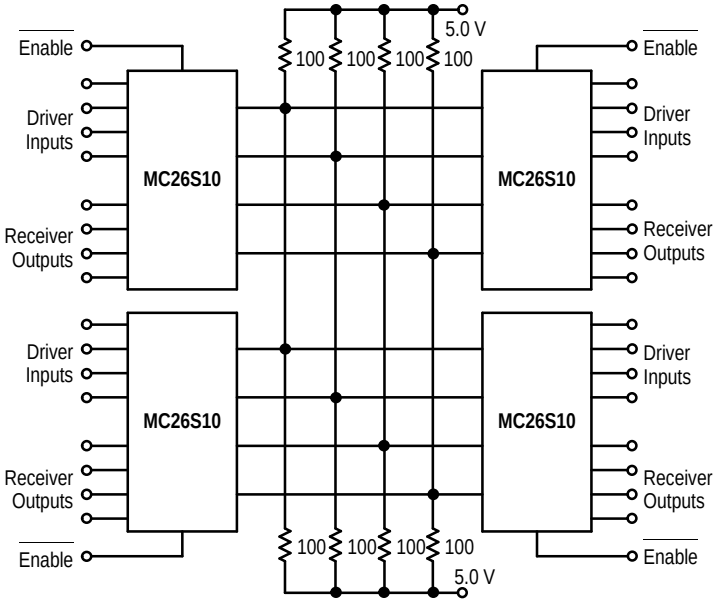
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC26S10P	T_A = 0 to +70°C	Plastic DIP
MC26S10D		SO–16

PIN CONNECTIONS



Simplified Application



TRUTH TABLE

$\overline{\text{Enable}}$	Driver Input	Bus	Receiver Output
L	L	H	L
L	H	L	H
H	X	Y	Y

L = Low Logic State
H = High Logic State
X = Irrelevant
Y = Assumes condition controlled by other elements on the bus

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	Vdc
Input Voltage	V_I	–0.5 to +5.5	Vdc
Input Current	I_I	–3.0 to +5.0	mA
Output Voltage – High Impedance State	$V_{O\ (Hi–z)}$	–0.5 to V_{CC}	V
Output Current – Bus	$I_{O(B)}$	200	mA
Output Current – Receiver	$I_{O(R)}$	30	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = 4.75 to 5.25 V and T_A = 0 to +70°C. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IL}	–	–	0.8	V
Input voltage – High Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IH}	2.0	–	–	V
Input Clamp Voltage (Driver and Enable Inputs) (I_{IK} = –18 mA)	V_{IK}	–	–	–1.2	V
Input Current – Low Logic State (V_{IL} = 0.4 V) (Enable Input) (Driver Inputs)	I_{IL}	 – –	 – –	 –0.36 –0.54	mA
Input Current – High Logic State (V_{IH} = 2.7 V) (Enable Input) (Driver Inputs)	I_{IH}	 – –	 – –	 20 30	µA
Input Current – Maximum Voltage (V_{IH1} = 5.5 V) (Enable or Driver Inputs)	I_{IH1}	–	–	100	µA
Driver Output Voltage – Low Logic State (I_{OL} = 40 mA) (I_{OL} = 70 mA) (I_{OL} = 100 mA)	$V_{OL(D)}$	 – – –	 0.33 0.42 0.51	 0.5 0.7 0.8	V
Driver (Bus) Leakage Current (V_{OH} = 4.5 V) (V_{OL} = 0.8 V)	$I_{O(D)}$	 – –	 – –	 100 –50	µA
Driver (Bus) Leakage Current (V_{CC} = 0 V, V_{OH} = 4.5 V)	$I_{O1(D)}$	–	–	100	µA
Receiver Input High Threshold ($V_{IH(E)}$ = 2.4 V)	$V_{TH(R)}$	2.25	2.0	–	V
Receiver Input Low Threshold ($V_{IH(E)}$ = 2.4 V)	$V_{TL(R)}$	–	2.0	1.75	V
Receiver Output Voltage – Low Logic State (I_{OL} = 20 mA)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Voltage – High Logic State (I_{OH} = –1.0 mA)	$V_{OH(R)}$	2.7	3.4	–	V
Receiver Output Short–Circuit Current (Note1)	$I_{OS(R)}$	–18	–	–60	mA
Power Supply Current – Output Low State ($V_{IL(E)}$ = 0 V)	I_{CC}	–	45	70	mA

NOTE: 1. One output shorted at a time. Duration not to exceed 1.0 second.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Driver Input to Output	$t_{PLH(D)}$ $t_{PHL(D)}$	– –	10 10	15 15	ns
Propagation Delay Time Enable Input to Output	$t_{PLH(\overline{E})}$ $t_{PHL(E)}$	– –	14 13	18 18	ns
Propagation Delay Time Bus to Receiver Output	$t_{PLH(R)}$ $t_{PHL(R)}$	– –	10 10	15 15	ns
Rise and Fall Time of Driver Output	$t_{TLH(D)}$ $t_{THL(D)}$	4.0 2.0	10 4.0	– –	ns

SWITCHING WAVEFORMS AND CIRCUITS

Figure 1. Data Input to Bus Output (Driver)

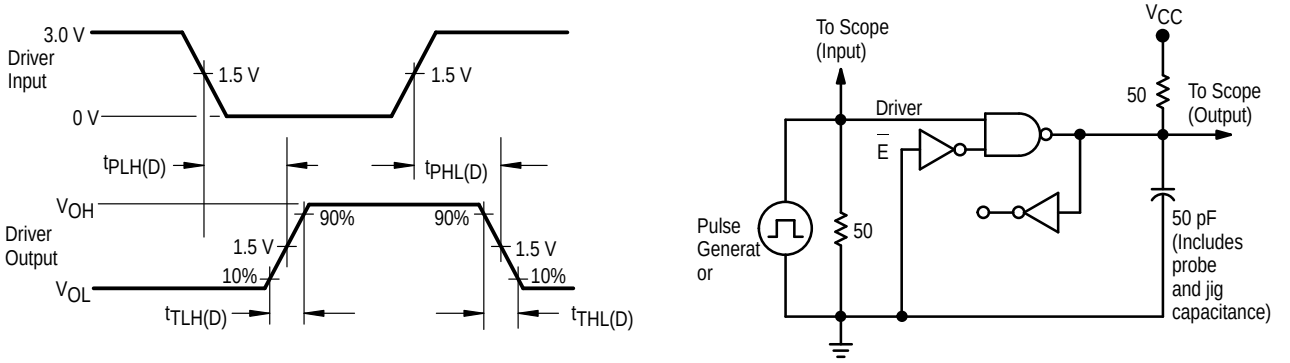


Figure 2. Enable Input to Bus Output (Driver)

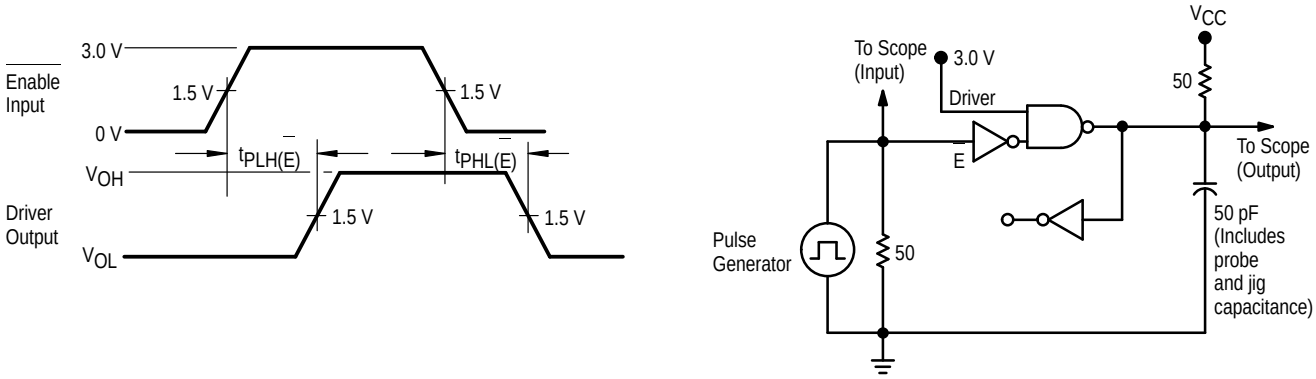
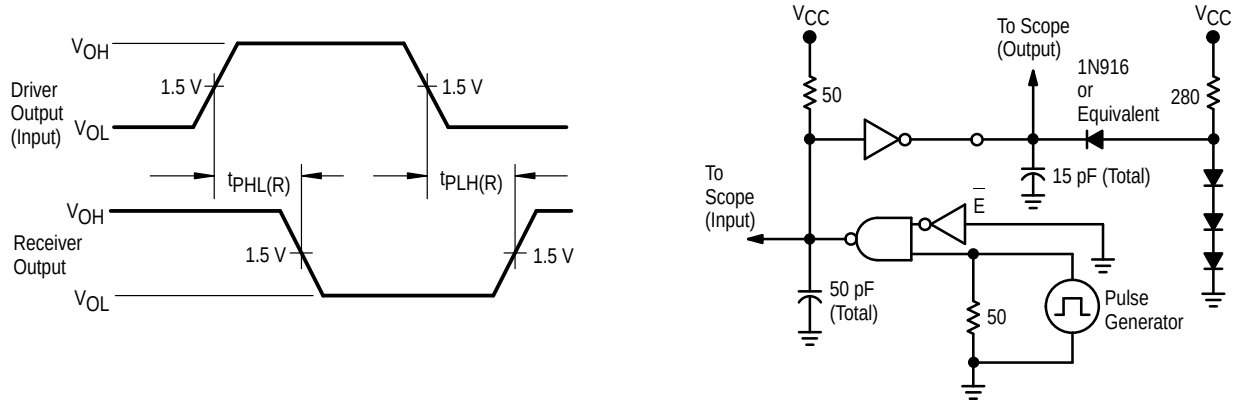
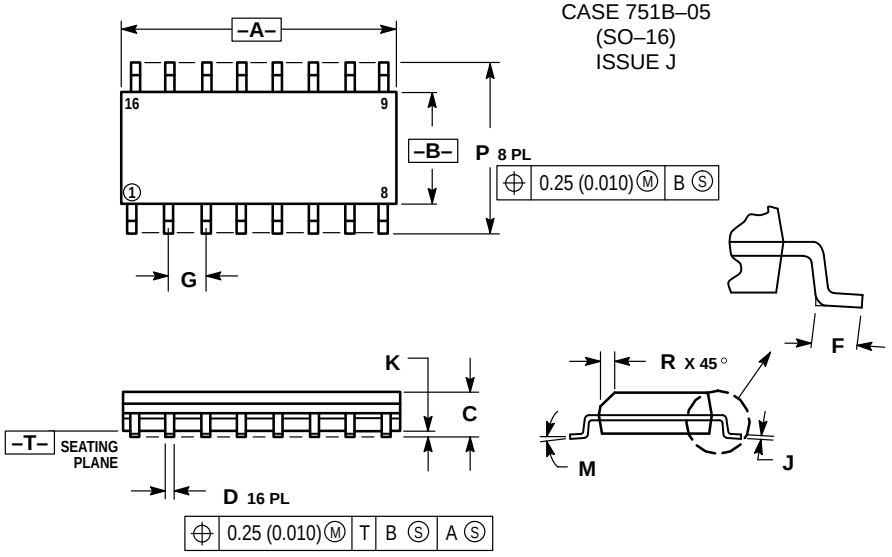


Figure 3. Bus Input to Receiver Output



OUTLINE DIMENSIONS

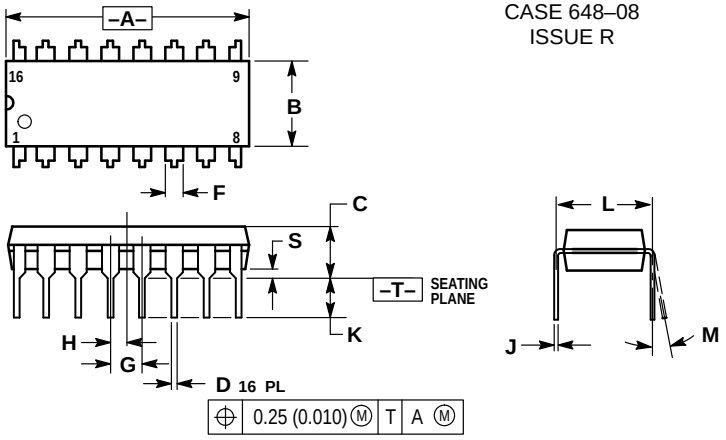
D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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