


MOTOROLA

Dual Peripheral-High-Voltage Positive "NAND" Driver

The dual driver consists of a pair of PNP buffered AND gates connected to the bases of a pair of high voltage NPN transistors. They are similar to the MC75452 drivers but with the added advantages of: 1) 70 V capability 2) output suppression diodes and 3) PNP buffered inputs for MOS compatibility. These features make the MC1472 ideal for mating MOS logic or microprocessors to lamps, relays, printer hammers and incandescent displays.

- 300 mA Output Capability (each transistor)
- 70 Vdc Breakdown Voltage
- Internal Output Clamp Diodes
- Low Input Loading for MOS Compatibility (PNP buffered)

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_{in}	5.5	V
Output Voltage	V_{out}	80	V
Clamp Voltage	V_C	80	V
Output Current (Continuous)	I_O	399	mA
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to + 150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	Volts
Operating Ambient Temperature	T_A	0	70	$^\circ\text{C}$
Output Voltage	V_O	V_{CC}	70	Volts
Clamp Voltage	V_C	V_O	70	Volts

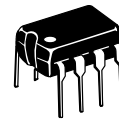
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1472P1	$T_A = 0$ to $+70^\circ\text{C}$	Plastic DIP

MC1472

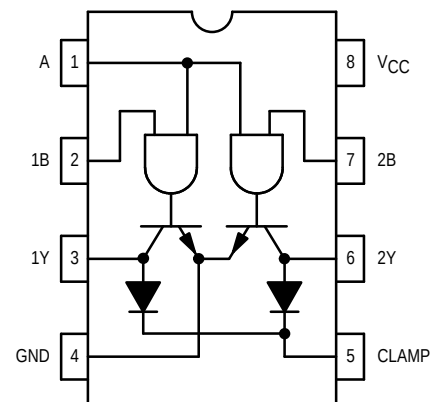
DUAL PERIPHERAL POSITIVE "NAND" DRIVER

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS



Positive Logic: $Y = AB$

TRUTH TABLE

A	B	Y
L	L	H ("OFF" STATE)
L	H	
H	L	
H	H	L ("ON" STATE)

H = Logic One
L = Logic Zero

MC1472

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, min/max limits apply across the 0°C to 70°C temperature range with $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$. All typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$.)

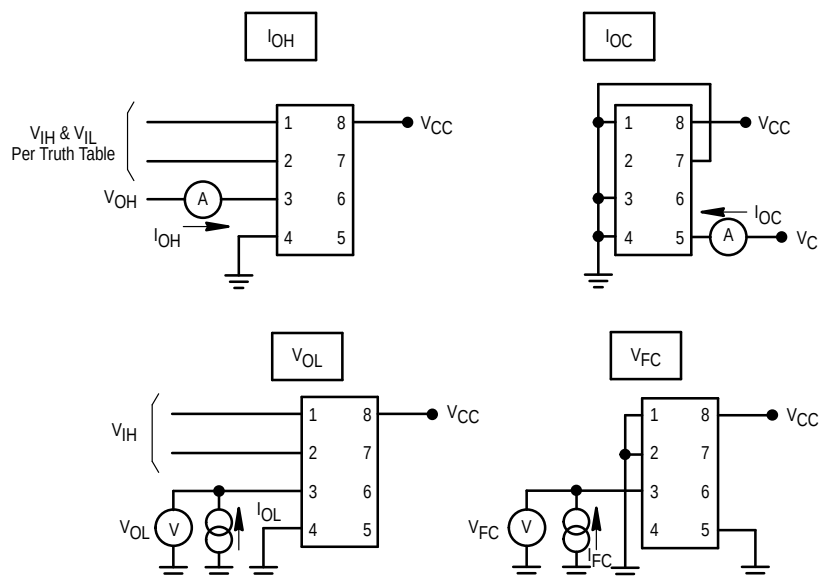
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State	V_{IH}	2.0	–	5.5	Vdc
Input Voltage – Low Logic State	V_{IL}	0	–	0.8	Vdc
Input Current – Low Logic State ($V_{IL} = 0.4\text{ V}$) A Input B Input	I_{IL}	–	–	– 0.3 – 0.15	mA
Input Current – High Logic State ($V_{IH} = 2.4\text{ V}$) A Input B Input ($V_{IH} = 5.5\text{ V}$) A Input B Input	I_{IH}	– – – –	– – – –	40 20 200 100	μA
Input Clamp Voltage ($I_{CC} = -12\text{ mA}$)	V_{IK}	–	–	– 1.5	V
Output Leakage Current – High Logic State ($V_O = 70\text{ V}$, See Test Figure)	I_{OH}		–	100	μA
Output Voltage – Low Logic State ($I_{OL} = 100\text{ mA}$) ($I_{OL} = 300\text{ mA}$)	V_{OL}	– –	– –	0.4 0.7	V
Output Clamp Diode Leakage Current ($V_C = 70\text{ V}$, See Test Figure)	I_{OC}	–	–	100	V
Output Clamp Forward Voltage ($I_{FC} = 300\text{ mA}$, See Test Figure)	V_{FC}	–	–	1.7	V
Power Supply Current (All Inputs at V_{IH}) (All Inputs at V_{IL})	I_{CC}	– –	– –	70 15	mA

NOTE: All currents into device pins are shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted.

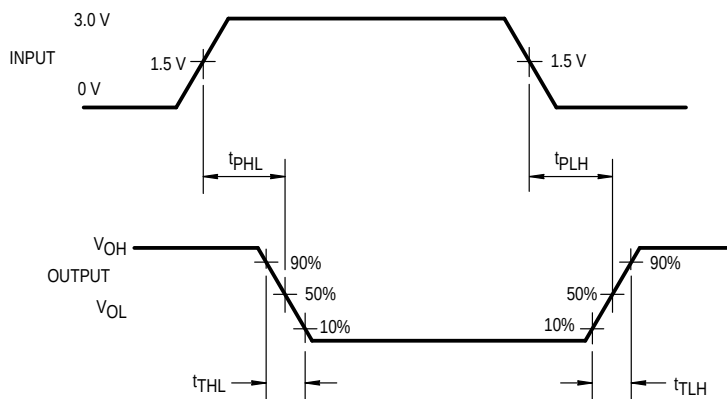
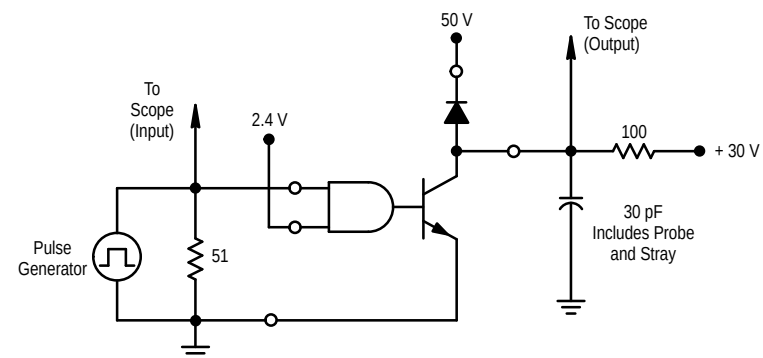
SWITCHING CHARACTERISTICS $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Output High to Low Output Low to High	t_{PHL} t_{PLH}	– –	– –	1.0 0.75	μs
Output Transition Time Output High to Low Output Low to High	t_{THL} t_{TLH}	– –	– –	0.1 0.1	μs

TEST CIRCUITS

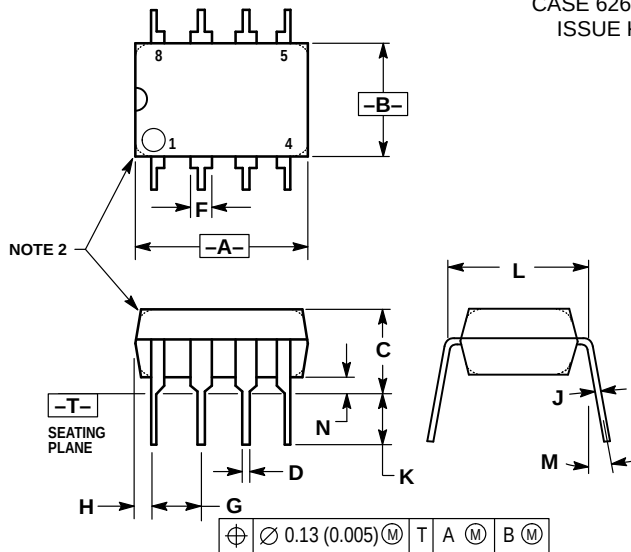


SWITCHING TEST CIRCUIT AND WAVEFORM



OUTLINE DIMENSIONS

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
ISSUE K



NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	10°		10°	
N	0.76	1.01	0.030	0.040

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