MC14580B

4 x 4 Multiport Register

The MC14580B is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

- No Restrictions on Clock Input Rise or Fall Times
- 3–State Outputs
- Single Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or one Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin Compatible with CD40108

L SUFFIX
CERAMIC
CASE 623

P SUFFIX
PLASTIC
CASE 709

DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

T_A = – 55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

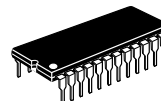* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
    Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
    Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT

Q3$_B$	1 •	24	V_{DD}
Q2$_B$	2	23	Q1$_B$
3–STATE A	3	22	Q0$_B$
Q0$_A$	4	21	3–STATE B
Q1$_A$	5	20	D0
Q2$_A$	6	19	D1
Q3$_A$	7	18	D2
WRITE 0	8	17	D3
WRITE 1	9	16	CLOCK
READ 1$_B$	10	15	WE
READ 0$_B$	11	14	READ 1$_A$
V_{SS}	12	13	READ 0$_A$

BLOCK DIAGRAM

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MOTOROLA
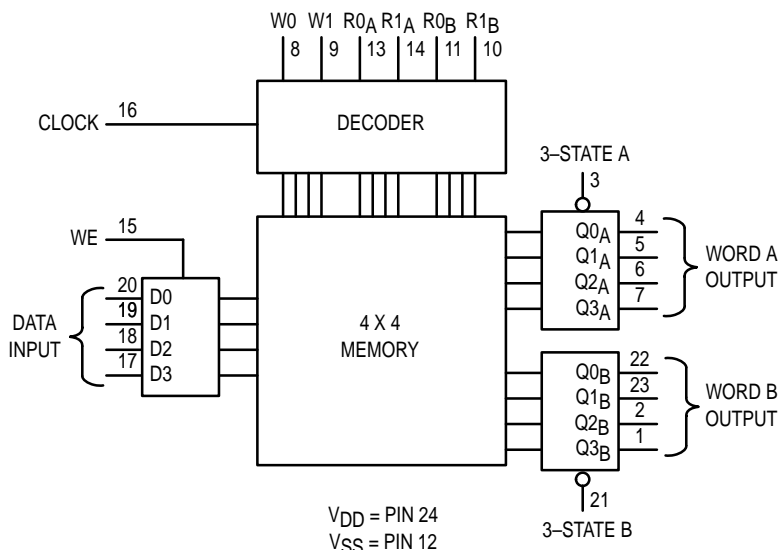
ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	− 3.0 − 0.64 − 1.6 − 4.2	— — — —	− 2.4 − 0.51 − 1.3 − 3.4	− 4.2 − 0.88 − 2.25 − 8.8	— — — —	− 1.7 − 0.36 − 0.9 − 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.010 0.020 0.030	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15			I_T = (1.18 µA/kHz) f + I_{DD} I_T = (1.91 µA/kHz) f + I_{DD} I_T = (2.67 µA/kHz) f + I_{DD}					µAdc
Three–State Leakage Current	I_{TL}	15	—	± 0.1	—	±0.0001	±0.1	—	±3.0	µAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L − 50) \text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL} (Figures 3 and 6)	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Output	t_{PLH}, t_{PHL} (Figures 3 and 6)	5.0 10 15	— — —	650 250 170	1300 500 340	ns
Write Enable Setup Time (Enabling a Write or Read)	t_{su} (Figure 5)	5.0 10 15	800 300 200	400 150 100	— — —	ns
Write Enable Removal Time (Disabling a Write or Read)	t_{rem} (Figure 5)	5.0 10 15	0 0 0	– 100 – 50 – 35	— — —	ns
Setup Time** Address, Data to Clock	t_{su} (Figure 3)	5.0 10 15	50 30 25	20 0 0	— — —	ns
Hold Time** Clock to Address, Data	t_h (Figure 3)	5.0 10 15	480 195 150	160 65 50	— — —	ns
3–State Enable/Disable Delay Time	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL} (Figures 4 and 7)	5.0 10 15	— — —	130 60 45	260 120 90	ns
Clock Pulse Width	t_w (Figure 3)	5.0 10 15	820 330 220	410 165 110	— — —	ns

** When loading repetitive highs, the output may glitch low momentarily after the rising edge of Clock. However, data integrity remains unaffected and data is valid after the propagation delays listed in the Switching Characteristics Table.

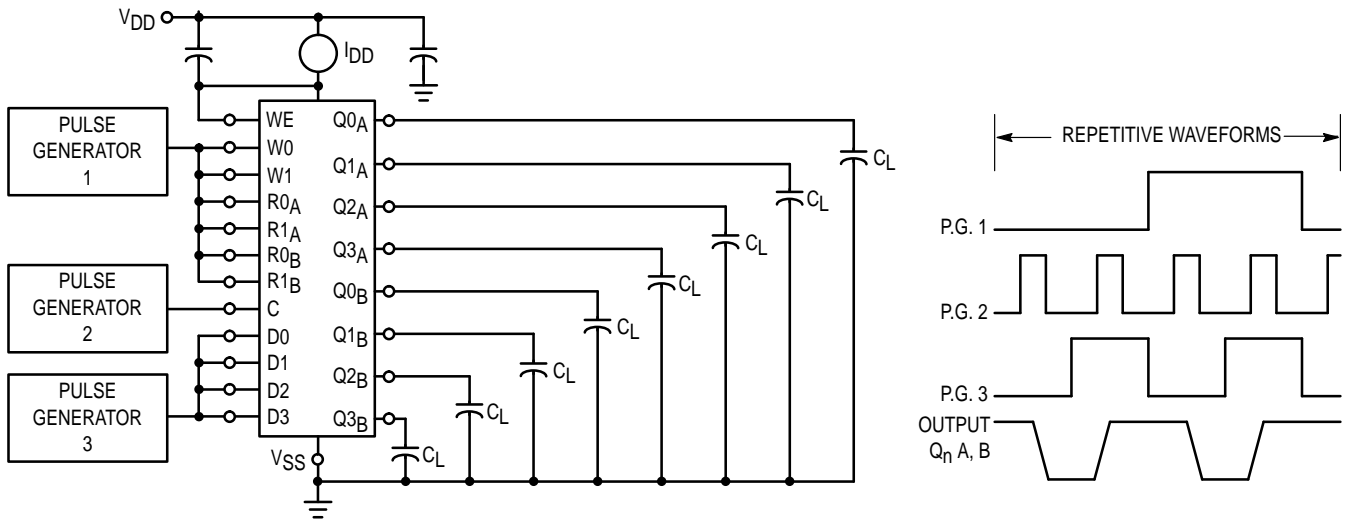|	Sink Current	Source Current
Position of S1	2	1
V_{GS} =	V_{DD}	– V_{DD}
V_{DS} =	V_{out}	V_{out} – V_{DD}
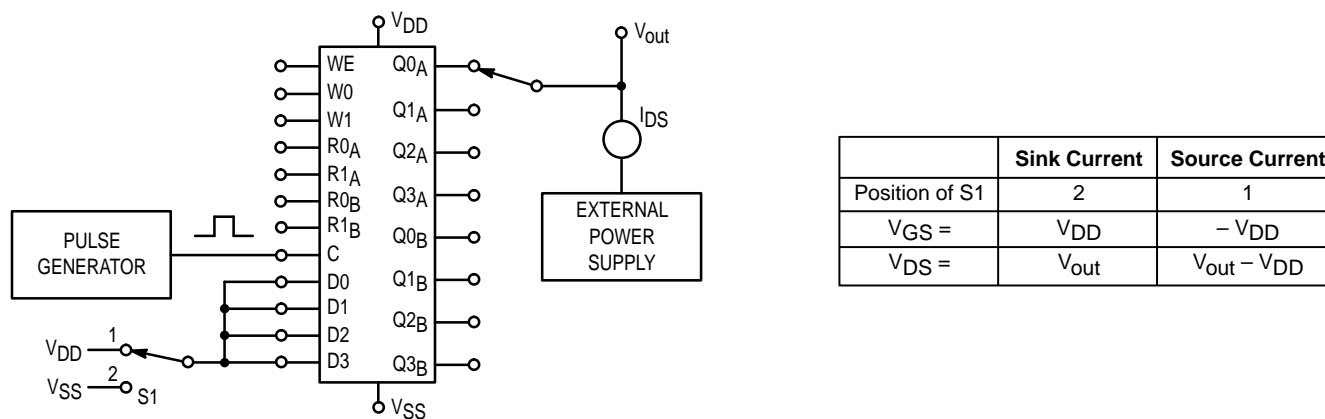
Figure 1. Output Drive Current Test Circuit

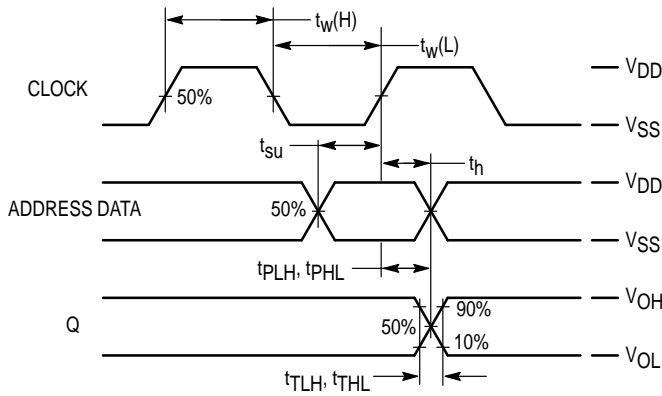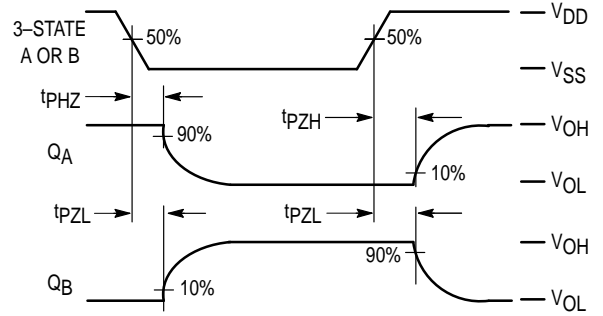**Figure 2. Power Dissipation Test Circuit and Waveforms** (3–State Inputs are High)
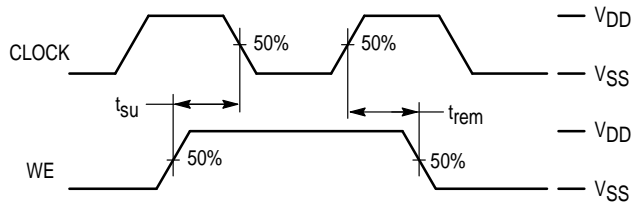

Figure 3.

Figure 4.

Figure 5.

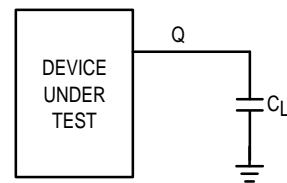**Figure 6. Test Circuit**
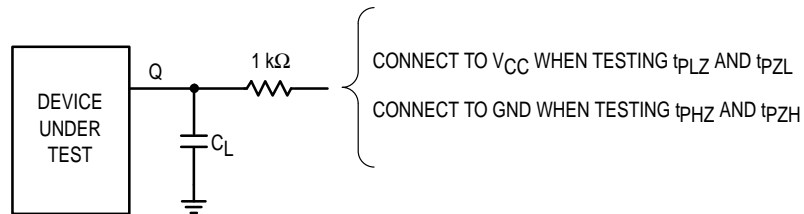
Figure 7. Test Circuit

LOGIC DIAGRAM

R1$_A$ 14 R0$_A$ 13 R1$_B$ 10 R0$_B$ 11 $\overline{\text{3–STATE A}}$ 3

CLOCK 16
WE 15

C Q / D $\overline{Q}$ (×4)

Q3$_A$ 7
Q2$_A$ 6
Q1$_A$ 5
Q0$_A$ 4
Q3$_B$ 1
Q2$_B$ 2
Q1$_B$ 23
Q0$_B$ 22

D3 17 — C D Q
D2 18 — C D Q
D1 19 — C D Q
D0 20 — C D Q

W1 9 — C D Q $\overline{Q}$
W0 8 — C D Q $\overline{Q}$

21
$\overline{\text{3–STATE B}}$
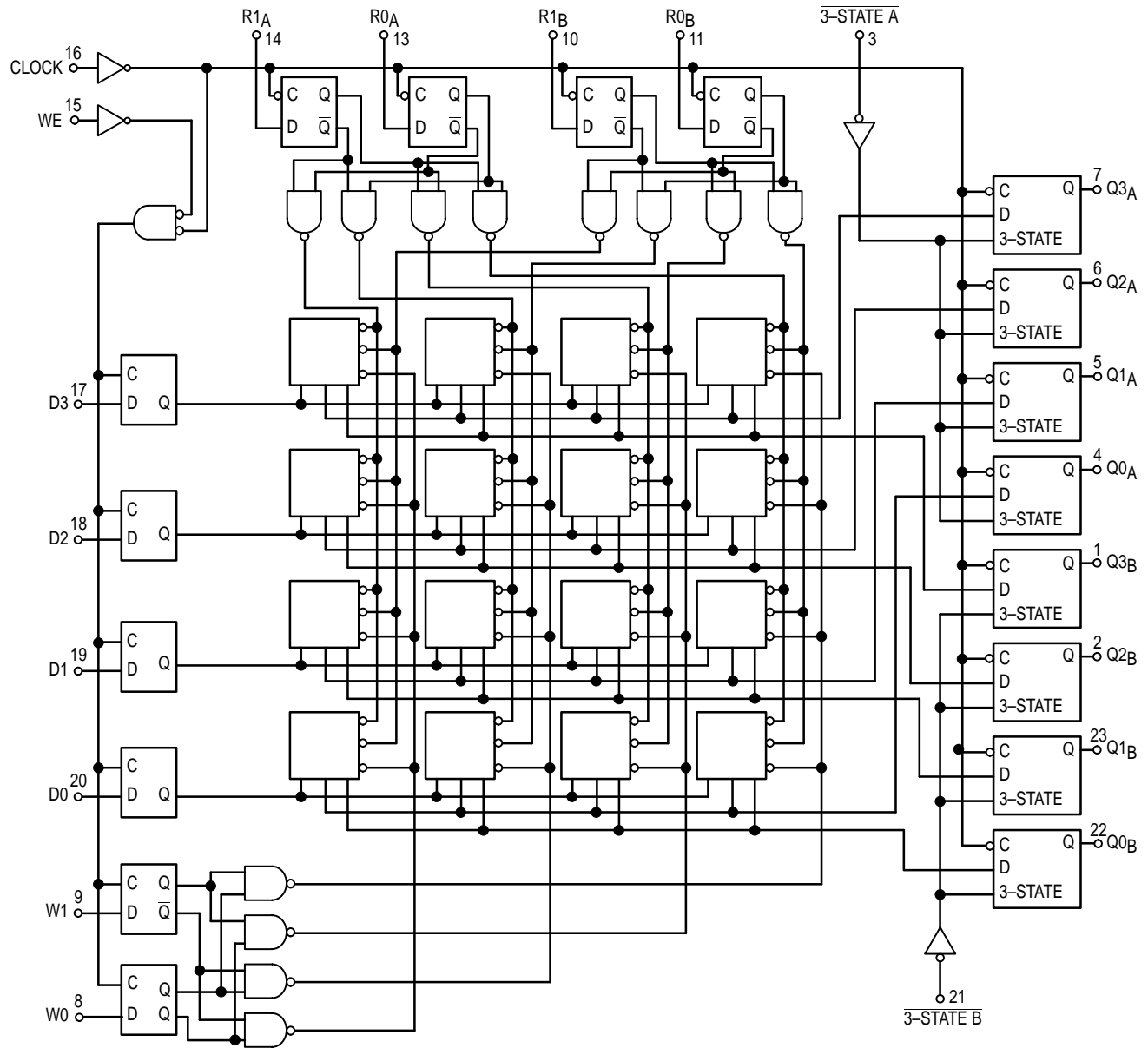
TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1$_A$	Read 0$_A$	Read 1$_B$	Read 0$_B$	3–State A	3–State B	D$_n$	Q$_n$A	Q$_n$B
⌐	1	0	1	0	1	0	1	1	1	1	1	1
⌐	1	0	1	0	1	0	1	1	1	0	0	0
⌐	X	X	X	X	X	X	X	1	1	X	No Change	No Change
X	X	X	X	X	X	X	X	0	0	X	Z	Z
0	X	X	X	X	X	X	X	1	1	X	No Change	No Change
1	X	X	X	X	X	X	X	1	1	X	No Change	No Change
⌐	1	0	0	0	1	1	0	1	1	D$_n$ to word 0	Contents of word 1 displayed	Contents of word 2 displayed
⌐	0	0	0	0	1	1	0	1	1	Word 0 not altered	Contents of word 1 displayed	Contents of word 2 displayed

Z = High Impedance
X = Don't Care

MOTOROLA CMOS LOGIC DATA　　　　　　　　　　　　　　**MC14580B**

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OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
CASE 623–05
ISSUE M
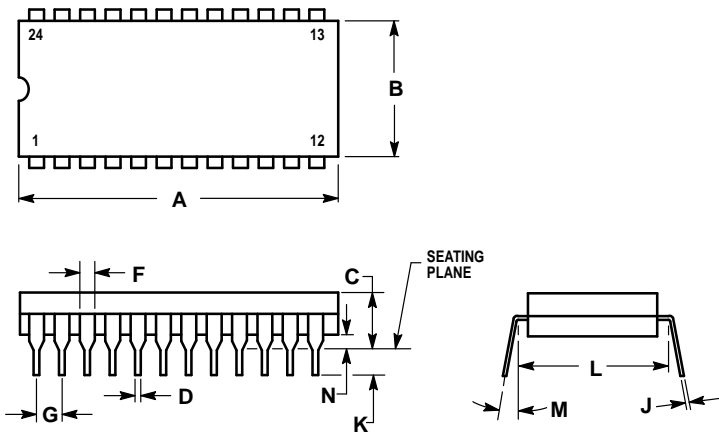
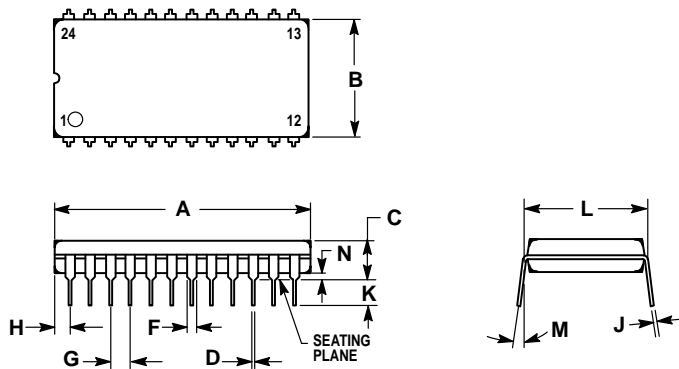
NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

P SUFFIX
PLASTIC DIP PACKAGE
CASE 709–02
ISSUE C

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E
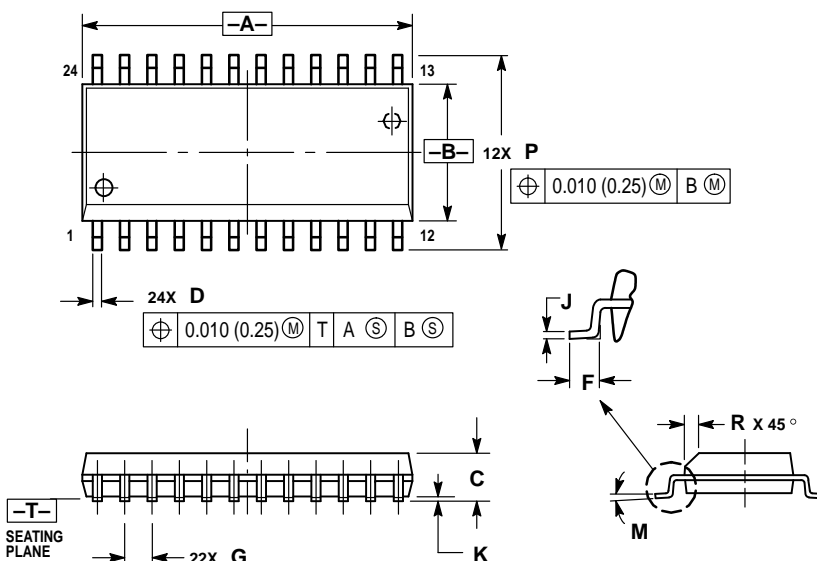
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

MOTOROLA

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MC14580B/D