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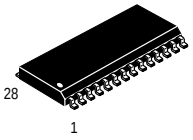
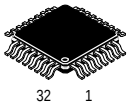
MC145574

Technical Summary

ISDN S/T Interface Transceiver



DW SUFFIX
SOG PACKAGE
CASE 751F



PB SUFFIX
TQFP
CASE 873A

ORDERING INFORMATION

MC145574DW	SOG Package
MC145574PB	TQFP

This technical summary provides an overview of the MC145574 S/T interface transceiver. A complete data booklet with comprehensive technical information is available and can be ordered through your Motorola Sales Office.

The MC145574 is Motorola's second generation S/T transceiver and is a follow–on to the MC145474/75 transceiver. It is intended to provide the improved interfacing capabilities and reduced power consumption required by today's ISDN applications while maintaining the functionality and extended range performance of the MC145474/75.

The MC145574 provides an economical VLSI layer 1 interface for the transportation of two 64 kbps B channels and one 16 kbps D channel between the network termination (NT) and terminal equipment applications (TEs). The MC145574 conforms to CCITT I.430 and ANSI T1.605 specifications. The MC145574 provides the modulation/line drive and demodulation/line receive functions required of the interface. In addition, the MC145574 provides the activation/deactivation, error monitoring, framing, bit, and octet timing. The MC145574 provides the control signals for the interface to the layer 2 devices. Complete multiframe capability is provided.

The MC145574 features the interchip digital link (IDL2) for the exchange of the 2B+D channel information between ISDN components and systems. The MC145574 provides an industry standard serial control port (SCP) to program the operation of the transceiver. As an alternative to IDL+SCP combination, the general circuit interface (GCI) is provided.

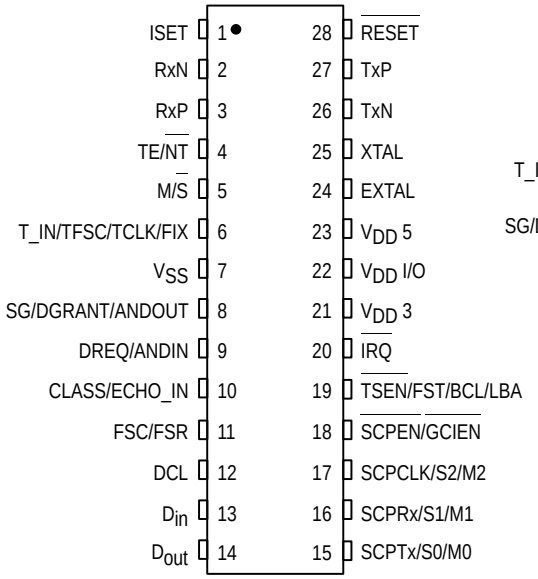
The MC145574 is not pin compatible with the MC145474/75 but it is intended to have a compatible register set and be fully compatible with current application software; however, to make full use of the additional MC145574 features software, modifications will be required.

- Three Selectable Resolutions: 320 (CGA), 480 (EGA), or 640 (VGA) Dots per Line
- Conforms to CCITT I.430, ETSI ETS 300012, and ANSI T1.605 Specifications
- Register/Software Compatible with the First Generation MC145474/75
- Pin Selectable NT or TE Modes of Operation
- Incorporates the IDL2, with Timeslot Assigner
- Industry Standard Microprocessor SCP
- Features GCI Interface
- Uses 2.5:1 Transformers for Transmit and Receive
- Exceeds the Recommended Range of Operation in all Configurations
- Complete Multiframing Capability Supported (SC1 – SC5 and Q Channel)
- Optional B Channel Idle, Invert, or Exchange
- Supports Full Range of S/T and IDL Loop–Backs
- Supports Transmit Power Down, Listening, and Absolute Minimum Power Mode
- Supports Crystal or External Clock Input Mode
- NT Star and NT Terminal Modes Supported
- Low Power Consumption
- Compatible with 3 V Devices

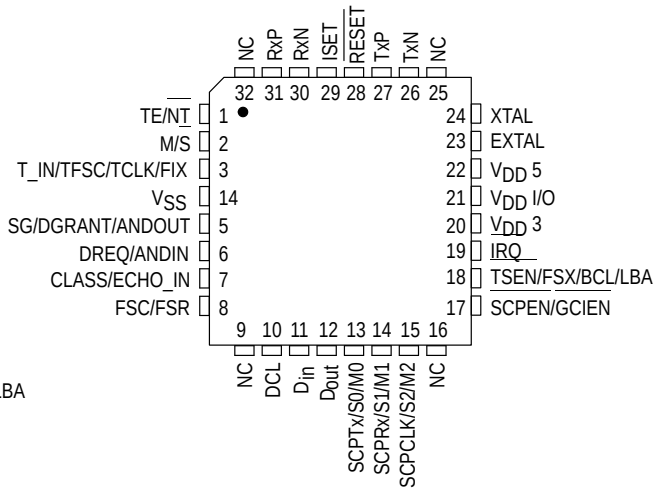
REV 2.1
7/96

PIN ASSIGNMENTS

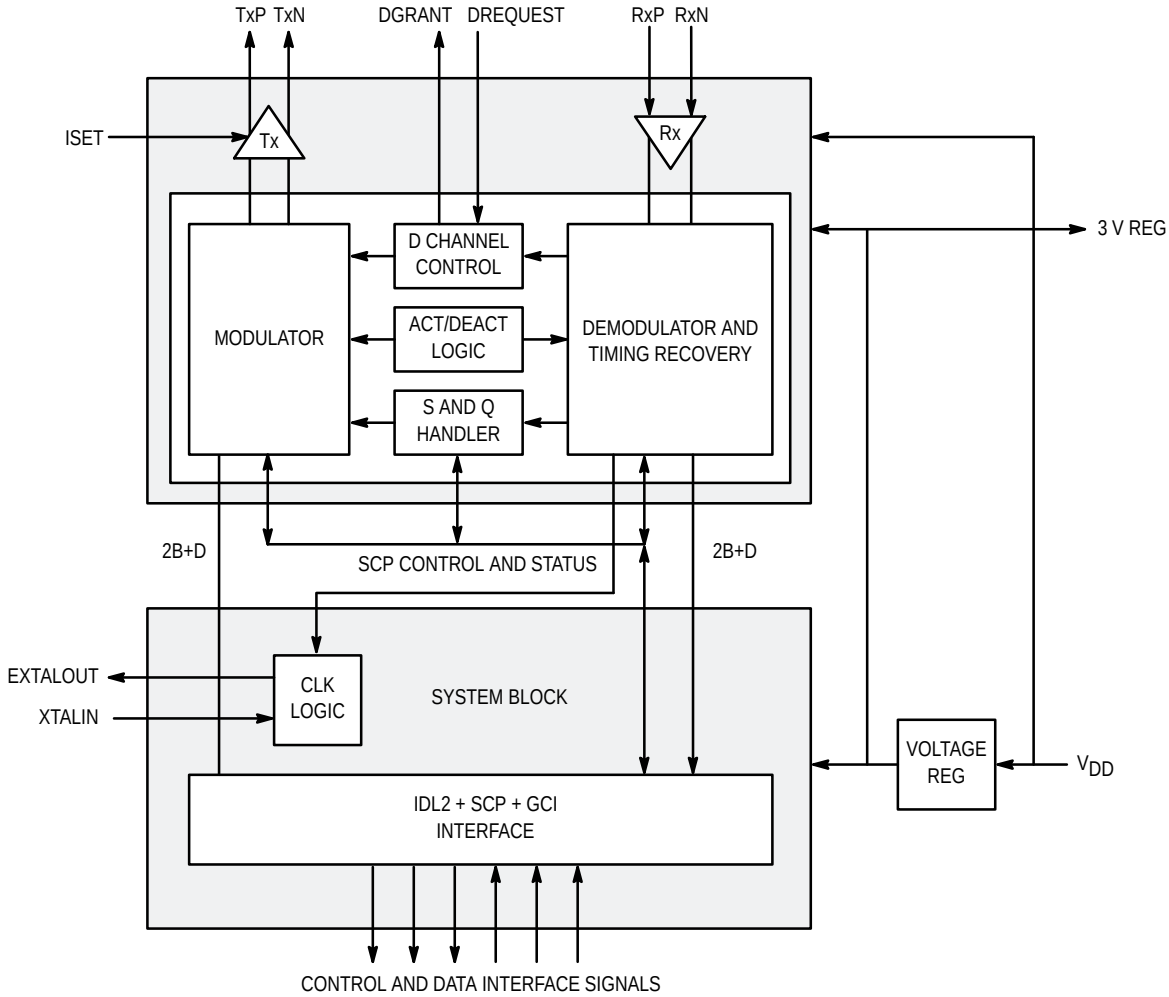
28–LEAD SOIC



32–LEAD TQFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD} 5	Supply Voltage	– 0.5 to + 7	V
V_{in}	Input Voltage (Any Pin to V_{SS})	– 0.3 to V_{DD} 5 + 0.3	V
I	DC Current (Any Pin Excluding V_{DD} 5, V_{DD}IO, V_{DD} 3, V_{SS}, TxP, and TxN)	± 10	mA
T_A	Operating Temperature Range	– 40 to + 85	°C
T_{stg}	Storage Temperature Range	– 85 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

DIGITAL DC ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C, V_{DD} 5 = 5.0 V ± 5%, Voltages referenced to V_{SS})

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	—	V
Input Low Voltage	V_{IL}	—	0.8	V
Input Leakage Current @ 5.25 V	I_{in}	—	5	µA
High Impedance Input Current @ 4.5/0.5 V	Ilkg(Z)	—	10	µA
Input Capacitance	C_{in}	—	10	pF
Output High Voltage (I_{OH} = – 400 µA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 5.0 mA)	V_{OL}	—	0.4	V
XTAL Input High level	$V_{IH(X)}$	3.0	—	V
XTAL Input Low level	$V_{IL(X)}$	—	0.5	V
EXTAL Output Current (V_{OH} = 4.6 V)	$I_{OH(X)}$	—	– 400	µA
EXTAL Output Current (V_{OL} = 0.4 V)	$I_{OL(X)}$	—	400	µA
IRQ Output Low Current (V_{OL} = 0.4 V)		—	2	mA
IRQ Output Off State Impedance		100	—	kΩ

ANALOG CHARACTERISTICS (T_A = – 40 to + 85°C, V_{DD} 5 = 5.0 V ± 5%, Voltages referenced to V_{SS})

Characteristic	Min	Typ	Max	Unit
TxP/TxN Drive Current: R_L = 50 Ω	5.4	6.0	6.6	mA
(TxP – TxN) Voltage Limit	—	—	1.17	Vpeak
Rx Input Sensitivity, Normal Mode (RxP – RxN)	90	—	—	mVpeak
Rx Input Sensitivity, Sleep Mode (RxP – RxN)	220	—	—	mVpeak
Voltage Regulator	3.0	3.2	3.4	V

POWER DISSIPATION (T_A = – 40 to + 85°C, V_{DD} 5 = 5.0 V ± 5%, Voltages referenced to V_{SS} and V_{DD}IO connected to V_{DD} 5)

Characteristic	Min	Typ	Max	Unit
DC Supply Voltage	4.75	5	5.25	V
Worst Case Power Consumption**	—	60*	90	mW
Transmit Power Down	—	50*	70	mW
Sleep Mode	—	0.5*	4	mW
Absolute Minimum Power Down	—	0.1*	2	mW

* These values have been measured on some sampled devices from several lots at 25° C and V_{DD} = 5 V.

** While sending and receiving 96 kHz signal on S/T interface.

IDL TIMING CHARACTERISTICS (IDL SLAVE) (T_A = – 40 to + 85°C, V_{DD} 5 = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive FSRs	Note 1		
2	FSR Active After DCL Falling Edge (Hold Time)	30	—	ns
3	FSR Active Before DCL Falling Edge (Setup Time)	30	—	ns
4	DCL Period	Note 2		
5	DCL Width High	45	55	% of DCL Period
6	DCL Width Low	45	55	% of DCL Period
7	D_{in} Valid Before DCL Falling Edge (Setup Time)	30	—	ns
8	D_{in} Valid After DCL Falling Edge (Hold Time)	30	—	ns
9	D_{out} Time to High–Impedance	—	35	ns
10	D_{out} High–Impedance to Active State	—	70	ns
11	DCL to D_{out} Active	—	70	ns

NOTES:
1. FSR is an 8 kHz signal.
2. DCL input frequency can be run from 512 kHz to 4.096 MHz.

IDL TIMING CHARACTERISTICS (IDL MASTER WITH THE IDL DCL RATE SET TO 2.56 MHz)
(T_A = – 40 to + 85°C, V_{DD} 5 = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive FSRs	Note 1		
2	FSR Active After DCL Falling Edge (Hold Time)	160	230	ns
3	FSR Active Before IDL DCL Falling Edge (Setup Time)	160	230	ns
4	DCL Period	Note 2		
5	DCL Width High	Note 2		
6	DCL Width Low	Note 2		
7	D_{in} Valid Before DCL Falling Edge (Setup Time)	30	—	ns
8	D_{in} Valid After DCL Falling Edge (Hold Time)	30	—	ns
9	D_{out} Time to High Impedance	0	35	ns
10	D_{out} High–Impedance to Active State	—	45	ns
11	DCL to D_{out} Active	—	45	ns

NOTES:
1. FSR is an 8 kHz signal.
2. DCL output frequency can be programmed at 512 kHz, 1.536 MHz, 2.048 MHz, or 2.56 MHz.

SCP TIMING CHARACTERISTICS (T_A = – 40 to + 85°C, V_{DD} 5 = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
12	SCP EN Active Before Rising Edge of SCP CLK	50	—	ns
13	SCP Rising Edge Before SCP EN Active	50	—	ns
14	SCP Rx Valid Before SCP CLK Rising Edge (Setup Time)	20	—	ns
15	SCP Rx Valid After SCP CLK Rising Edge (Hold Time)	20	—	ns
16	SCP CLK Period (Note 1)	244	—	ns
17	SCP CLK Width (Low)	30	—	ns
18	SCP CLK Width (High)	30	—	ns
19	SCP Tx Active Delay	—	50	ns
20	SCP EN Active to SCP Tx Active	—	50	ns
21	SCP CLK Falling Edge to SCP Tx High Impedance	—	40	ns
22	SCP EN Inactive Before SCP CLK Rising Edge	50	—	ns
23	SCP CLK Rising Edge Before SCP EN Inactive	50	—	ns
24	SCP CLK Falling Edge to SCP Tx Valid Data	—	50	ns

NOTE:
1. Maximum SCP Clock Frequency is 4.096 MHz.

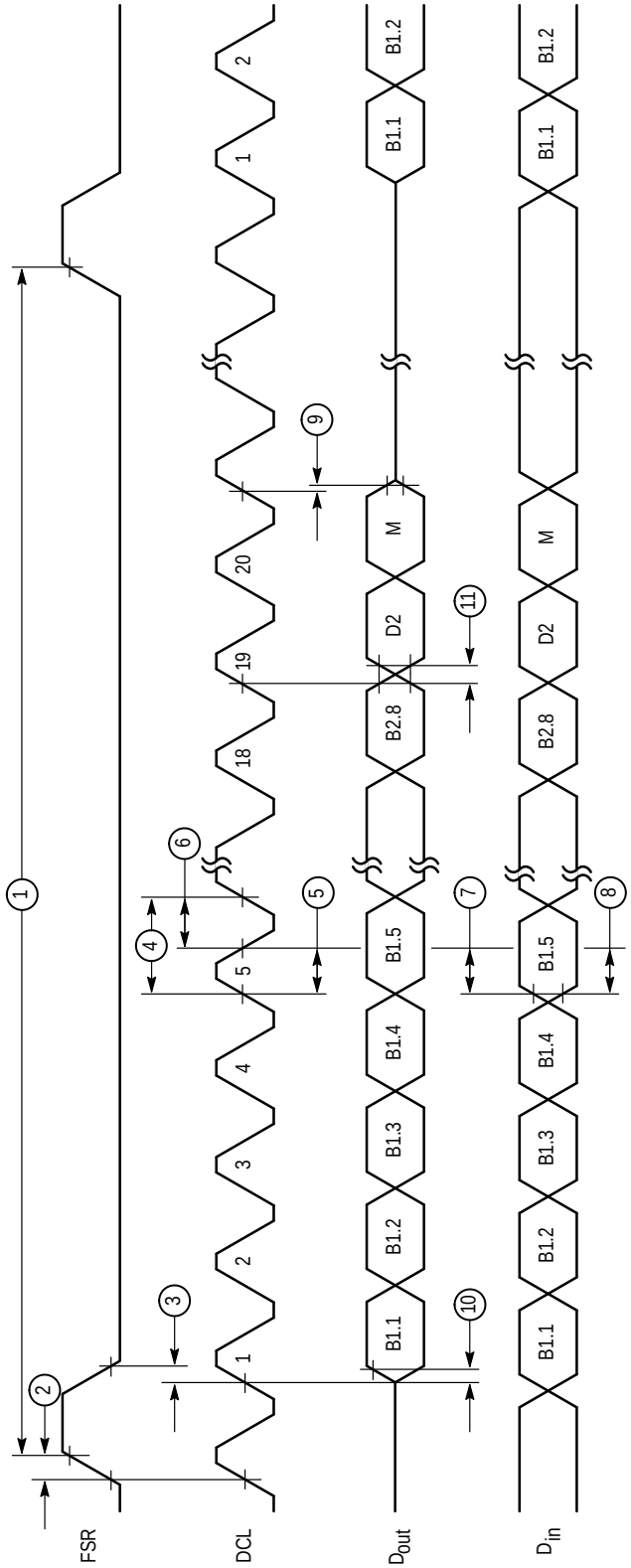
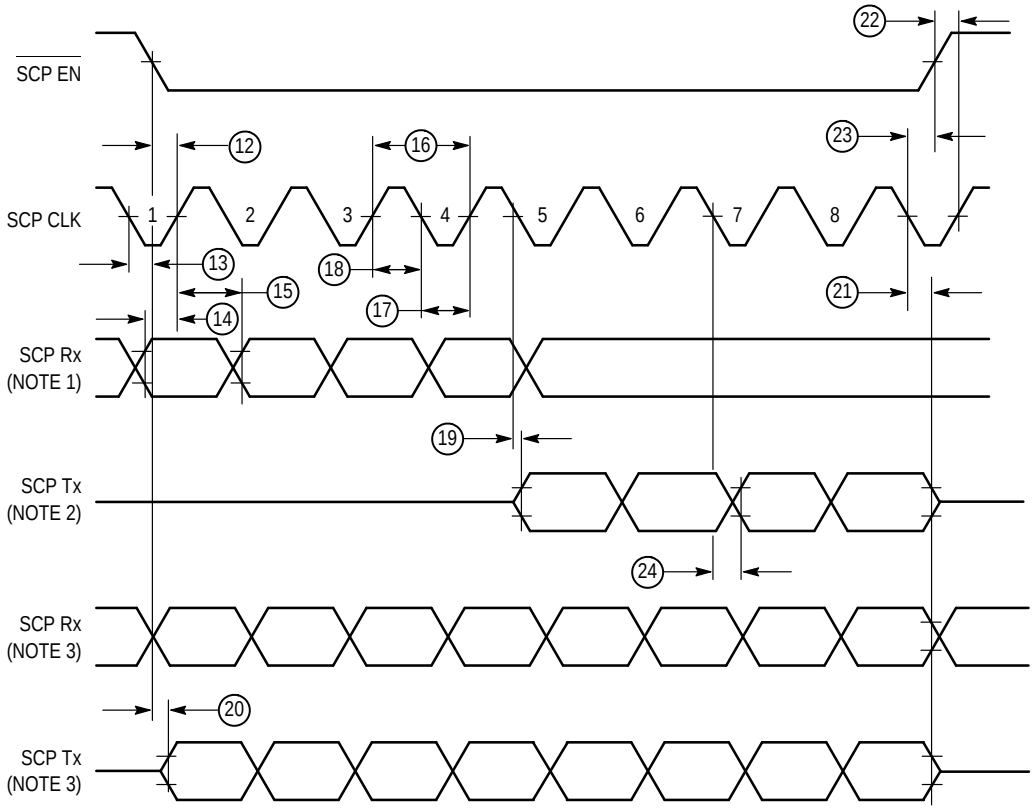


Figure 1. IDL Timing Characteristics



NOTES:

1. During a nibble read, four bits are presented on SCP Rx.
2. During a nibble read, SCP Tx will be active for the duration of the 4–bit transmission as shown.
3. During a byte read, eight bits are presented on SCP Rx. A byte transaction consists of two 8–bit exchanges. During the second 8–bit exchange, data is either written to the byte from SCP Rx or is read from the byte. If the operation is a read operation, then data is presented onto SCP Tx. Refer to “The Serial Control Port” section for a detailed description.

Figure 2. SCP Timing Characteristics

GCI TIMING CHARACTERISTICS (GCI SLAVE) (T_A = – 40 to + 85°C, V_{DD} 5 = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive FSCs	Note 1		
2	FSC Active After DCL Falling Edge (Hold Time)	30	—	ns
3	FSC Active Before DCL Falling Edge (Setup Time)	70	—	ns
4	DCL Period	Note 2		
5	DCL Width High	45	55	% of DCL Period
6	DCL Width Low	45	55	% of DCL Period
7	D_{in} Valid Before DCL Falling Edge (Setup Time)	30	—	ns
8	D_{in} Valid After DCL Falling Edge (Hold Time)	50	—	ns
11	DCL to D_{out} Active	—	70	ns

NOTES:
1. FSC is an 8 kHz signal.
2. DCL input frequency can be run from 512 kHz to 4.096 MHz.

GCI TIMING CHARACTERISTICS (GCI MASTER WITH THE GCI DCL RATE SET TO 2.048 MHz)
(T_A = – 40 to + 85°C, V_{DD} 5 = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive FSCs	Note 1		
2	FSC Active After DCL Falling Edge (Hold Time)	210	280	ns
3	FSC Active Before DCL Falling Edge (Setup Time)	210	280	ns
4	DCL Period	Note 2		
5	DCL Width High	Note 2		
6	DCL Width Low	Note 2		
7	D_{in} Valid Before DCL Falling Edge (Setup Time)	30	—	ns
8	D_{in} Valid After DCL Falling Edge (Hold Time)	50	—	ns
11	DCL to D_{out} Active	—	70	ns

NOTES:
1. FSC is an 8 kHz signal.
2. DCL output frequency can be programmed at 512 kHz, 1.536 MHz, or 2.048 MHz.

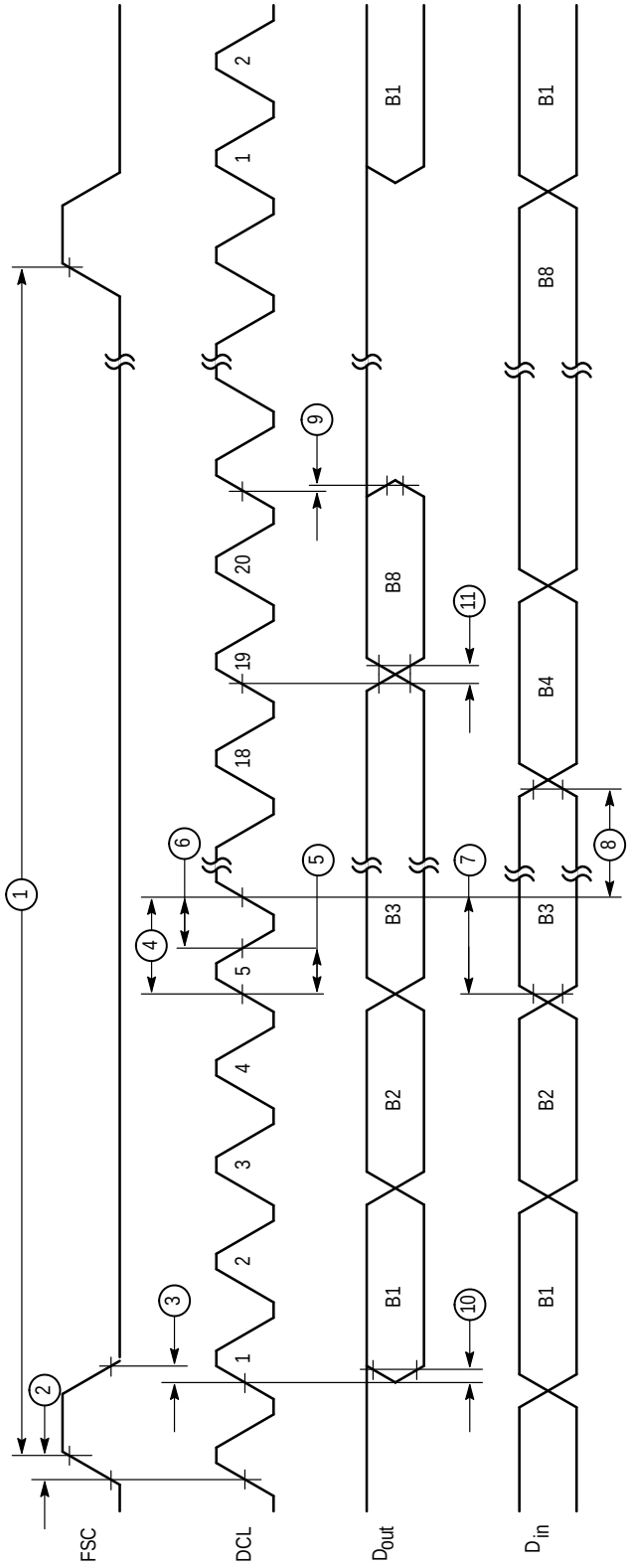


Figure 3. GCI Timing Characteristics

NT1 STAR MODE TIMING CHARACTERISTICS

NT1 STAR MODE OF OPERATION

A wiring configuration which may be used to support multiple T interfaces is known as the “NT1 Star Mode of Operation.” This mode of operation is supported by the MC145574. Note that the NT1 Star mode contains multiple NTs. Each of these NTs can be connected to either a passive bus (short, extended, or branched) or to a single TE.

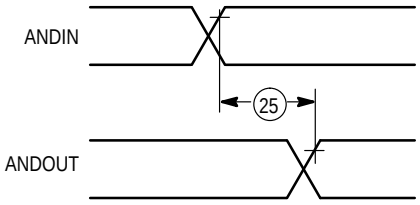


Figure 4. NT1 Star Mode

Table 1. D Channel Timing Characteristics (IDL Mode)

Reference Number	Characteristic	Min	Max	Unit
25	Propagation Delay from ANDIN to ANDOUT	—	35	ns
26	DREQUEST Valid Before Falling Edge of FSR	30	—	ns
27	DREQUEST Valid After Falling Edge of FSR	30	—	ns
28	DGRANT Valid Before Falling Edge of FSR	390	—	ns

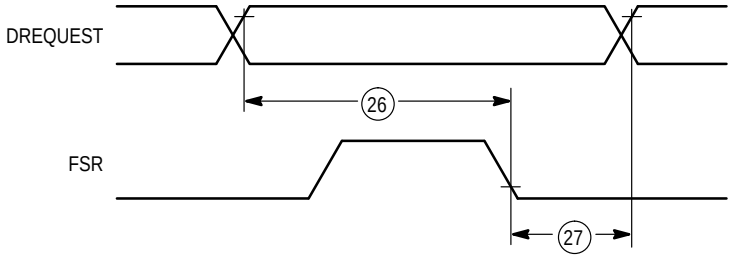


Figure 5. D Channel Request Timing

PIN DESCRIPTIONS

$V_{SS(A)}$ (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

ISET

This pin is used to program the current and should have an external resistor connected to ground. The resistor should have a value of 30 kΩ ± 5%.

RxN, RxP

These two pins form the differential receiver for the S/T Interface. They are connected to the S/T loop via a transformer.

TE/$\overline{NT}$

This pin allows the external selection of NT or TE mode. When this pin is held low NT mode is selected and when held high TE mode.

This pin is OR'd with an SCP register bit enabling TE/NT selection to be made in software.

M/$\overline{S}$

This pin allows the external selection of mode for the IDL and GCI interface. This pin functions in both NT and TE modes. When this pin is held low, SLAVE mode is selected and when held high, MASTER mode.

This pin is OR'd with an SCP register bit enabling MASTER/SLAVE selection to be made in software.

T_IN/TFSC/TCLK/FIX

This pin performs four functions dependent on the mode of operation. In all NT modes, except NT Terminal mode, this pin is the FIX input and enables the device to differentiate between fixed and adaptive timing modes. When this pin is held low, ADAPTIVE timing is selected and when held high, FIXED timing. This pin is OR'd with an SCP register bit enabling FIXED/ADAPTIVE selection to be made in software.

In the NT terminal mode this pin is the T_IN input. T_IN is an IDL input port that will accept B1, B2, and D Data. Please refer to the NT Terminal section for further details. In the NT Terminal mode, the FIX function is controlled via an SCP register bit.

In TE SLAVE mode this pin outputs TFSC. TFSC is an 8 kHz frame clock that is synchronized to the received S/T Interface and can be used as the synchronization source in the NT–2 slave–slave mode. Alternatively, this pin can output TCLK, selected via the SCP. TCLK is a clock, whose frequency can be chosen via the SCP, which is synchronized to the received S/T Interface. TCLK can be used as an alternative to TFSC in NT–2 slave–slave mode.

V_{SS}

This is the most negative power supply and digital logic ground. It is normally 0 V.

SG/DGRANT/ANDOUT

This pin performs three functions dependent on the mode of operation. In NT Star mode it is the ANDOUT output function for use in NT Star applications.

In the TE Master and NT Terminal modes, this pin is the DGRANT output function used for gaining D channel access.

In GCI TE Master, this pin is SG and indicates Stop/Go access to the D channel.

DREQ/ANDIN

This pin performs three functions dependent on the mode of operation. In NT Star mode, it is the ANDIN input function for use in NT Star applications.

In the TE Master and NT Terminal modes, this pin is the DREQUEST input used for requesting D channel access.

In all other modes, this input has no defined function and should be tied to V_{SS}.

CLASS/ECHO_IN

This pin performs two functions dependent on the mode of operation. In NT Star mode, it is the ECHO_IN input function for use in NT Star applications.

In the TE Master mode, this pin is the CLASS input used to determine the D channel access class.

In all other modes, this input has no defined function and should be tied to V_{SS}.

FSR/FSC

This pin is bidirectional, the direction depending on whether the device is to be a timing master or slave to the IDL/GCI interface. In either case, this pin should be driven with or drive an 8 kHz frame sync signal. In GCI mode this pin is called FSC. In IDL mode this pin is called FSR.

This pin is also the frame sync signal for the IDL receive direction (FSR) when independent frame sync's have been enabled via the SCP interface.

DCL

This pin is the clock pin for the IDL/GCI interface and will be either an input or an output depending on whether the interface is operating as a slave or a master.

D_{in}

This pin is the data input pin for the IDL/GCI.

D_{out}

This pin is the data output pin for the IDL/GCI.

SCPTx/S0/M0

This pin has three functions. It is the data output pin, SCPTx, in SCP mode. It is a time slot select input pin, S0, in GCI slave mode. It is a mode select pin, M0, in GCI master mode.

SCPRx/S1/M1

This pin has three functions. It is the data input pin, SCPRx, in SCP mode. In GCI slave mode it is a time slot select input pin, S1, and it is a mode select pin, M1, in GCI master mode

SCPCLK/S2/M2

This pin has three functions. It is the clock input pin, SCPCLK, in SCP mode. In GCI Slave mode, it is a time slot

select input pin, S2. In GCI Master mode, it is a mode select pin, M2.

SCPEN/GCIEN

This pin has two functions. It is the SCP enable pin, SCPEN, in SCP mode. In GCI mode, it is the GCI enable pin, GCIEN. Please refer to the section on GCI for details on how the device enters GCI mode.

TSEN/FSX/BCL/LBA

This pin is initially high impedance but can be programmed to have three separate functions. The TSEN signal is enabled via the SCP. This pin then becomes an open drain output that pulls low when data is being output from D_{out}. This signal can then be used to enable an external driver in applications where the IDL data goes off board, PBX's, etc.

In IDL mode it can also be used as the 8 kHz frame sync, FSX, for the transmit path. In this mode the pin is bidirectional, the direction depending on whether the device is an IDL master or slave. FSX only operates when dual frame sync mode has been enabled via the SCP.

In GCI mode this pin is an output clock, BCL. BCL is a bit rate clock that is half the frequency of the DCL clock and is synchronous with FSC. This clock can be used as the data clock for standard devices such as a codec.

LBA is the default function for both the IDL and GCI modes. This pin is initially an output, LBA, Loop–back Active. The LBA pin is normally low but when a loop–back is activated within the device, this pin will toggle transition to a high during the time that the loop–back is enabled. This pin can be redefined by writing to internal registers within the device.

IRQ

This pin is an open drain output that pulls low when the device wants to inform the µP that a status change has occurred. This pin returns to high impedance after clearing the interrupt condition via the SCP.

V_{DD} 3

This pin is the 3 V regulated supply output used to power the internal digital circuitry.

V_{DD} IO

This is the positive supply pin for the output drivers. This pin should be connected to V_{DD} if 5 V drivers are required or the 3 V regulator output, V_{DD} 3, if 3 V drivers are required. For further information, refer to the section on Power Supply Strategy.

V_{DD} 5

This is the positive supply pin and is normally 5 V ± 5%.

This pin should have a capacitor of 100 nF connected to ground. For further information refer to section on Power Supply Strategy.

EXTAL

This pin should be connected to the external 15.36 MHz crystal using the circuit defined in the T1 specification.

XTAL

This pin should be connected to an external 15.36 MHz crystal using the circuit defined in the T1 specification or alternatively, it can be driven by a 15.36 MHz clock source.

TxN, TxP

These two pins form a differential output driver that will connect to the S/T interface via a transformer.

RESET

This pin is always an input and is the reset pin for the device and is active low. When this pin is held low, a hardware reset is applied and the device is held in the deactivated state. At the initial application of power, the T2 should be reset. This pin is a Schmitt–trigger input and could have an external RC circuit connected to perform the power on reset function.

ADDITIONAL NOTES

Input Levels

The MC145574 S/T transceiver is always TTL/CMOS level compatible on all digital input pins.

SCP HIDOM

The MC145574 S/T transceiver has the capability of forcing all outputs (both analog and digital) to the high impedance state. This feature, known as the "serial control port high impedance digital output mode," is provided to allow "in circuit" testing of other circuits or devices resident on the same PCB without requiring the removal of the MC145574.

The SCP HIDOM mode is entered by holding SCPEN low for a minimum of 33 consecutive rising edges of the SCP CLK while SCP Rx is high. If SCPEN goes high, or if SCP Rx goes low, the device will exit the SCP HIDOM mode and return to normal operation.

WIRING CONFIGURATIONS

INTRODUCTION

The MC145574 ISDN S/T transceiver conforms to CCITT I.430 and ANSI T1.605 specifications. It is a layer 1 S/T transceiver designed for use at the S and T reference points. It is designed for both point–to–point and multipoint operation. The S/T transceiver is designed for use in either the network terminating (NT) mode or in terminal endpoint (TE) applications. Two 64 kbps B channels and one 16 kbps D channel are transmitted in a full duplex fashion across the interface.

The configurations described in this document are deemed to be the most common, but by no means the only wiring configurations. Note that when operating in the TE mode, only one TE has the 100 Ω termination resistors in the transmit and receive paths. Figures 6 through 9 illustrate where to connect the termination resistors for the described loop configurations.

A description of the most commonly used loop configurations is as described below.

POINT–TO–POINT OPERATION

In the point–to–point mode of operation one NT communicates with one TE. As such, 100 Ω termination resistors must

be connected across the transmit and receive paths of both the NT and TE transceivers. Figure 6 illustrates this wiring configuration.

When using the MC145574 in this configuration, the NT must be in adaptive timing. This is accomplished by holding the FIX pin low, i.e., connecting it to V_{SS}. CCITT I.430 and ANSI T1.605 specify that the S/T transceiver must be able to operate up to a distance of 1 km in the point–to–point mode. This is the distance D1 as shown in Figure 6.

SHORT PASSIVE BUS OPERATION

The short passive bus is intended for use when up to eight TEs are required to communicate with one NT. TEs can be distributed at any point along the passive bus, the only requirement being that the termination resistors be located at the end of the passive bus. Figure 7 illustrates this wiring configuration. CCITT I.430 and ANSI T1.605 specify a maximum operational distance from the NT of 200 meters. This corresponds to the distance D2 as shown in Figure 7.

EXTENDED PASSIVE BUS OPERATION

A wiring configuration whereby the TEs are restricted to a grouping at the far end of the cable, distant from the NT, is shown as the “Extended Passive Bus.” This configuration is as illustrated in Figure 8. The termination resistors are to be positioned as illustrated in the diagram.

The essence of this configuration is that a restriction is placed on the distance between the TEs. The distance D3 as illustrated in Figure 8 corresponds to the maximum distance between the grouping of TEs. CCITT I.430 and ANSI T1.605 specify a distance of 25 to 50 meters for the separation between the TEs, and a distance of 500 meters for the total length. These distances correspond to the distances D3 and D4 as shown in Figure 8.

Note that the “NT configured” MC145574 should be placed in the adaptive timing mode for this configuration. This is achieved by holding the FIX pin low.

BRANCHED PASSIVE BUS OPERATION

A wiring configuration which has somewhat similar characteristics to those of the “Extended Passive Bus” is known as the “Branched Passive Bus” and is illustrated in Figure 9. In this configuration, the branching occurs at the end of the bus. The branching occurs after a distance D1 from the NT. The distance D5 corresponds to the maximum separation between the TEs.

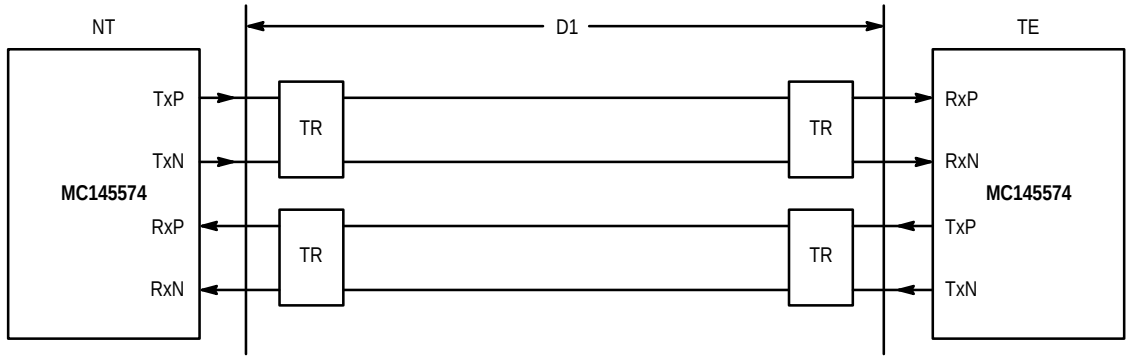


Figure 6. Point–to–Point

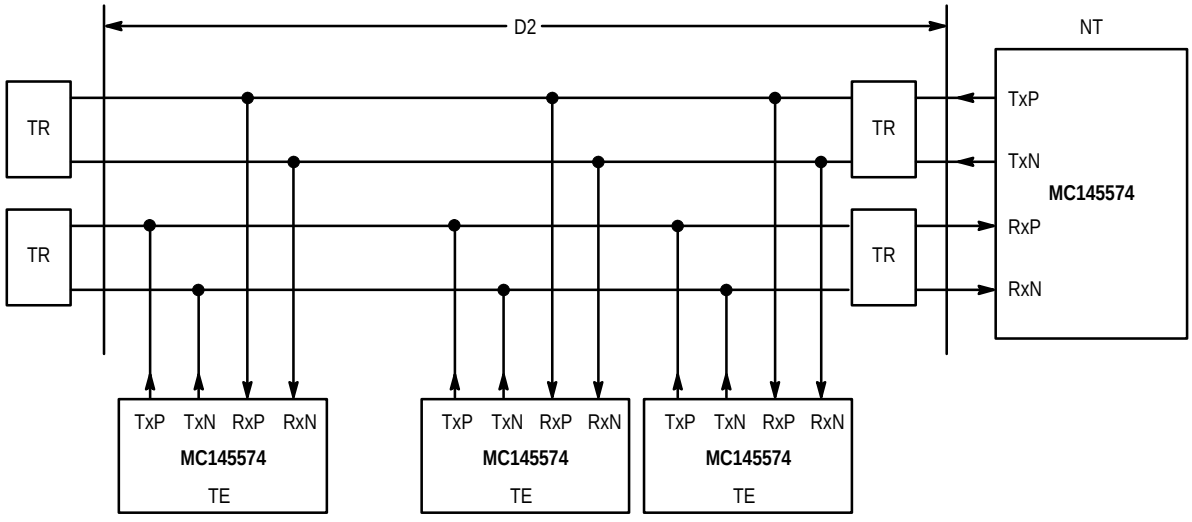


Figure 7. Short Passive Bus

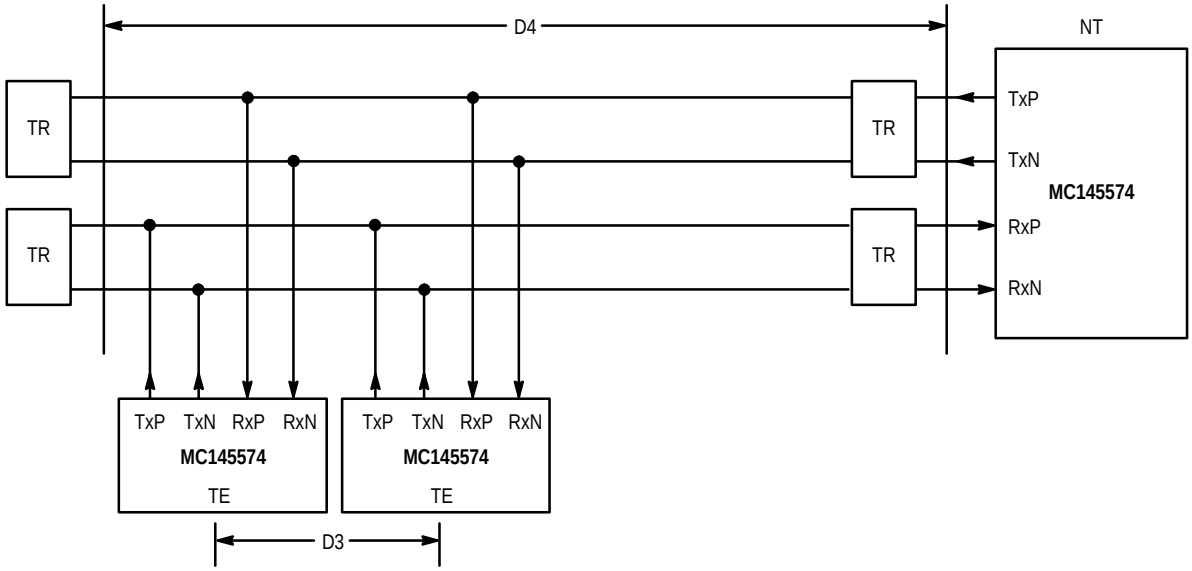


Figure 8. Extended Passive Bus

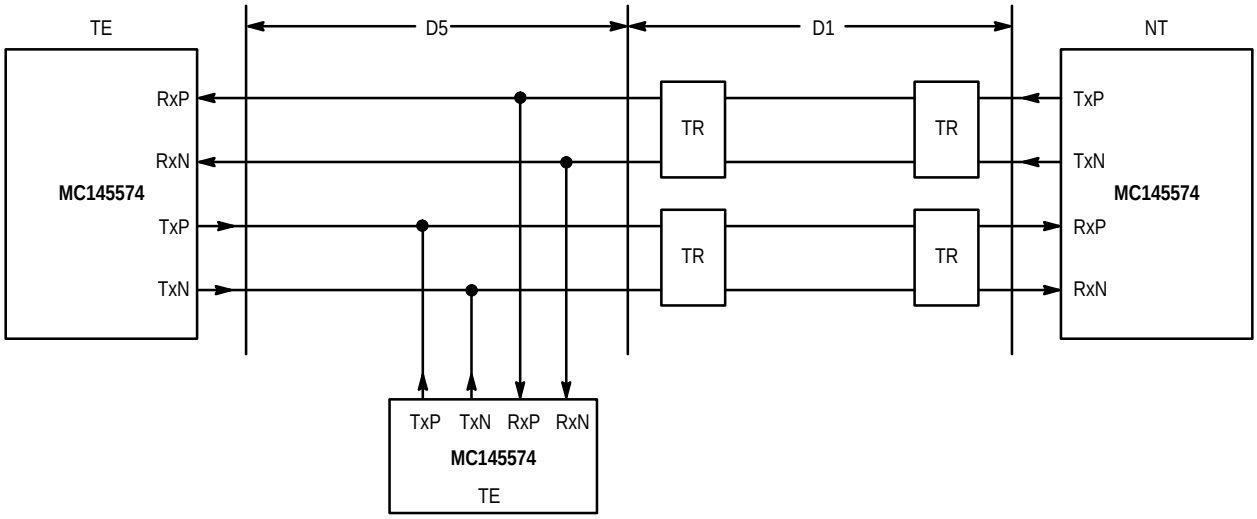


Figure 9. Branched Passive Bus

ACTIVATION/DEACTIVATION OF S/T TRANSCEIVER

INTRODUCTION

CCITT I.430 and ANSI T1.605 define five information states for the S/T transceiver. When the NT is in the fully operational state, it transmits INFO 4. When the TE is in the fully operational state, it transmits INFO 3. INFO 1 is transmitted by the TE when it wants to wake up the NT. INFO 2 is transmitted by the NT when it wants to wake up the TE, or in response to the TEs transmitted INFO 1. These states cause unique patterns of symbols to be transmitted over the S/T interface. Only when the S/T loop is in the fully activated state are the 2B+D channels of data transmitted over the interface.

ACTIVATION OF S/T LOOP BY NT

The NT activates the loop by transmitting INFO 2 to the TE or TEs. This is accomplished in the MC145574 by setting NR2(3) to a “1”. Note that this bit is internally reset to “0” after the internal activation state machine has recognized its active transition.

The TE and TEs, on receiving INFO 2, will synchronize to it and transmit back INFO 3 to the NT. The NT, on receiving INFO 3 from the TE, will respond with INFO 4, thus activating the loop.

ACTIVATION OF S/T LOOP BY TE

The TE can activate an inactive loop by transmitting INFO 1 to the NT. This is accomplished in the MC145574 by setting NR2(3) to a “1”. Note that this bit is internally reset to “0” after the internal activation state machine has recognized its active transition.

The NT, upon detecting INFO 1 from the TE, will respond with INFO 2. The TE, upon receiving a signal from the NT, will cease transmission of INFO 1, reverting to an INFO 0 state. After synchronizing to the received signal and having

fully verified that it is INFO 2, the TE will respond with INFO 3, thus activating the loop.

ACTIVATION PROCEDURES IGNORED

The MC145574 has the capability of being forced into the highest transmission state. This is accomplished by setting BR7(7) to a "1". Thus when this bit is set in the NT, it will force the NT to transmit INFO 4. Correspondingly, in the TE, setting this bit to "1" will force the TE to transmit INFO 3.

Note that CCITT I.430 and ANSI T1.605 specifications allow a TE to be activated by reception of INFO 4, without having to go through the intermediate handshaking. This is to allow for the situation where a TE is connected to an already active loop.

An NT, however, cannot be activated by a TE sending it INFO 3, without going through the intermediate INFO 1, INFO 2, INFO 3, and INFO 4 states.

This "Activation Procedures Ignored" feature is provided for test purposes, allowing the NT to forcibly activate the TE or TEs. In the TE, the forced transmission of INFO 3 enables verification of the TEs operation.

THE INTERCHIP DIGITAL LINK

INTRODUCTION

The Interchip Digital Link of the MC145574, IDL2, is backwards compatible with the IDL of the MC145474/75 S/T transceiver of first generation. But in addition to the standard operating mode, this enhanced interface features some new modes that are programmable through the SCP.

The IDL2 is a four–wire interface used for full–duplex communication between ICs on the board–level. The interface consists of a transmit path, a receive path, an associated clock, and a sync signal. These signals are known as D_{out}, D_{in}, DCL, and FSR, respectively. The clock determines the rate of exchange of data in both the transmit and receive directions, and the sync signal controls when this exchange is to take place. Three channels of data are exchanged every 8 kHz. These channels consist of two 64 kbps B channels and one 16 kbps D channel used for full duplex communication between the NT and TE.

There are two modes of operation for an IDL device: IDL master and IDL slave. If an IDL device is configured as an IDL master, then FSR and DCL are outputs from the device. Conversely, if an IDL device is configured as an IDL slave, then FSR and DCL are inputs to the device. Ordinarily the MC145574 should be configured as an IDL slave when acting as an NT, and as an IDL master when acting as a TE. The exception to this rule is the option to configure the NT as an IDL master. The TE configured MC145574 also features the new option of operating in IDL slave mode.

THE SERIAL CONTROL PORT

The MC145574 is equipped with a serial control port (SCP). This SCP is used by external devices (such as an MC145488 DDLC) to communicate with the S/T transceiver. The SCP is an industry standard serial control port and is compatible with Motorola's SPI used on several single–chip MCUs.

The SCP is a five–wire bus with control and status bits, data being passed to and from the S/T transceiver in a full–duplex fashion, and an indicator of the interrupt status register.

The SCP interface consists of a transmit path, a receive path, an associated clock, an enable signal, and an interrupt indicate. These signals are known as SCPTx, SCPRx, SCPCLK, SCPEN, and IRQ.

The clock determines the rate of exchange of data in both the transmit and receive directions, the enable signal governs when this exchange is to take place, and the interrupt signal indicates that an interrupt condition exists and a read operation of the interrupt status register, NR3, is required.

The operation/configuration of the S/T transceiver is programmed by setting the state of the control bits within the S/T transceiver. The control, status, and data information reside in eight 4–bit wide nibble registers, sixteen 8–bit wide byte registers, and sixteen 8–bit wide overlay registers. The nibble registers are accessed via an 8–bit SCP bus transaction. The 16–byte wide registers are accessed by first writing to a pointer register within the eight 4–bit wide nibble registers. This pointer register (NR(7)) will then contain the address of the byte wide register to be read from or written to, on the following SCP transaction. Thus, an SCP byte access is in essence a 16–bit operation. Note that this 16–bit operation can take place by means of two 8–bit accesses or a single 16–bit access.

SCP TRANSACTIONS

There are six types of SCP transactions. These are:

1. SCP nibble read.
2. SCP nibble write.
3. SCP byte read.
4. SCP byte write.
5. SCP merged read.
6. SCP merged write.

SCP Nibble Read

A nibble read is an 8–bit SCP transaction. Figure 10 illustrates this process. To initiate an SCP nibble read the SCPEN pin must be brought low. Following this, a Read/Write (R/W) bit followed by three primary address bits (A0 – A3), are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK, following the high to low transition of SCPEN. If a read operation is to be performed, then R/W should be a "1". The three address bits clocked in after the R/W bit select which nibble register is to be read. The contents of this nibble register are shifted out on SCPTx on the subsequent four falling edges of SCPCLK, i.e., the four falling edges of SCPCLK after the rising edge of SCPCLK which clocked in the last address bit (LSB). SCPEN should be brought back high after the transaction, before another falling edge of SCPCLK is encountered. Note that SCP Rx is ignored during the time that SCPTx is being driven. Also note that SCPTx comes out of high impedance only when it is transmitting data.

SCP Nibble Write

A nibble write is an eight bit SCP transaction. To initiate an SCP nibble write the SCPEN pin must be brought low. Following this, a R/W bit followed by three primary address bits are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK following the high to

low transition of SCPEN. If a write operation is to be performed then R/W should be a “0”. The three address bits clocked in after the R/W bit select the nibble register to be written to. The data shifted in on the next four rising edges of SCPCLK is then written to the selected register. Throughout this whole operation the SCPTx pin remains in high–impedance state. Note that if a selected register or bit in a selected register is “read only” then a write operation has no effect.

SCP Byte Read

A byte read is a 16–bit SCP transaction. To initiate an SCP byte read, the SCPEN must be brought low. Following this, an R/W bit is shifted in from SCPRx on the next rising edge of SCPCLK. This bit determines the operation to be performed, read or write.

If R/W is a “1” then a read operation is selected. Conversely, if R/W is a “0” then a write operation is selected. The next three bits shifted in from SCPRx on the three subsequent rising edges of SCPCLK are primary address bits as mentioned previously. If all three bits are “1” then nibble register 7 is selected (NR7). This is a pointer register, selection of which informs the device that a byte operation is to be performed. When NR7 is selected, the following four bits shifted in from SCP Rx on the following four rising edges of SCPCLK are automatically written to NR7. These four bits are the address bits for the byte operation. In a read operation, the next eight falling edges of SCPCLK will shift out the data from the selected byte register on SCPTx.

As mentioned previously, an SCP byte access is a 16–bit transaction. This can take place in one 16–bit exchange or two 8–bit exchanges. If the transaction is performed in two 8–bit exchanges the SCPEN should be returned high after the first eight bits have been shifted into the part.

When SCPEN comes low again, the MSB of the selected byte will present itself on SCPTx. The following seven falling edges of SCPCLK will shift out the remaining seven bits of the byte register. Note that the order in which data is written into the part and read out of the part is independent of whether the byte access is done in one 16–bit exchange or in two 8–bit exchanges.

SCP Byte Write

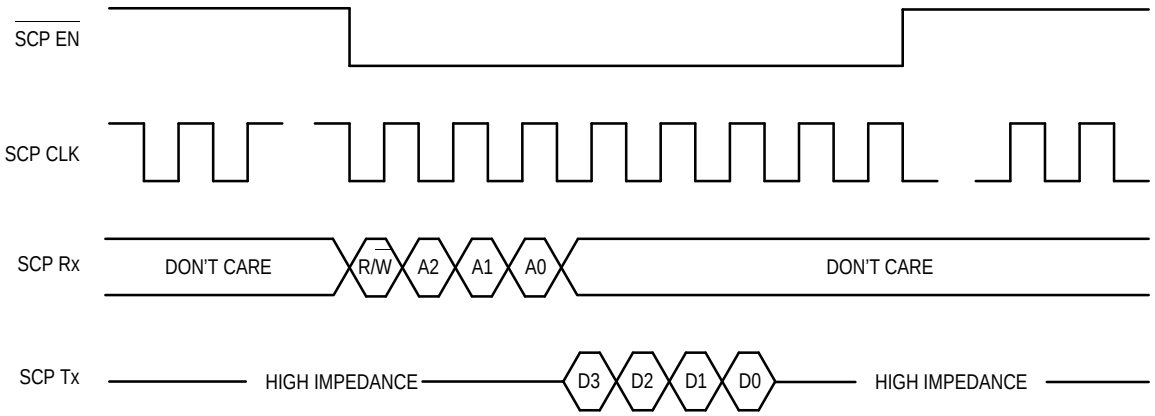
A byte write is also a 16–bit SCP transaction. To initiate an SCP byte write the SCP EN must be brought low. As before, the next bit determines whether the operation is to be read or write. If the first bit is a “0” then a write operation is selected. Again, the next three bits read in from SCP Rx on the subsequent three rising edges of SCPCLK must all be “1” in order to select the pointer nibble register (NR7). The following four bits shifted in are automatically written into NR7. As in an SCP byte read, these bits are the address bits for the selected byte register operation. The next eight rising edges of SCPCLK shift in the data from the SCPRx. This data is then stored in the selected byte register. Throughout this operation SCPTx will be in a high–impedance state. Note that if the selected byte is “read only,” then this operation will have no effect.

As mentioned previously, an SCP byte access is a 16–bit transaction. This can take place in one 16–bit exchange or two 8–bit exchanges. If the transaction is performed in two 8–bit exchanges, then SCPEN should be returned high after the first eight bits have been shifted into the part.

When SCPEN comes low again, the next eight rising edges of SCPCLK shift data in from SCPRx. This data is then stored in the selected byte.

SCP Merged Read/Write

Merged operations are accomplished by not taking SCPEN high between separate SCP instructions. The SCP bytes/nibbles are strung together in a continuous bit stream and can be a mux or read/write command. The device is able to extract the separate instructions and provide the appropriate response. The SCPEN signal goes low at the start of the bit stream and goes high again at the end. SCPCLK should only be active during valid bit times while SCPEN is low.



NOTES:
1. R/W = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCP CLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCP CLK, MSB first.

Figure 10. Serial Control Port Nibble Read Operation

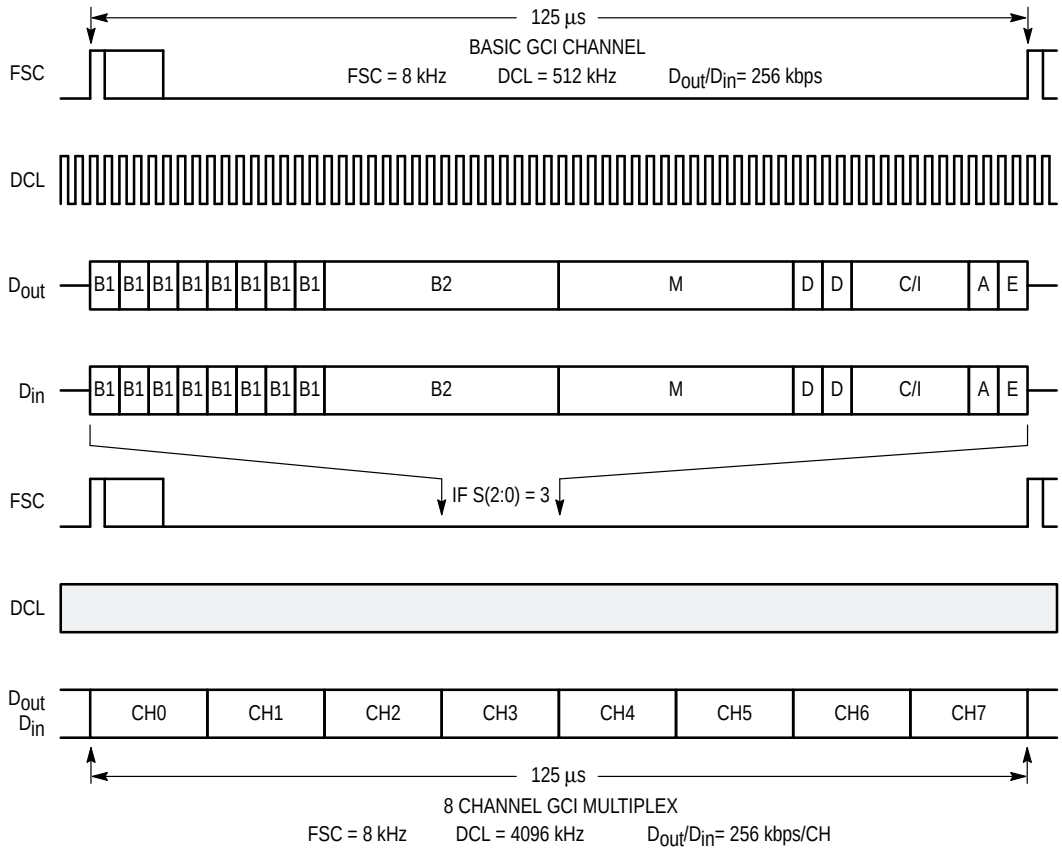


Figure 11.

GENERAL CIRCUIT INTERFACE

The MC145574 is able to work with a general circuit interface port (GCI). This GCI is a standard four–wire interface between devices for the subscriber access in ISDN and analog environments. The principle use, in the these applications, is to control the subscriber line interface circuitry.

Some of the benefits of the General Circuit Interface are:

- Operation and maintenance features.
- Activation and deactivation facilities (via C/I channel).
- Well defined transmission protocols to ensure correct information transfer between GCI compatible devices.
- Point–to–Point and Multipoint communication links.
- Multiplexed mode of operation where up to eight GCI channels can be combined to form a single data stream.

The GCI interface consists of a transmit path, a receive path, an associated clock, and a frame sync signal. These signals are known as D_{out}, D_{in}, DCL, and FSC.

The clock determines the rate of exchange of data in both the transmit and receive directions, and the frame sync signal indicates when this exchange will start.

GCI FRAME STRUCTURE

In a GCI channel, information is in a four byte time–division based structure with a repetition rate of 8 kHz. The four bytes are B1 and B2 channels, a Monitor (M) channel, and a Control/Indication (C/I) channel.

The two independent B channels are used to carry subscriber voice and data information.

The M channel is used for operation and maintenance facilities.

The C/I channel is further subdivided into two bits for the D channel information, four bits for the C/I channel and two bits for the A and E channels that are used to control the transfer of information on the monitor channel.

Figure 11 shows the relative positions of these channels.

NIBBLE MAP DEFINITION

INTRODUCTION

There are seven nibble register (NR0 through NR6) in the MC145574. Control and status information reside in these nibble registers. These nibble registers are accessed via the SCP. The nomenclature used in this data sheet is such that NR2(3) refers to nibble register 2, bit 3.

The MC145574 nibble register map is compatible to the MC145474/475 nibble register map, the only modification being the removal of bits NR6(2) and NR6(1) related to the IDL A/M FIFOs and the addition of bits (NR2(0), NR3(0), and NR4(0) for NT mode only).

Tables 2 and 3 show an SCP nibble map for NT and TE operations, respectively.

Table 2. SCP Nibble Map for NT Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Act Ind (AI)	Error Ind (EI)		Frame Sync (FS)
NR2	Act Req (AR)	Deact Req (DR)	Act Timer T1 Expire	NT Term Class
NR3	IRQ3 Δ Rx Info	IRQ2 Multiframe Reception	IRQ6 FECV Detection	IRQ7 NT Term D Col
NR4	IRQ3 Enable	IRQ2 Enable	IRQ6 Enable	IRQ7 Enable
NR5	Idle B1 Channel on S/T Loop	Idle B2 Channel on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B+D IDL Transparent Loop–back			Exchange B1 and B2 at IDL

Table 3. SCP Nibble Map for TE Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Act Ind (AI)	Error Ind (EI)	Multiframing Detection	Frame Sync (FS)
NR2	Act Req (AR)		Act Timer T3 Expire	Class
NR3	IRQ3 Δ Rx Info	IRQ2 Multiframe Reception	IRQ1 D Channel Collision	
NR4	IRQ3 Enable	IRQ2 Enable	IRQ1 Enable	
NR5	En B1 S/T Loop–back on S/T Loop	En B2 S/T Loop–back on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B+D IDL Transparent Loop–back			Exchange B1 and B2 at IDL

BYTE MAP DESCRIPTION

INTRODUCTION

There are sixteen byte registers (BR0 through BR15) in the MC145574. Control, status, and maintenance information reside in these byte registers. These byte registers are accessed via the SCP. The nomenclature used in this data sheet is such that BR2(3) refers to byte register 2, bit 3.

The byte register map is fully compatible with the byte register map of the MC145474, exceptions are:

1. The functions that were related to the IDL A/M FIFO's have been removed, writing to these registers will have no effect and reading them will return FFH.
2. The TTL Input Level bit BR13 (6) has been removed. The digital inputs are both CMOS and TTL compatible. Writing to this bit has no effect on the circuit, and reading it returns "0" or "1" depending on what value, if any, has been written.
3. The only addition to the byte register map is the bit BR15 (0), used for enabling the overlay registers.

Tables 4 and 5 show the byte map for NT and TE modes of operation, respectively.

OVERLAY MAP DEFINITION

INTRODUCTION

There are ten nibble register (OR0 through OR8 and OR15) in the MC145574. The overlay registers are a second bank of registers available when the overlay register control bit BR15(7) is set to a logic "1". These overlay registers are in the IDL2 TSA mode used to assign the timeslot used by each channel (B1,B2 and D) for transmission and reception: (OR0 through OR5), OR6, OR7 and OR8 are control registers used in the GCI indirect mode and OR15 gives the Revision number of the S/T chip. See Table 6 for the overlay register map.

Table 4. Byte Map for NT Mode of Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0								
BR1								
BR2	SC1.1	SC1.2	SC1.3	SC1.4				
BR3	Q.1	Q.2	Q.3	Q.4	Q Qual	MF Int		
BR4	FV7	FV6	FV5	FV4	FV3	FV2	FV1	FV0
BR5	BPV7	BPV6	BPV5	BPF4	BPV3	BP32	BPV1	BPV0
BR6	B1 S/T LB TP	B1 S/T LB NTP	B2 S/T LB TP	B2 S/T LB NTP	IDL B1 LB TP	IDL B1 LB NTP	IDL B2 LB TP	IDL B2 LB NTP
BR7	ACT PR Disabled	AONT	Enable MFrame	Invert E Channel	IDL MS Mode	IDL CLK SPD 0	LAPD Pol Cont	ACT T2 EXP
BR8								
BR9	TXSC2.1	TXSC2.2	TXSC2.3	TXSC2.4	TXSC3.1	TXSC3.2	TXSC3.3	TXSC3.4
BR10	TXSC4.1	TXSC4.2	TXSC4.3	TXSC4.4	TXSC5.1	TXSC5.2	TXSC5.3	TXSC5.4
BR11	Do Not React to INFO 1	Do Not React to INFO 2	Rx INFO St Bit 1	Rx INFO St Bit 0	Tx INFO St Bit 1	Tx INFO St Bit 0	Ext S/T Loop–back	Tx 96K Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13	NT1 Star		IDL CLK SPD1	Mute B2 to IDL Tx	Mute B1 to IDL Tx	Force E to Zero		
BR14	IDL ADJ En	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR15	Overlay Reg En		Rev 5	Rev 4	Rev 3	Rev 2	Rev 1	Rev 0

Table 5. Byte Map for TE Mode of Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0								
BR1								
BR2	Q.1	Q.2	Q.3	Q.4				
BR3	SC1.1	SC1.2	SC1.3	SC1.4	MF Detect	MF Int		
BR4	FV7	FV6	FV5	FV4	FV3	FV2	FV1	FV0
BR5	BPV7	BPV6	BPV5	BPF4	BPV3	BP32	BPV1	BPV0
BR6	B1 S/T LB TP	B1 S/T LB NTP	B2 S/T LB TP	B2 S/T LB NTP	IDL B1 LB TP	IDL B1 LB NTP	IDL B2 LB TP	IDL B2 LB NTP
BR7	ACT PR Disabled	D Chan Proc Ignored		Map E to D	IDL Free Run	IDL CLK SPD 0	LAPD Pol Cont	
BR8								
BR9	RXSC2.1	RXSC2.2	RXSC2.3	RXSC2.4	RXSC3.1	RXSC3.2	RXSC3.3	RXSC3.4
BR10	RXSC4.1	RXSC4.2	RXSC4.3	RXSC4.4	RXSC5.1	RXSC5.2	RXSC5.3	RXSC5.4
BR11			Rx INFO St Bit 1	Rx INFO St Bit 0	Tx INFO St Bit 1	Tx INFO St Bit 0	Ext S/T Loop–back	Tx 96K Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13			IDL CLK SPD1	Mute B2 to IDL Tx	Mute B1 to IDL Tx		Force IDL Tx	
BR14	IDL ADJ En	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR15	Overlay Reg En		Rev 5	Rev 4	Rev 3	Rev 2	Rev 1	Rev 0

Table 6. Overlay Registers Map

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
OR0	D_{out} B1 CHANNEL TIME SLOT BITS (7:0)							
OR1	D_{out} B2 CHANNEL TIME SLOT BITS (7:0)							
OR2	D_{out} D CHANNEL TIME SLOT BITS (7:0)							
OR3	D_{in} B1 CHANNEL TIME SLOT BITS (7:0)							
OR4	D_{in} B2 CHANNEL TIME SLOT BITS (7:0)							
OR5	D_{in} D CHANNEL TIME SLOT BITS (7:0)							
OR5	(GCI Indirect Mode)					S2	S1	S0
OR6	TSA B1 EN	TSA B2 EN	TSA D EN			GCI_IND EN	CLK1	CLK0
OR7	Disable 3 V Reg	Enable S/G Bit	Enable TCLK	Dual Fr Sync's	Long Frame	8/10 Bits Select	TSEN	TSEN D_EN
OR8			DIS Stal	TE En	MS En	FIX En	NTTerm	Sleep Enable
OR15	Overlay Reg EN		Rev 5	Rev 4	Rev 3	Rev 2	Rev 1	Rev 0

D CHANNEL OPERATION

INTRODUCTION

The S/T interface is designed for full duplex transmission of two 64 kbps B channels and one 16 kbps D channel, between one NT device and one or more TEs. The TEs gain access to the B channels by sending layer 2 frames to the network over the D channel. CCITT I.430 and ANSI T1.605 specify a D channel access algorithm for TEs to gain access to the D channel. The MC145574 S/T transceiver is fully compliant with the D channel access algorithm as defined in CCITT I.430 and ANSI T1.605. The D channel operation is handled through the SCP when using the S/T Interface either in IDL or GCI indirect mode, and handled through the C/I channel when using the S/T Interface GCI direct mode.

The various bits and pins directly pertaining to D channel operation are shown in Tables 7 and 8.

D channel data is clocked into the MC145574 via D_{out} on the falling edges of DCL. Data is clocked out onto D_{out} on the rising edges of DCL in either GCI or IDL2 modes of operation.

IDL2 D CHANNEL OPERATION

Gaining Access to the D Channel in the TE Mode

The pins DREQUEST and DGRANT are used in the TE mode of operation to request and grant access to the D channel. An external device wishing to send a layer 2 frame should bring DREQUEST high, and maintain it high for the duration of the layer 2 frame. DGRANT is an output signal used to indicate to an external device that the D channel is clear. Note that the DGRANT signal actually goes high once received E echo bit prior to the programmed priority class selection. DGRANT goes high at a count of (n – 1) to accommodate the delay between the input of D channel data via the IDL interface and the line transmission of those bits towards the NT. If at the time of the FSR pulse falling edge, the DGRANT and the DREQUEST signals are both detected high, the TE mode transceiver will begin FIFO buffering of the input D channel bits from the IDL interface. This FIFO is four bits deep. Note that DGRANT goes high on the boundaries of the demodulated E bits. In order for the contention algorithm to work on the D channel, HDLC data must be used. The MC145574 modulates the D channel data onto the S/T bus in the form that it is received from the IDL bus. Thus, the data must be presented to it in HDLC format. Note that one of the applications of the MC145488 DDLC is for use with the MC145574 in the terminal mode. The MC145488 will perform the HDLC conversion and perform the necessary D channel handshaking.

Setting the Class for TE Mode of Operation

Recommendation CCITT I.430 and ANSI T1.605 specifications mandate two classes of operation for a TE, with respect to D channel operation. These two classes of operation are class 1 and class 2. Each of these classes have two associated priorities, high priority and low priority. These classes and their associated priorities pertain to the number of demodulated E bits required to be “1”, before the D channel is deemed to be clear for use. Using the MC145574 in the TE mode of operation, the user programs the device for class 1 or class 2 operation by either NR2(0) or pin 10.

Table 9 illustrates how to configure the MC145574 for either class 1 or class 2 operation. This table also illustrates when DGRANT goes high. Note that although DGRANT goes high one E bit before the required count, data will not be modulated onto the D bit timeslots in the S/T frame until the required number of E bits = “1” are received. Thus, data gets modulated onto the D channel if the E bit following the low to high transition of DGRANT is “1”.

The device will automatically switch from high to low priority and back, within each class of operation, in accordance with CCITT I.430 and ANSI T1.605.

MULTIFRAMING

INTRODUCTION

A layer 1 signalling channel between the NT and TE is provided in the MC145574 in accordance with CCITT I.430 and

ANSI T1.605. In the NT and TE direction, this layer 1 channel is the S channel. In the TE to NT direction it is the Q channel. The S channel is subdivided into five subchannels: SC1, SC2, SC3, SC4, and SC5. In normal operation the NT sets its Fa bit (bit 14) to a binary zero every frame. The “wrapping” action of the TE/TEs, as outlined in CCITT I.430 and ANSI T1.605, causes the Fa bit of the TE/TEs to be a “0” also. This is to ensure the existence of two–line code violations per frame, enabling fast synchronization.

Multiframing is activated by the NT by setting the M bit (bit 26) in the NT and TE frame to a binary one, once every 20 frames. In addition to this, the Fa bit (bit 14) in the NT to TE direction is set to a binary one, once every five frames. When multiframing is enabled, the NT sends its S channel data (SC1 through SC5) in the S timeslot (bit 37) every frame. Table 10 shows the order in which the S channel data is transmitted. Note that the M bit = “1” sets the multiframe boundary. Once every five frames the Fa bit is set to “1” in the NT to TE direction. This serves as a Q bit identifier for the TE/TEs, which send their Q data in their Fa bit position in the corresponding frames. In order to avoid Q data collision, those TEs which have not been addressed for multiframing, must send ‘1s’ in the Q bit timeslots.

DEVICE CONFIGURATIONS

The MC145574 can be configured in several different modes for different applications.

NT CONFIGURATIONS

To select NT mode, pin 4 (TE/$\overline{\text{NT}}$) must be held low. The NT device can operate in a mixture of different configurations. How each aspect of the NT’s operation is selected will be discussed separately in the following sections. However for a broad view of the NT’s various flavors, the NT family tree is shown below.

NT Fixed or Adaptive Timing

The receiver/demodulator of the NT can operate in two different modes depending on the type of loop that the device is connected to. These modes are called FIXED and ADAPTIVE Timing modes. The mode of operation is chosen by the state of Pin 6. When this pin is held low, the device is in adaptive mode and when held high, the device is in fixed timing mode. The choice of mode is dependent on the loop characteristics. The intention is that fixed timing should be used for short passive bus configurations and adaptive timing used for all others. However, the performance of the timing recovery circuit employed in the MC145474/75 and hence, also in the MC145574 allows the use of adaptive timing in all loop configurations. Thus, it is recommended that adaptive timing be used in all configurations.

It is also possible to select fixed timing mode via the SCP control bit OR8(2), the FIX pin is internally OR’d with this SCP bit, and one should note that in the NTTerm mode this is the only way to select fixed timing.

NT Master or Slave

In NT mode, the IDL or GCI interface can be selected either as a master or a slave. This selection is made with Pin 5. When held low slave mode is selected and when held high master mode is selected.

In slave mode the IDL/GCI interface frame sync and clock are inputs and the S/T loop interface timing is slaved to these inputs. In master mode the IDL/GCI interface frame sync and clock are outputs, these signals being derived from the 15.36 MHz XTAL oscillator. The S/T loop interface timing, however, is always slaved to the IDL/GCI frame sync.

Therefore, in NT mode the S/T loop interface timing is always slaved to the IDL/GCI frame sync. The source of this timing can be selected to be from the IDL/GCI driver (Slave mode) or from the NT device itself (Master mode).

NT Master mode will be referred to as NTM, likewise NT Slave mode will be NTS.

It is also possible to select NTM by writing to the SCP control bit BR7(3). Or alternatively in TE or $\underline{\text{N}}$T mode, master selection can be made via OR8(3), the M/S pin is internally OR’d with these SCP bits.

NT Star and NT Terminal Modes

In NT mode two further mode extensions can be selected via control bits accessible through the SCP. These NT mode extensions have no effect on the IDL/GCI interface but alter the operation of other pins to perform the desired functions. These two modes are called NT Star and NT Term.

NT Star Mode

Appendix B of ANSI T1.605 describes an example of an NT that will support multiple T interfaces. This is to accommodate multipoint operation with more than eight TEs. The MC145574 can be configured for NT Star mode of operation. This mode is for use in wire ORing multiple NT configured S/T chips on the IDL side. Each NT has a common FSR, DCL, D_{out}, and D_{in}. Each NT is then connected to its own individual S/T loop containing either a single TE or a group of TEs. As such, the contention for either of the B channels or for the D channel is now extended from a single passive bus to a grouping of passive busses.

ISDN employs the use of HDLC data on the D channel. Access to either of the B channels is requested and either granted or denied by the user sending layer 2 frames on the D channel. In normal operation where there is only one NT, the TEs are granted access to the D channel in accordance with their priority and class. By counting the required number of E channel echo bits being “1”, the TEs know when the D channel is clear. Thus, in the NT Star mode of operation, where there are multiple passive busses competing for the same B1, B2, and D channels, the same E echo channel must be transmitted from each NT to its passive bus. This is accomplished in the MC145574 by means of the ANDIN, ANDOUT, and ECHO_IN pins.

Figure 12 shows how to connect the multiple number of NTs in the NT Star mode. Successive connection of the ANDOUT (this is the output of an internal AND gate whose inputs are the demodulated D bits and the data on the ANDIN pin) and ANDIN pins, and the common connections of the ECHO_IN pins, succeeds in sending the same E echo channel to each group of TE/TEs. To configure a series of NTs for NT Star mode, BR13(7) must be set to “1” in each NT. Data transmitted on IDL Tx in NT Star mode, will have the following format: a logic “0” is V_{SS}, a logic “1” causes IDL_D_{out} to go to a high–impedance state. This then permits the series wire ORing of the IDL bus. Note that one of the NTs must have its ANDIN pin pulled high.

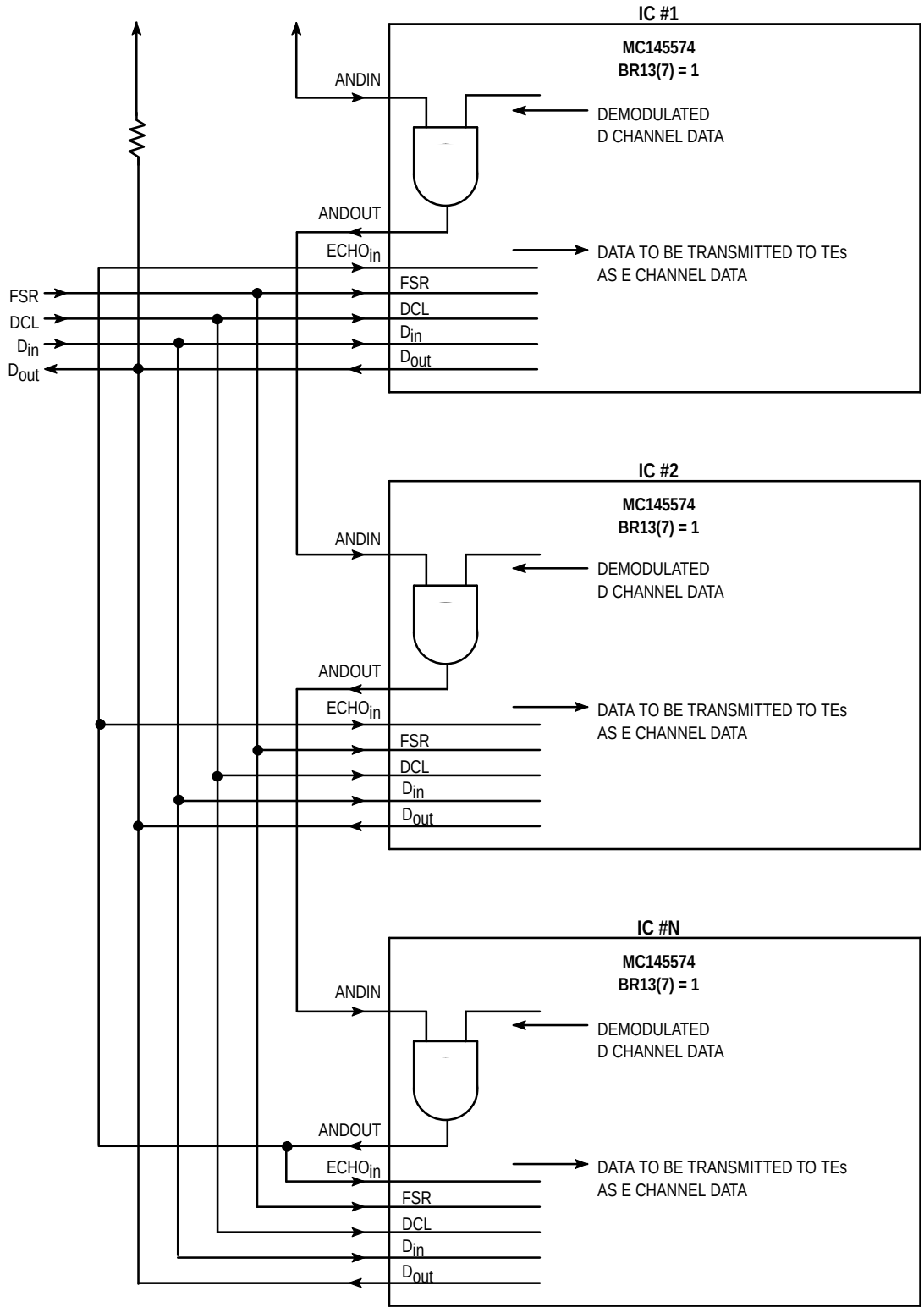
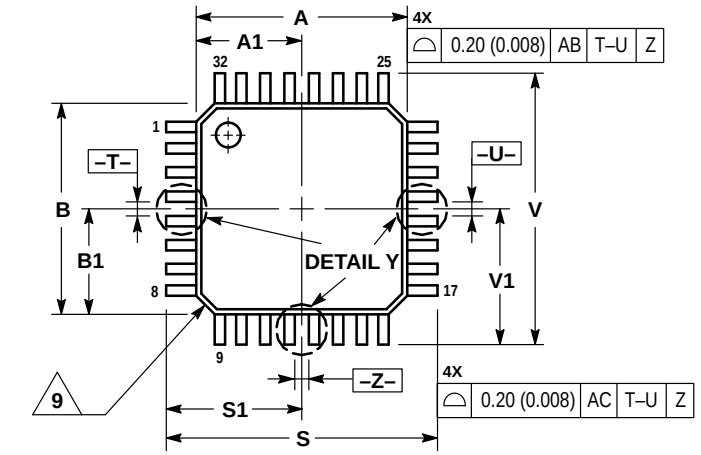
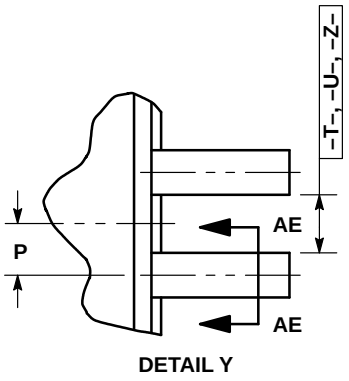


Figure 12. NT Star Mode of Operation

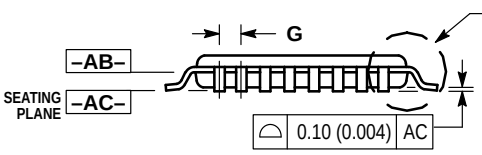
PACKAGE DIMENSIONS

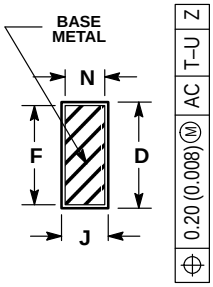
PB SUFFIX
TQFP (THIN QUAD FLAT PACKAGE)
CASE 873A–02



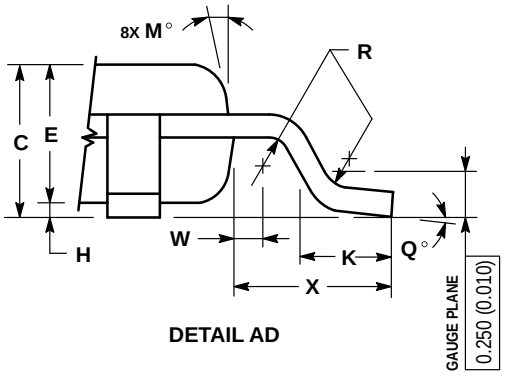


DETAIL Y





SECTION AE–AE

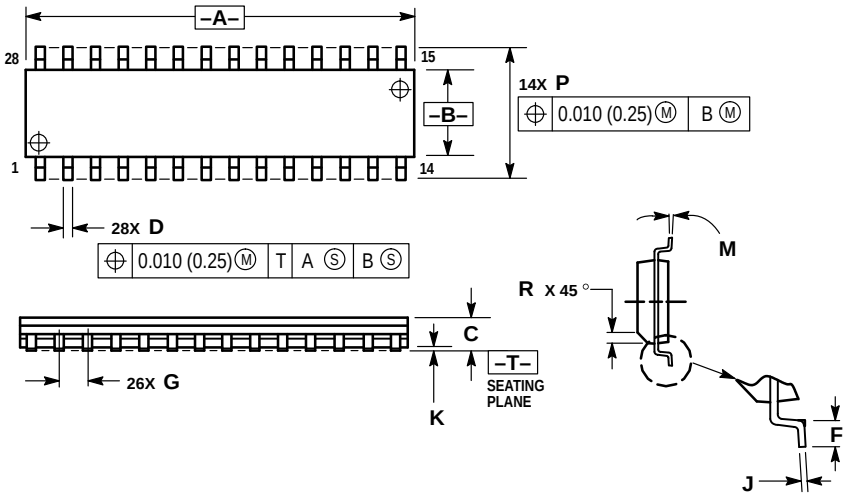


DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

DW SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751F–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.01	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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