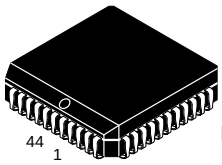
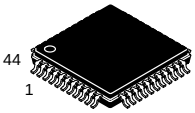
MC145572

Technical Summary

ISDN U-Interface Transceiver



FN SUFFIX
PLCC PACKAGE
CASE 777



PB SUFFIX
TQFP
CASE 824D

ORDERING INFORMATION

MC145572FN	PLCC Package
MC145572PB	TQFP

This technical summary provides an overview of the MC145572 U–Interface Transceiver. A complete data booklet with comprehensive technical information is available and can be ordered through your Motorola Sales office.

The MC145572 U–Interface Transceiver is a single chip device for Integrated Services Digital Network Basic Access Interface that conforms to the American National Standard ANSI T1.601–1992. The device, which can be configured for LT (Line Termination) or NT (Network Termination) applications, performs all necessary Layer 1 functions while utilizing 2B1Q line coding.

The MC145572 is a redesign of the MC145472 and MC14LC5472 U–Interface Transceivers. The internal signal processing algorithms are the same as for the original MC145472 to maintain its industry–leading performance. The control and time division multiplex interfaces have been significantly enhanced to serve the needs of the growing ISDN marketplace. The use of the latest process technologies permits the MC145572 to be made available in 44–lead PLCC and PQFP packages.

The MC145572 is designed to be easily retrofit into existing MC145472/MC14LC5472 designs with no software changes and few hardware changes. New designs can take advantage of enhanced digital interface features of the MC145572, such as the timeslot assigner and the availability of superframe alignment signals.

The MC145572 can operate in many different modes. The control of these various modes is provided via special purpose pins and the Serial Control Port (SCP) or the Parallel Control Port (PCP). The SCP conforms to the Motorola Serial Control Peripheral Interface standard, an industry standard serial microprocessor interface. The PCP is a standard microprocessor bus port. The designer may choose between using GCI or the Motorola IDL–type time division 2B+D data interface. A timeslot assigner is also provided on the MC145572.

The customer data crossing the U Reference Point consists of two 64 kbps B channels and one 16 kbps D channel in each direction. Maintenance and framing overhead is also included for a total 160 kbps data (80 Kbaud signaling) rate.

Features

- Single Chip 2B1Q Echo Canceling Adaptively Equalized Transceiver
- Conforms to ANSI T1.601–1992, *Integrated Services Digital Network (ISDN)–Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification)* of the American National Standards Institute
- Warm Start Capability
- NT Synchronizes to and Operates with 80 kHz ± 32 ppm Received Signal from LT
- Supports Master–Slave, and Slave–Slave Timing Modes
- On–Chip FIFOs for Transmit and Receive Directions
- 2B+D Customer Data Provided by the Industry Standard Interchip Digital Link
- General Circuit Interface (GCI)
- Timeslot Assigner
- Control, Status, and Extended Maintenance Functions Provided through the Serial Control Port (SCP)
- Microprocessor Bus Compatible Parallel Port Available as Pin Selectable Option

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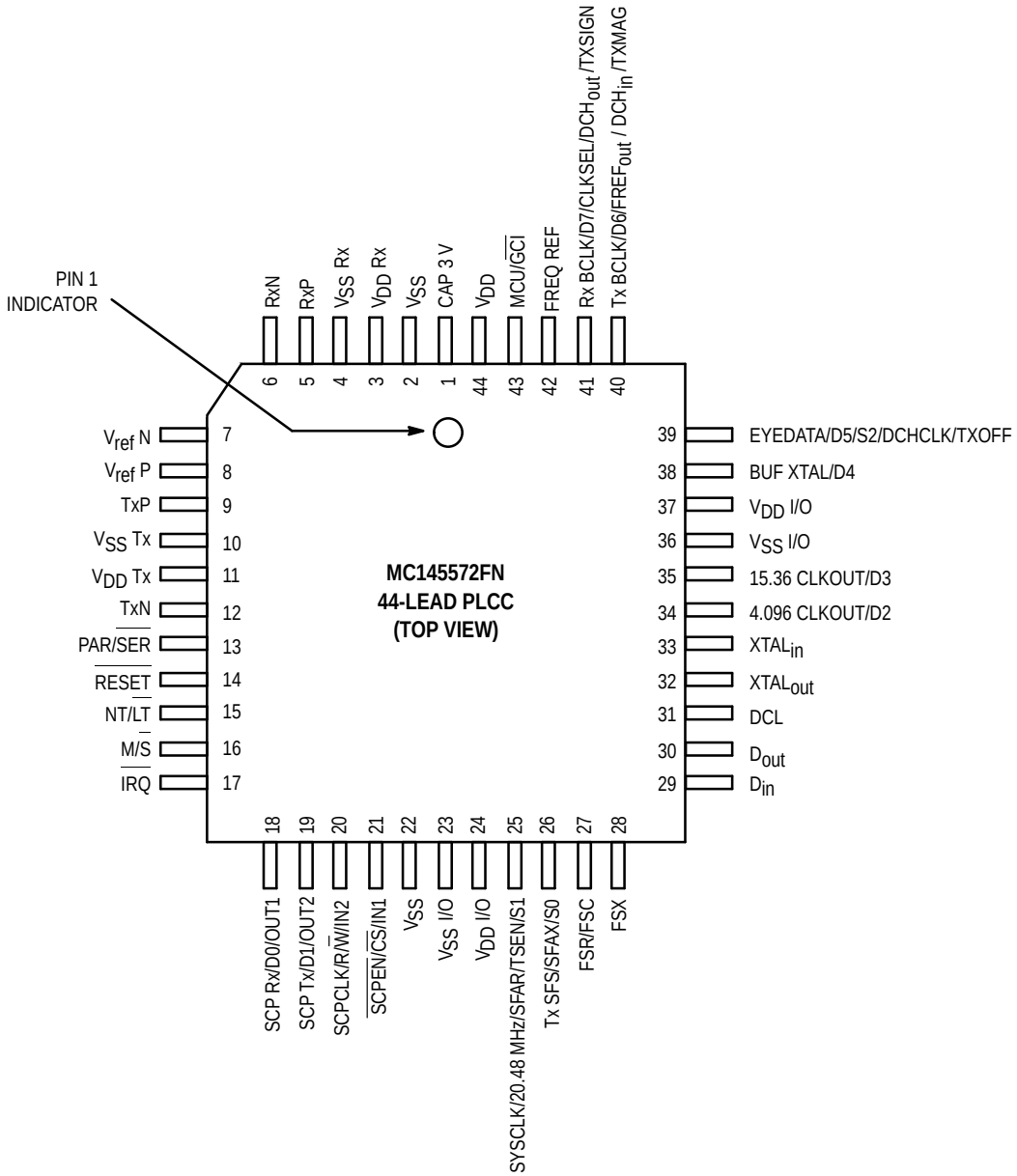
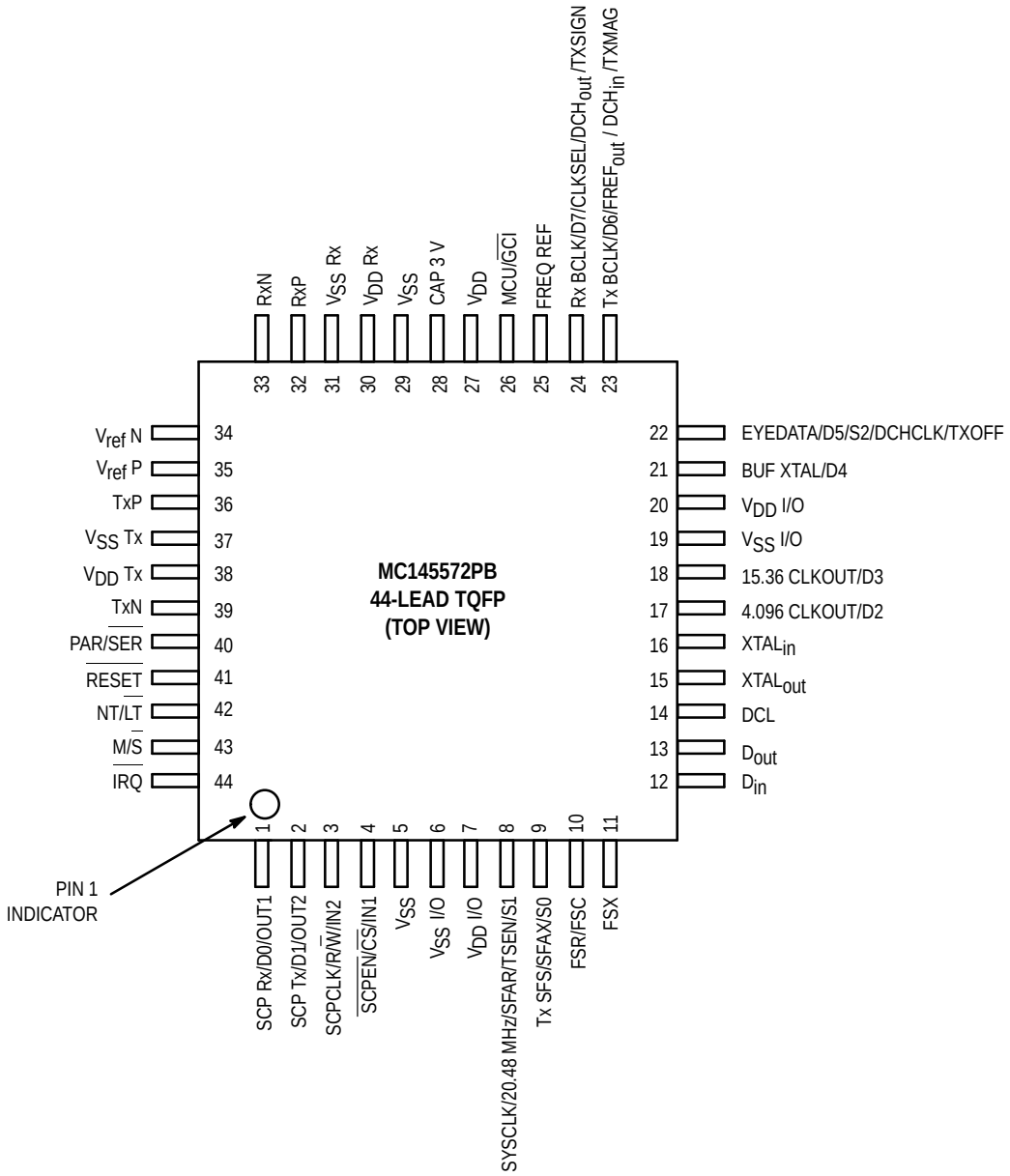
- On–Chip Conformance with Activation and Deactivation as Specified in ANSI T1.601
- Automatic Handling of Basic Maintenance Functions
- Automatic Internal Compliance with the Embedded Operations Channel (eoc) Protocol as Specified in the American National Standard
- Complete Set of Loop–Backs for Both the IDL and U–Reference Point Directions
- Pin Selectable for Line Termination or Network Termination Applications
- On–Chip 2.5 V Transmit Driver Meeting 1992 Requirement
- 8 kHz Reference Frequency in LT Mode
- High Performance CMOS Process Technology
- 5 V Power Supply

MC145572FN PIN ASSIGNMENT



MC145572PB PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to 7.0	V
V_{in}	Voltage, Any Pin to V_{SS}	– 0.3 to V_{DD} + 0.3	V
I_{in}	DC Current, Any Pin (Except for V_{DD}, V_{SS}, TxP, and TxN)	± 10	mA
T_A	Operating Temperature	– 40 to 85	°C
T_{stg}	Storage Temperature	– 85 to 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., V_{SS}, V_{DD}, V_{LS}, or V_{AG}).

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = – 40 to 85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Current Sourced from CAP 3 V pin @ 2.7 V	CAP 3V	—	—	5	mA

POWER CONSUMPTION (Voltages referenced to V_{SS}, T_A = – 40 to 85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Power Consumption, Activated		—	225	275	mW
Power Consumption, Absolute Power Down		—	—	5	mW

PERFORMANCE (V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C)

Parameter	Min	Typ	Max	Unit
Cold Start Time, LT Mode	—	9	—	s
Cold Start Time, NT Mode	—	4	—	s
Warm Start Time, LT and NT Modes	—	200	—	ms
Transmit Linearity	45	—	—	dB
Bit Error Rate, 16,500k ft of 26 AWG, 1500 ft of 24AWG, +1 dB NEXT Margin, ANSI T1.601–1992 (see Note)	—	—	10^{-7}	
Differential Receiver Sensitivity		15	20	mV

NOTE: Bit error rate performance depends significantly on the characteristics of the line interface circuit used to couple the MC145572 to the transmission line. This parameter is provided for informational purposes only.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V + 5%, T_A = – 40 to 85°C)

Parameter	Test Conditions	Symbol	Min	Max	Unit
High–Level Input Voltage, except FREQREF and RESET		V_{IH}	2.0	—	V
Low–Level Input Voltage, except FREQREF and RESET		V_{IL}	– 0.3	0.8	V
High–Level Input Voltage, FREQREF and RESET		V_{IH}	3.75	—	V
Low–Level Input Voltage, FREQREF and RESET		V_{IL}	—	1.25	V
High–Level Output Voltage (I_{OH} = – 400 μA)		V_{OH}	2.4		V
Low–Level Output Voltage (I_{OL} = 5 mA)		V_{OL}		.5	V
High–Level Input Current		I_{IH}	—	TBD	μA
Low–Level Input Current		I_{IL}	—	TBD	μA
High–Level Output Current	$V_{OH} = V_{DD} - 0.5$ V	I_{OH}	TBD	—	mA
Low–Level Output Current	V_{OL} = 0.4 V	I_{OL}	TBD	—	mA
$\overline{IRQ}$ Output Current	V_{OL} = 0.4 V	I_{IRQ}	TBD	—	mA
$\overline{IRQ}$ High Impedance		$R_{IRQ\ off}$	TBD	—	kΩ
Input Capacitance, Digital Pins		C_{in}	—	10	pF
$XTAL_{in}$ High–Level Input			TBD	—	V
$XTAL_{in}$ Low–Level Input			—	TBD	V
$XTAL_{out}$ Output Current	V_{OH} = 3.2 V		TBD	—	mA
	V_{OL} = 1 V		TBD	—	mA

NOTE: All digital outputs except $XTAL_{out}$ are three–stateable regardless of their normal operating condition.

2B1Q INTERFACE ELECTRICAL CHARACTERISTICS

PINS TxP AND TxN (V_{DD} = 5.0 V ± 5%, T_A = – 40 to 85°C, R_L = 60 Ω from TxP to TxN)

Parameter	Min	Typ	Max	Unit
Output Resistance — Full Power Mode	—	—	0.05	Ω
Output Resistance — Power Down Mode	—	10	30	Ω
Output Resistance — Absolute Power Down Mode	—	10	30	Ω
Output Peak Voltage from TxP to TxN	—	± 4.0	—	V_{pk} $-V_{pk}$
Output Load Capacitance	—	—	47	nF
Power Supply Rejection	—	60	—	dB
Peak Current	—	75	—	mA

PINS TxP AND TxN (V_{DD} = 5.0 V ± 5%, T_A = – 40 to 85°C)

Parameter	Min	Max	Unit
Input Resistance — Full Power Mode	1	—	MΩ
Input Resistance — Power Down Mode	1	—	MΩ
Input Resistance — Absolute Power Down Mode	1	—	MΩ
Input Capacitance	—	TBD	pF
Power Supply Rejection	—	TBD	dB
Input Voltage Range for RxP or RxN	$((V_{DD} - V_{SS})/2) - 0.5$	$((V_{DD} - V_{SS})/2) + 0.5$	V

IDL2 MASTER SHORT FRAME SYNC TIMING, 8/10 BIT AND TSAC FORMATS

Ref. No.	Parameter		Min	Typ	Max	Unit	Note
1	FSR or FSX Period		125	125	—	µs	1
2	Delay From the Rising Edge of DCL to the Rising Edge of FSX or FSR		—		30	ns	
3	Delay From the Rising Edge of DCL to the Falling Edge of FSX or FSR		—		30	ns	
4	DCL Clock Period		391		1953	ns	2
5	DCL Pulse Width High	512 kHz	878		1074	ns	3
		2.048 MHz	210		265		
		2.56 MHz	170		215		
	DCL Clock 249 Pulse Width High	2.048 MHz	160		315		
		2.56 MHz	120		265		
	DCL Clock 59 Pulse Width High	512 kHz	825		1120		
6	DCL Pulse Width Low		45		55	% of DCL Period	4
7	Delay From Rising Edge of DCL to Low–Z and Valid Data on D_{out}		—		30	ns	
8	Delay From Rising Edge of DCL to Data Valid on D_{out}		5		30	ns	
9	Delay From Rising Edge of DCL to Hi–Z on D_{out}		—		30	ns	
10	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)		25		—	ns	
11	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)		25		—	ns	
12	Delay From Rising Edge of DCL to TSEN Low		—		30	ns	5
13	Delay From Falling Edge of DCL to TSEN High		—		30	ns	

NOTES:

1. FSR or FSX occur on average every 125 µs.
2. The DCL Frequency may be 512 kHz, 2.048 MHz, or 2.56 MHz.
3. The duty cycle of DCL is between 45% and 55% when operated in master timing mode. This duty cycle is guaranteed for all DCL clocks except the clock that is used for making timing adjustments in order to maintain synchronization with the received signal when operating in NT mode. In NT master mode the MC145572 conveys timing adjustments over the DCL clock of the device. This is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive IDL frames once per U–Interface basic frame. The total adjustment is 96 ns distributed over the two IDL frames. When DCL is configured for 2.048 MHz or 2.56 MHz the adjustment occurs during clock pulse number 249 after FSX/FSR. The count starts at clock pulse 0 for the DCL clock immediately following FSX/FSR. When DCL is configured for 512 kHz the adjustment occurs during DCL pulse number 59. It is important to remember this when using the timeslot assigner since it is possible to program it to transfer 2B or D data during the clock period where the timing adjustment is being made and this may affect setup and hold times for other components in a system.
4. The pulse width during the low phase of the clock varies between 45% and 55% of the nominal frequency. Timing adjustments are not made during the low phase of DCL.
5. In IDL 8 and 10 bit formats, TSEN can be valid during the B1, B2, and D channel timeslots.

ISDN BASIC ACCESS SYSTEM OVERVIEW

ISDN REFERENCE MODEL

The Integrated Services Digital Network (ISDN) Reference Model is shown in Figure 1. This is a general model that can be adapted to many different implementations of the ISDN. The diagram indicates the position of the U–Reference Point between the Line Termination (LT) and the Network Termination 1 (NT1) blocks in the model.

The U–Interface is the physical access point to the ISDN at the U–Reference Point. This interface is a single twisted wire pair supporting full–duplex transmission of digital information at a rate of 160 kbps. The twisted wire pair can extend up to 18,000 feet and may include bridge taps. This interface is often referred to as a Digital Subscriber Line.

U–INTERFACE TRANSCEIVER ISDN APPLICATIONS

Figure 2 shows some typical ISDN applications of the MC145572 U–Interface Transceiver as well as related ISDN applications for S/T–Interface terminal equipment using Motorola semiconductor solutions.

The LT example shows the U–Interface Transceiver in a line card environment. This line card can be located in an ISDN central office switch or other ISDN compatible switching equipment, including a remote switch or carrier terminal. In this application, the Interchip Digital Link (IDL) and Serial Control Port (SCP) of the MC145572 are interfaced to the backplane of the switching equipment as required for the particular switch architecture.

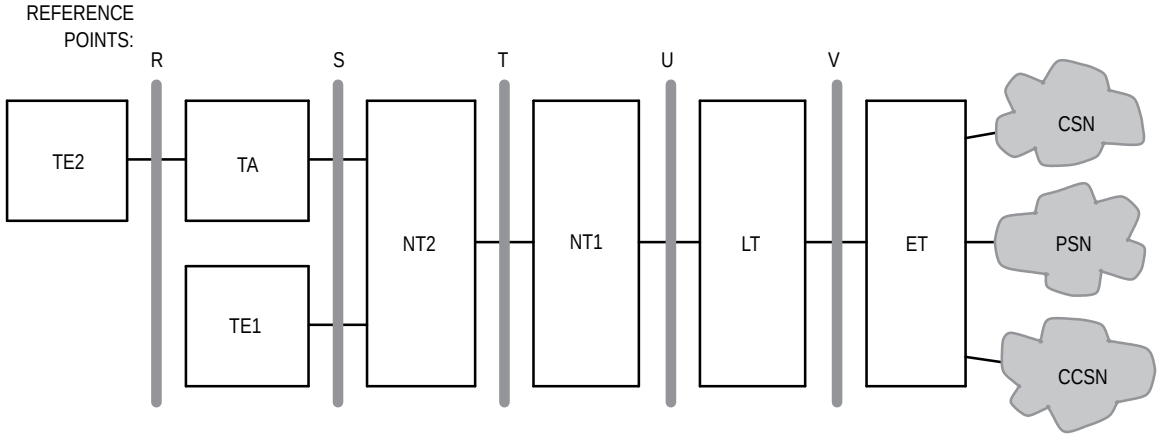
The NT1 converts the 2–wire U–Interface to the 4–wire S/T–Interface as shown. By combining an MC145572 with a Motorola MC145574 S/T–Interface Transceiver, an NT1 can be readily implemented.

Also shown is a highly integrated U–Interface ISDN terminal, designated NT1/TE1, which implements a complete voice and data terminal with a U–Interface for immediate and cost effective access to the ISDN. The MC145572 is shown interfaced to the M68000 core based MC68302 Integrated Multiprotocol Processor (IMP), which handles Layers 2 – 7 of the OSI Reference Model. Voice is supported with a conventional codec–filter device such as the MC145480.

The network is completed with a Terminal Adaptor (TA) and an S/T–interface ISDN Terminal (TE1). Two different architectures are shown: the TA is implemented with the MC145488 Dual Data Link Controller and a host MCU system, and the TE1 is shown implemented with the MC68302 IMP.

NON–ISDN U–INTERFACE TRANSCEIVER APPLICATIONS

A typical non–ISDN pair gain application block diagram is shown in Figures 3 and 4. Pair gain is a technique to multiplex two or more analog phone lines over a single twisted pair.



Key:

CCSN:	Common Channel Signalling Network	NT2:	Network Termination 2 (OSI Layers 2 and 3)
CSN:	Circuit Switched Network	PSN:	Packet Switched Network
ET:	Exchange Termination (C.O. Switch)	TA:	Terminal Adapter
LT:	Line Termination (Line Card)	TE1:	Terminal Equipment 1 (ISDN Terminal)
NT1:	Network Termination 1 (OSI Layer 1 Only)	TE2:	Terminal Equipment 2 (Non–ISDN Terminal)

Figure 1. ISDN Reference Model

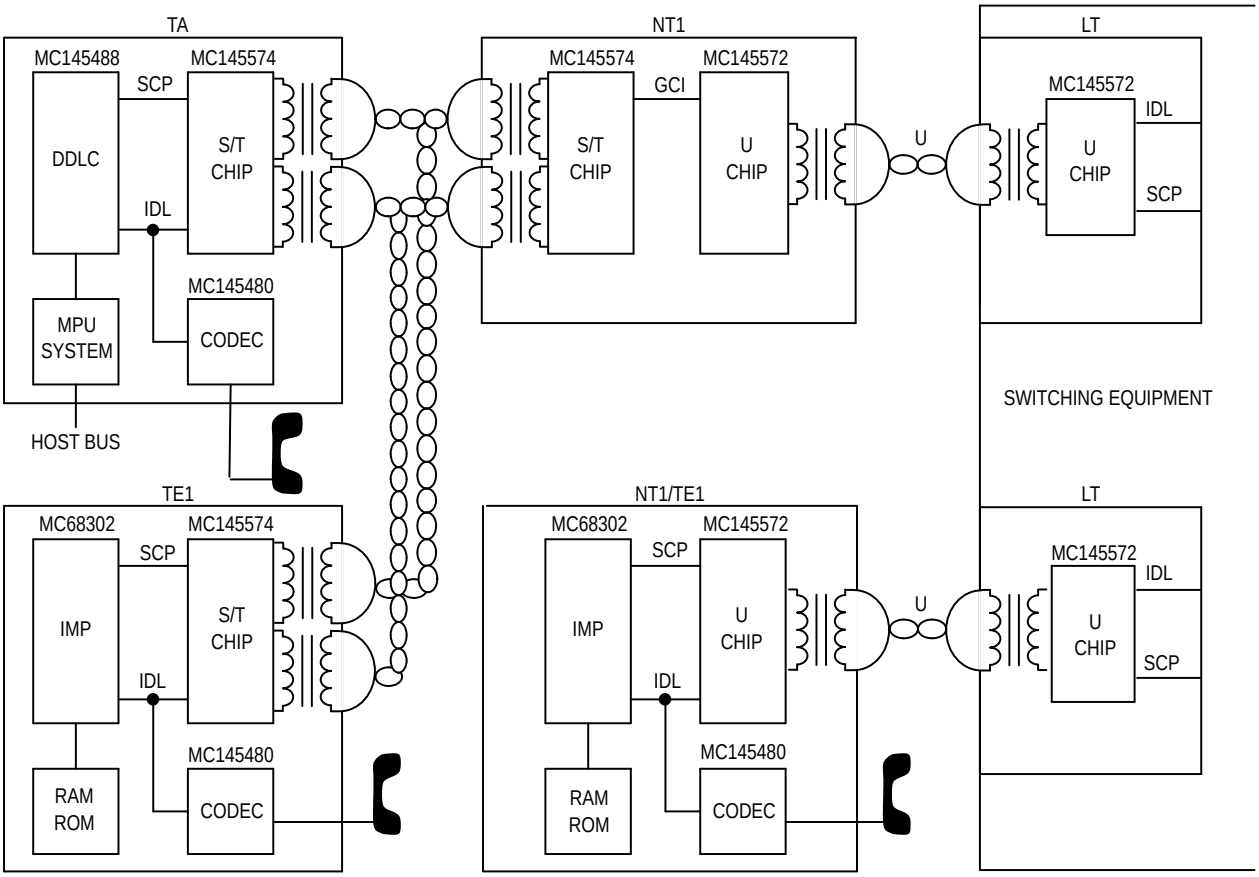


Figure 2. MC145572 Typical ISDN Applications

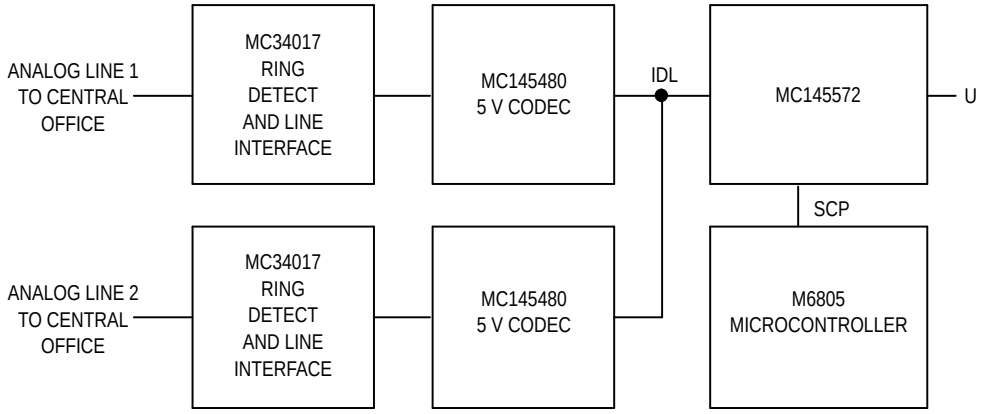


Figure 3. Pair Gain Application, Central Office Terminal

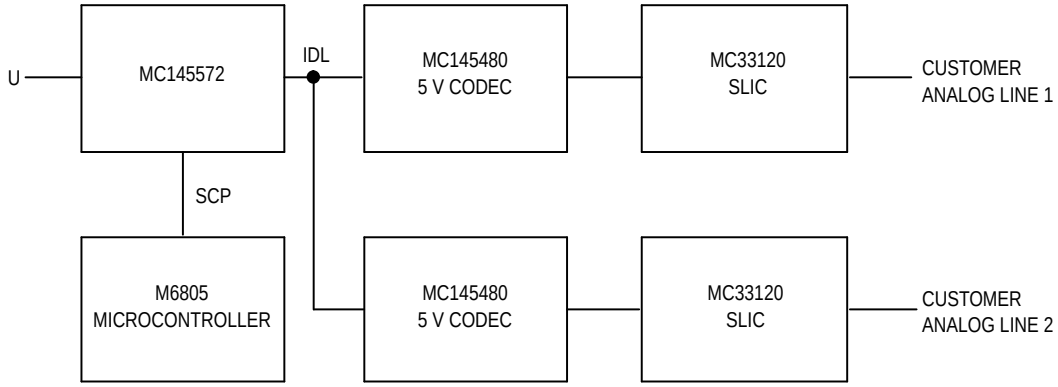


Figure 4. Pair Gain Application, Remote Terminal

FUNCTIONAL OVERVIEW

A functional block diagram of the MC145572 U–Interface Transceiver is shown in Figure 5. This device utilizes mixed analog and digital signal processing circuit technology to implement an adaptively equalized echo canceling full–duplex transmitter/receiver or transceiver.

The 2B+D data is input to the device at the D_{in} pin of the time division multiplexed data interface. This data is passed through a three frame deep FIFO prior to being formatted and scrambled in the Superframe Framer. The resulting 160 kbps binary data stream is converted to an 80 kbaud dibit stream which is subsequently converted to four analog amplitudes by the DAC (digital–to–analog converter). The resulting pulse amplitude modulated signal is band limited by the Tx Filter prior to entering the Tx Driver which differentially drives the line coupling circuit to the twisted wire pair.

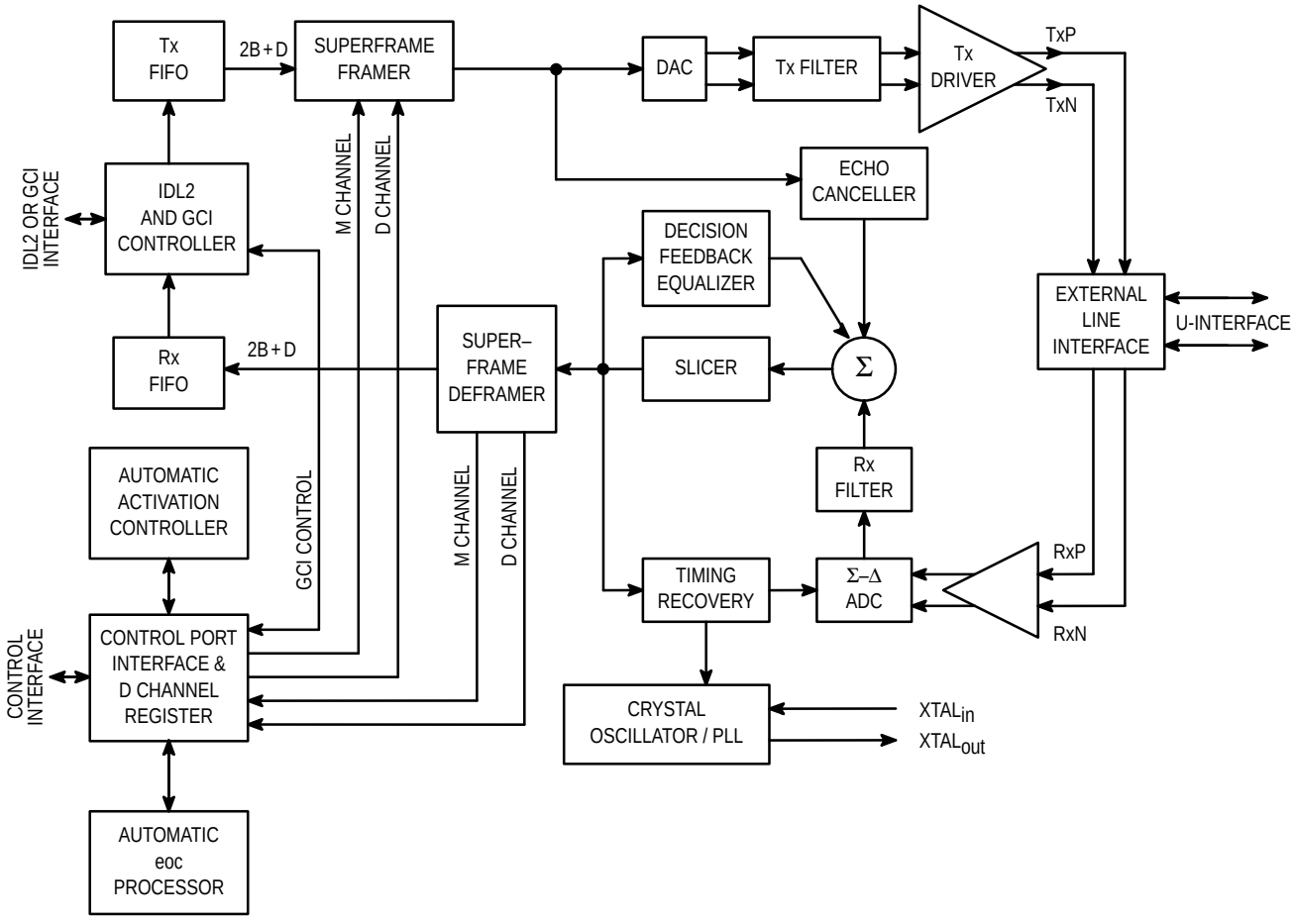


Figure 5. MC145572 Functional Block Diagram

From the twisted wire pair, information from the far end U–Interface Transceiver is coupled through the external line interface circuit to the differential receiver inputs RxP and RxN. (In this two wire environment, the transmitted signal is also coupled into the receiver inputs.) This combined analog signal is converted to a digital word in the Σ–Δ (sigma–delta) ADC (analog–to–digital converter). After filtering, an adaptively generated replica of the transmitted signal, calculated by the echo canceler, is subtracted from the combined signal leaving only the far end signal. In addition, phase distortion present in the far end signal is corrected by the Decision Feedback Equalizer. The resulting four level signal is decoded by the slicer to produce a 160 kbps data stream. Timing information is also recovered from the far end signal. The Superframe Deframer descrambles and disassembles the received superframes and passes the received 2B+D data through a three IDL frame deep FIFO to the IDL Interface where it is available at the D_{out} pin of the time division multiplexed data interface.

The MC145572 permits the designer to select one of three options for control of the device and access to its register set. When operating in MCU mode the MC145572 can be configured for either Serial Control Port or Parallel Control Port mode of operation. In Serial Control Port mode control and status of the device is handled via the Serial Control Port (SCP), a standard four wire serial microcontroller interface. In Parallel Control Port mode the MC145572 is configured to provide an eight bit wide data port with a chip select and read/write pin. In either case the internal register set of the MC145572 gives an external microcontroller access to the 4 kbps Maintenance Channel provided across the U–interface.

When the MC145572 is configured for GCI mode the Command/Indicate channel of the GCI interface is used for control and status messages. The GCI Monitor channel is used to send and receive maintenance channel messages. The Monitor channel also permits the internal registers of the MC145572 to be read from or written to if it is desired to bypass the normal operation of the GCI interface.

The Embedded Operations Channel (eoc) portion of the M–channel can be handled automatically with the internal Automatic eoc Processor. In addition, activation and deactivation of the MC145572 is handled by an Automatic Activation Controller.

The MC145572 requires a single 20.48000 MHz pullable crystal connected between the $XTAL_{in}$ and $XTAL_{out}$ pins. No other external components are required for the crystal oscillator. Internal crystal pulling circuitry adjusts the crystal frequency in both the LT and NT modes of operation.

MC145572/MC14LC5472 COMPATIBILITY

After either a hardware or software reset the MC145572 maintains basic pin function and register compatibility with the MC14LC5472 U–Interface Transceiver when configured for MCU mode and using the Serial Control Port interface. There are differences between the MC14LC5472 and the MC145572 in exact signal requirements and outputs for these pins.

Most software written for the MC14LC5472 will operate the MC145572 without requiring any modifications. The MC145572 has an extended register set which provides access to the on chip timeslot assigner, I/O pin configuration bits, the D Channel, and internal parameters of the device. The extended registers are accessed by setting bits in register BR10 that were reserved bits for the MC14LC5472. The new registers then overlay the original registers and are referred to in this document as Overlay Registers OR0 through OR9, OR12, and OR13. Register BR10 is common to both register sets permitting software to switch between the basic register set and the overlay register set as required.

PIN DESCRIPTION QUICK REFERENCE

Tables 1 through 5 list the MC145572 pins in functional groups and provide brief pin descriptions. For more detailed information, refer to the section indicated in the title.

Table 1. Power Supply and Mode Selection Pins

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
Power Supply Pins			
V_{DD}	27	44	Positive power supply, nominally + 5 V.
V_{SS}	29, 5	2, 22	Negative power supply, nominally ground.
V_{DD} Rx, V_{DD} Tx	30, 38	3, 11	Positive power supply for analog circuits, nominally + 5 V.
V_{SS} Rx, V_{SS} Tx	31, 37	4, 10	Negative power supply for analog circuits, nominally ground.
V_{DD} I/O	7, 20	24, 37	Positive power supply for input and output circuits, nominally + 5 V.
V_{SS} I/O	6, 19	23, 36	Negative power supply for input and output circuits, nominally ground.
CAP 3V	28	1	Connection for internal 3 V regulator decoupling capacitor.
Mode Selection Pins			
$\overline{\text{RESET}}$	41	14	Hardware reset when at a logic low, normal operation when at a logic high. This pin has a Schmitt trigger input.
NT/$\overline{\text{LT}}$	42	15	Hardware selection of LT (logic low) and NT (logic high) operating mode.
MCU/$\overline{\text{GCI}}$	26	43	MCU mode versus GCI mode select input.
PAR/$\overline{\text{SER}}$	40	13	Parallel versus serial control port selection. PAR/$\overline{\text{SER}}$ = 1 (logic high) for a parallel port. PAR/$\overline{\text{SER}}$ = 0 (logic low) for serial control port interfacing.

Table 2. Time Division Multiplex Interface Pins

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
Time Division Multiplex Data Interface			
M/$\overline{\text{S}}$	43	16	Master/Slave mode select input for the IDL2 or GCI interface. Master mode for M/$\overline{\text{S}}$=1 (logic high).
FSR/FSC	10	27	The MCU 8 kHz Frame Sync for data transmitted on the D_{out} pin. In GCI operation, this pin serves as the FSC pin.
FSX	11	28	The MCU 8 kHz frame sync for data input to the D_{in} pin. This pin is not used in GCI mode.
DCL	14	31	MCU bit clock, or GCI 2x bit clock.
D_{out}	13	30	Serial data out of MCU or GCI interface.
D_{in}	12	29	Serial data into MCU or GCI interface.

Table 3. Digital Data Interface Pins

Pin Name			Pin No.		
MCU/SCP Mode	**MCU/PCP Mode**	**GCI Mode**	**TQFP**	**PLCC**	**Pin Description**
SCPEN	CS	IN1	4	21	In serial port, MCU mode, SCPEN is the active low SCP enable input. In parallel port, MCU mode, CS is the active low chip select. In full GCI mode, defined when MCU/GCI = 0, this input is IN1.
SCPCLK	R/W	IN2	3	20	In serial port, MCU mode, SCPCLK is the serial control port clock input. In parallel port, MCU mode, R/W is the read versus write indication to the parallel port. In full GCI mode, defined when MCU/GCI = 0, this input is IN2.
SCP Rx	D0	OUT1	1	18	In serial port, MCU mode, SCP Rx is the serial control port data input. In parallel port, MCU mode, D0 is the LSB of the parallel data bus. In full GCI mode, defined by MCU/GCI = 0, OUT1 is an output reflecting the state of bit 5 as set in BR7.
SCP Tx	D1	OUT2	2	19	In serial port, MCU mode, SCP Tx is the serial control port data output. In parallel port, MCU mode, this is signal D1 of the parallel data bus. In full GCI mode, defined by MCU/GCI = 0, OUT2 is an output reflecting the state of bit 6 as set in BR7
IRQ	IRQ	—	44	17	Open–drain active low output for microcontroller interrupt.
4.096 CLKOUT	D2	4.096 CLKOUT	17	34	4.096 MHz clock out. In parallel port, MCU mode, this is signal D2 of the parallel data bus.
15.36 CLKOUT	D3	15.36 CLKOUT	18	35	15.36 MHz clock out. Not synchronized to recovered clock in the NT mode. In parallel port, MCU mode, this is signal D3 of the parallel data bus.
BUF XTAL	D4	BUF XTAL	21	38	This is a square wave output from the 20.48 MHz oscillator and it is not synchronized to the recovered clock in the NT mode. In parallel port, MCU mode, this is signal D4 of the parallel data bus.
EYEDATA DCHCLK	D5	S2	22	39	In serial port MCU mode, this pin may carry either EYEDATA or DCHCLK. In parallel port MCU mode, this is signal D5 of the parallel data bus. In full GCI mode, this pin is the S2 input.
TXBCLK DCH_{in}	D6	$FREF_{out}$	23	40	In serial port MCU mode, this pin may carry either TXBCLK or DCH_{in}. TXBCLK is an 80 kHz clock output, aligned and synchronized to the transmitted baud. DCH_{in} is the D channel port serial data input. In parallel port MCU mode, this is signal D6 of the parallel data bus. In full GCI mode, operating as a GCI slave, this pin provides 2.048 MHz or 512 kHz synchronized clock output.
RXBCLK DCH_{out}	D7	CLKSEL	24	41	In serial port MCU mode, this pin may carry either RXBCLK or DCH_{out}. RXBCLK is an 80 kHz clock output, aligned and synchronized to the received baud. DCH_{out} is the D channel port serial data output. In parallel port MCU mode, D7 is the MSB of the parallel data bus. In full GCI mode, operating as a GCI master, CLKSEL selects between 512 kHz and 2.048 MHz for DCL. CLKSEL = 1 selects 2.048 MHz.
SYSCLK 20.48 MHz SFAR TSEN	SYSCLK 20.48 MHz SFAR TSEN	S1	8	25	In either MCU mode, this pin may carry either SYSCLK, 20.48 MHz, SFAR, or TSEN outputs. SYSCLK is a 10.24 MHz clock for sampling EYEDATA. SFAR is the receive data superframe alignment output in the NT and LT modes. TSEN is an active low open–drain buffer enable output, used for enabling a bus driver to buffer MCU data out from the MC145572, onto a PCM highway. TSEN is active only when D_{out} is active. In full GCI mode, this pin is the S1 input.
Tx SFS SFAX	Tx SFS SFAX	S0	9	26	In either MCU mode, this pin may carry either Tx SFS output, or SFAX input/output. When this pin is unused connect a 100 kΩ resistor to V_{SS} in LT mode. Tx SFS is provided for compatibility to the MC145472, which provides an absolute transmit superframe reference. SFAX is the transmit data superframe alignment input in the LT mode, or superframe alignment out put in the NT mode. In LT mode SFAX can also be an output. In full GCI mode, this pin is the S0 input.

Table 4. 2B1Q Interface Pins

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
TxP, TxN	36, 39	9, 12	Positive and negative outputs of the differential transmit driver.
RxP, RxN	32, 33	5, 6	Positive and negative inputs to the differential receive circuit.
V_{ref} P, V_{ref} N	35, 34	8, 7	Positive and negative signals for internal voltage reference. Connect a 0.1 μF ceramic capacitor between V_{ref}P and V_{ref}N.

Table 5. Phase–Locked Loop and Clock Pins

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
FREQREF	25	42	LT mode: 8 kHz reference clock input (Schmitt trigger input). NT mode: optional synchronized clock output, selected by control register in the MCU mode (MCU/GCI = 1).
$XTAL_{in}$, $XTAL_{out}$	16, 15	33, 32	Input and output signals of the 20.48 MHz crystal oscillator amplifier.

CONTROL INTERFACES

When operated in MCU mode the MC145572 has two configurations that provide MCU access to its internal register set. The Serial Control Port mode is a four wire serial interface that clocks data into or out of the MC145572 at data rates up to 4 Mbps. The Parallel Control Port mode configures the MC145572 to have an eight bit parallel data port that can be located anywhere in processor memory.

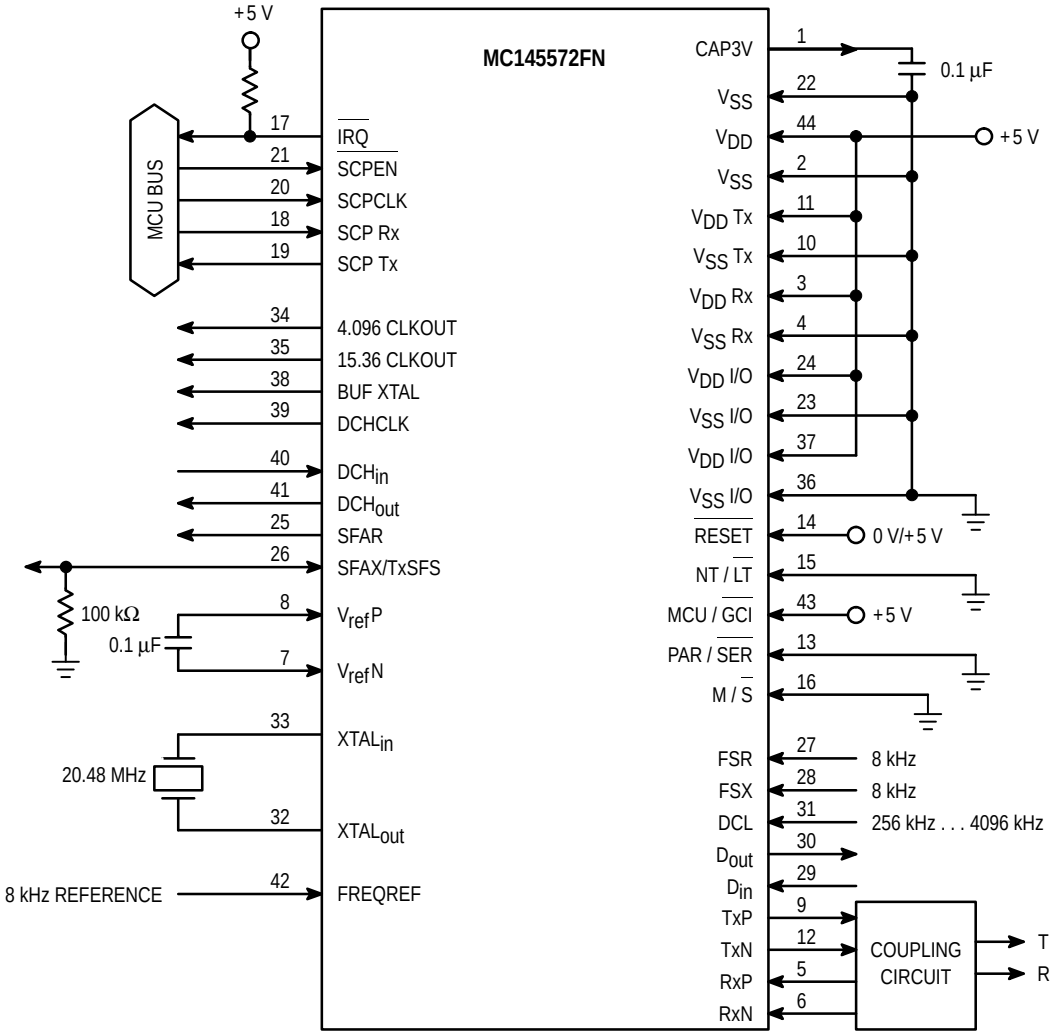
SERIAL CONTROL PORT MODE

The MC145572 is equipped with an industry standard Serial Control Port Interface. The Serial Control Port (SCP) is used by an external controller, such as an M68HC05 family microcontroller, MC145488 Dual Data Link Controller, or MC68302 Integrated Multiprotocol Processor, to communicate with the U–Interface Transceiver.

The SCP is a full–duplex four wire interface with control and status information passed to and from the U–Interface Transceiver. The Serial Control Port Interface consists of a transmit output, a receive input, a data clock, and an enable signal. These device pins are known as SCP Tx, SCP Rx, SCPCLK, and SCP EN, respectively. The SCP Clock determines the rate of exchange of data in both the transmit and receive directions, and the SCP Enable signal governs when this exchange is to take place. The four wire SCP Interface is supplemented with an interrupt request line, IRQ, for external microcontroller notification of an event requiring service.

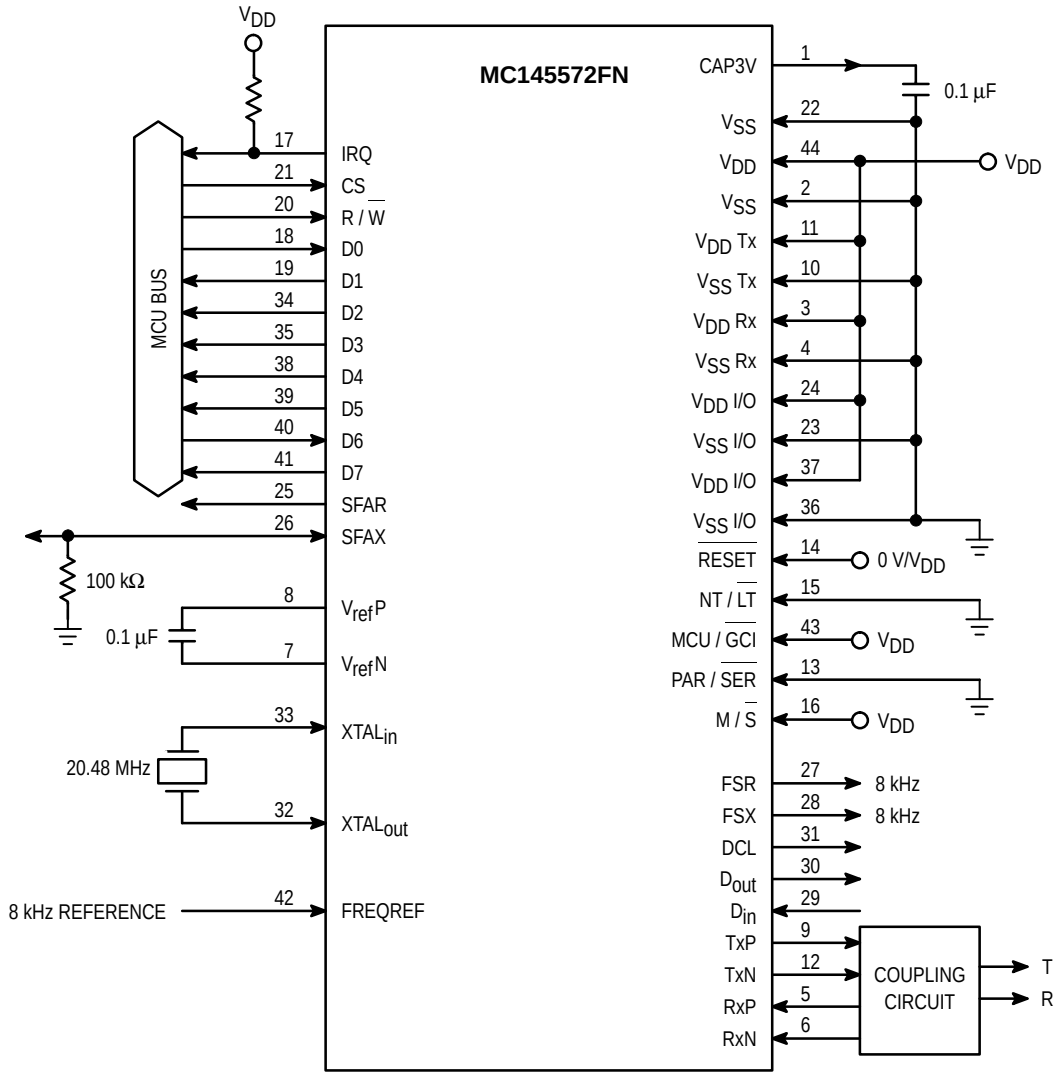
PARALLEL CONTROL PORT MODE

In the Parallel Control Port mode the MC145572 is configured to have a single address /byte wide data port for access to the internal register set. A read/write pin (R/W) and chip select pin (CS) are provided to enable read or write accesses to the data port. For an external microcontroller such as the MC68302 to access an individual nibble, byte or overlay register a sequence of write and read operations is required. The first access is always a write cycle that writes a pointer and internal read/write indicator to the MC145572. The pointer byte contains the Nibble or Byte Register address and for the case of Nibble Register writes the data to be written. This initial write may be followed by up to two read accesses or one write access. An open drain IRQ output pin is provided for interrupting an external MCU when a change of status is detected by the MC145572. Figure 7 shows pin configurations to operate the MC145572 in MCU mode using the Parallel Control Port for access to the register set.



NOTE: In LT mode the 100 kΩ resistor on SFAX/TxSFS is required when none of these pin functions is enabled.

Figure 6. MCU Mode with Serial Control Port Configuration



NOTE: In LT mode the 100 kΩ resistor on SFAX/TxSFS is required when none of these pin functions is enabled.

Figure 7. MCU Mode with Parallel Control Port Configuration

MCU MODE REGISTER DESCRIPTION REFERENCE

This section describes all of the MC145572 U–Interface Transceiver control and status registers available via the Serial and Parallel Control Ports. Tables 6 through 8 contain Register Maps.

The internal registers of the MC145572 are used when the device is in MCU mode. When in GCI mode, MCU/GCI = 0, the MC145572 is controlled via the C/I and monitor channels, and it is not necessary to access the registers in normal applications.

The MC145572 provides a Parallel Control Port interface mode that provides access to all control registers.

The register map for the MC145572 is nearly identical to that for the MC145472 after a hardware or software reset. Reserved bits in the MC145472 register map have been redefined to permit access to new registers in the MC145572. Most software developed for the MC145472 will work for the MC145572 without modifications.

The MC145572 Serial Control Port (SCP) Interface is pin–for–pin identical to that of the MC145474/75 S/T–Interface Transceiver. Using the same interface as the MC145474/75 provides a common interface for applications utilizing both the MC145572 and the MC145474/75 and for applications that can use either device, such as line cards or terminal equipment.

In addition to being pin–for–pin compatible, the architecture of the register map and the SCP Interface is nearly identical to that of the MC145474/75. This simplifies the code development effort and minimizes device driver code size for the microcontroller.

Table 6. Nibble Registers and R6 Map (NR0 – NR5; R6)

	b3	b2	b1	b0
NR0	SOFTWARE RESET	POWER DOWN ENABLE	ABSOLUTE POWER DOWN	RETURN TO NORMAL
NR1	LINKUP	ERROR INDICATION	SUPERFRAME SYNC	TRANSPARENT/ ACTIVATION IN PROGRESS
NR2	ACTIVATION REQUEST	DEACTIVATION REQUEST	SUPERFRAME UPDATE DISABLE	CUSTOMER ENABLE
NR3	IRQ3	IRQ2	IRQ1	IRQ0
NR4	ENABLE IRQ3	ENABLE IRQ2	ENABLE IRQ1	ENABLE IRQ0
NR5	RESERVED	BLOCK B1	BLOCK B2	SWAP B1/B2

	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R6	eoc a1	eoc a2	eoc a3	eoc dm	eoc i1	eoc i2	eoc i3	eoc i4	eoc i5	eoc i6	eoc i7	eoc i8

Table 7. Byte Register Map (BR0 – BR15A)

	b7	b6	b5	b4	b3	b2	b1	b0
BR0	M40	M41	M42	M43	M44	M45	M46	M47
BR1	M40	M41	M42	M43	M44	M45	M46	M47
BR2	M50	M60	M51	febe INPUT	RESERVED	RESERVED	RESERVED	RESERVED
BR3	M50	M60	M51	RECEIVED febe	COMPUTED nebe	VERIFIED act	VERIFIED dea	SUPERFRAME DETECT
BR4	febe COUNTER 7	febe COUNTER 6	febe COUNTER 5	febe COUNTER 4	febe COUNTER 3	febe COUNTER 2	febe COUNTER 1	febe COUNTER 0
BR5	nebe COUNTER 7	nebe COUNTER 6	nebe COUNTER 5	nebe COUNTER 4	nebe COUNTER 3	nebe COUNTER 2	nebe COUNTER 1	nebe COUNTER 0
BR6	U–LOOP B1	U–LOOP B2	U–LOOP 2B + D	U–LOOP TRANSPAR-ENT	IDL2–LOOP B1	IDL2–LOOP B2	IDL2–LOOP 2B + D	IDL2–LOOP TRANSPARENT
BR7	BR15A SELECT	**GCI IN2** / **OUT2**	**GCI IN1** / **OUT1**	IDL2 INVERT	IDL2 FREE RUN	IDL2 SPEED	IDL2 M/S INVERT	IDL2 8/10
BR8	FRAME STEERING	FRAME CONTROL 2	FRAME CONTROL 1	FRAME CONTROL 0	crc CORRUPT	MATCH SCRAM-BLER	RECEIVE WINDOW DISABLE	NT/LT INVERT
	FRAME STATE 3	FRAME STATE 2	FRAME STATE 1	FRAME STATE 0	RESERVED	RESERVED	RESERVED	NT/LT MODE
BR9	eoc CONTROL 1	eoc CONTROL 0	M4 CONTROL 1	M4 CONTROL 0	M5/M6 CONTROL 1	M5/M6 CONTROL 0	febe/nebe CONTROL	RESERVED
BR11	ACTIVATION CONTROL 6	ACTIVATION CONTROL 5	ACTIVATION CONTROL 4	ACTIVATION CONTROL 3	ACTIVATION CONTROL 2	ACTIVATION CONTROL 1	ACTIVATION CONTROL 0	ACTIVATION TIMER DISABLE
	ACTIVATION STATE 6	ACTIVATION STATE 5	ACTIVATION STATE 4	ACTIVATION STATE 3	ACTIVATION STATE 2	ACTIVATION STATE 1	ACTIVATION STATE 0	ACTIVATION TIMER EXPIRE
BR12	ACTIVATION CONTROL STEER	INTERPO-LATE ENABLE	LOAD ACTIVATION STATE	STEP ACTIVATION STATE	HOLD ACTIVATION STATE	JUMP SELECT	RESERVED	FORCE LINKUP
	EPI 18	EPI 17	EPI 16	EPI 15	EPI 14	EPI 13	EPI 12	EPI 11
BR13	ENABLE MEC UPDATES	ACCUM EC OUTPUT	ENABLE EC UPDATES	FAST EC BETA	ACCUM DFE OUTPUT	ENABLE DFE UPDATES	FAST DFE/ARC BETA	CLEAR ALL COEFF'S
	EPI 10	EPI 9	EPI 8	EPI 7	EPI 6	EPI 5	EPI 4	EPI 3
BR14	RESERVED	ro/wo TO r/w	RESERVED	FRAMER TO DEFRAMER LOOP	± 1 TONES	RESERVED	RESERVED	ENABLE CLKs
BR15	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	MASK 7	**MASK 6**	**MASK 5**	MASK 4	MASK 3	MASK 2	MASK 1	MASK 0
BR15A	FREQ ADAPT	JUMP DISABLE	RESERVED	RESERVED	ENABLE Tx SFS	RESERVED	RESERVED	EYE DATA ENABLE
				RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

NOTE: Bits in bold type were reserved bits in the MC145472/MC14LC5472 register map.

Table 8. Overlay Register Map (OR0 – OR13)

INIT GROUP REGISTER OVERLAY REGISTERS OR0 – OR9, OR11, AND OR12								
	b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
OR0	D_{out} B1 CHANNEL TIME SLOT BITS (7:0)							
OR1	D_{out} B2 CHANNEL TIME SLOT BITS (7:0)							
OR2	D_{out} D CHANNEL TIME SLOT BITS (7:0)							
OR3	D_{in} B1 CHANNEL TIME SLOT BITS (7:0)							
OR4	D_{in} B2 CHANNEL TIME SLOT BITS (7:0)							
OR5	D_{in} D CHANNEL TIME SLOT BITS (7:0)							
						GCI Slot (2:0)		
OR6	TSA B1 ENABLE	TSA B2 ENABLE	TSA D ENABLE	GCI SELECT M4–OR0	GCI MODE ENABLE	RESERVED	RESERVED	RESERVED
OR7	RESERVED	RESERVED	TSEN DCH ENABLE	IDL2 RATE2	IDL2 LONGFRAME MODE	CRC CORRUPT MODE	febe/nebe ROLLOVER	M4 TRINAL MODE
OR8	D/R MODE 1	D/R MODE 0	SFAX OUTPUT ENABLE	FREQREF OUTPUT ENABLE	TSEN ENABLE B1, B2	RESERVED	SFAX SFAR ENABLE	D CHANNEL PORT ENABLE
OR9	RESERVED	OPEN FEEDBACK SWITCHES	ANALOG LOOPBACK	CLKOUT 2048	4096 HIRATE	2048 DISABLE	1536 DISABLE	4096 DISABLE
BR10	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	**SELECT DUMP ACCESS**	**SELECT DCH ACCESS**	**SELECT INIT GROUP**
D CHANNEL ACCESS SELECT OVERLAY								
OR12	D CHANNEL TRANSMIT BITS (7:0)							
	D CHANNEL RECEIVE BITS (7:0)							
DUMP/RESTORE ACCESS SELECT OVERLAY								
OR13	DUMP REGISTER WRITE ACCESS (7:0)							
	DUMP REGISTER READ ACCESS (7:0)							

IDL2 TIME DIVISION BUS INTERFACE

The IDL2 Interface consists of six pins: M/$\overline{S}$, FSX, FSR, DCL, D_{in}, and D_{out}. With the M/S pin, the IDL2 Interface can be configured as a timing Master (FSR, FSX, and DCL are outputs) or a timing Slave (FSR, FSX, and DCL are inputs). Master or Slave configuration is independent of NT or LT mode selection. The IDL2 Interface receives 2B+D data on the D_{in} pin and buffers it through a FIFO to the U–Interface Superframe Framer. Simultaneously, this block accepts 2B + D data from the U–Interface Superframe Deframer, buffers it through a FIFO, and transmits it out the D_{out} pin. Refer to Figure 5 for a block diagram of the MC145572.

2B+D Data is transferred over the IDL2 interface at an 8 kHz rate. Each IDL2 2B+D frame contains 8 bits of B1 channel data, 8 bits of B2 channel data, and 2 bits of D channel data. The IDL2 interface supports five different frame formats and a time slot assigner. The frame formats are long frame and short frame synchronization each with either 8–bit or 10–bit 2B+D data formats. The fifth frame format is the IDL2 GCI Electrical frame format. In this format only the 2B+D data bits of the GCI interface are accessible by the MC145572. Either the Serial Control Port or the Parallel Control Port must be used for access to the internal register set of the MC145572 when IDL2 operation is enabled.

SHORT FRAME OPERATION

Short frame operation is the same as the IDL interface used on the MC145472 and MC14LC5472 U–Interface Transceivers with one exception. The MC145572 provides for two 8 kHz frame sync pins, FSX and FSR, when operated in IDL2 mode. The FSX pin is used to indicate IDL2 frame synchronization for data input into the D_{in} pin for transmission onto the U–Interface. The FSR pin is used to indicate IDL2 frame synchronization for data recovered from the U–Interface and output to the D_{out} pin. When configured for master mode, the MC145572 drives FSR and FSX simultaneously. When configured for IDL2 slave operation, the MC145572 FSX and FSR inputs can be driven independently. In slave mode, both FSX and FSR can be connected together so a single synchronization signal can be used to drive both inputs.

LONG FRAME OPERATION

When configured for long frame mode the 8 kHz frame sync is active during the 2B+D data transfer. The FSX pin is

used to indicate frame synchronization for data input into the D_{in} pin for transmission onto the U–Interface. The FSR pin is used to indicate frame synchronization for data recovered from the U–Interface and output to the D_{out} pin. When configured for master mode, the MC145572 drives FSR and FSX simultaneously. When configured for IDL2 slave operation, the MC145572 FSX and FSR inputs can be driven independently. In slave mode, both FSX and FSR can be connected together so a single synchronization signal can be used to drive both inputs.

GCI 2B+D OPERATION

By setting OR6(b3), GCI Mode Enable, to a '1' the IDL2 interface is configured to accept GCI interface timing. In this mode only 2B+D data is transferred between the MC145572 and the GCI interface. The other bits in the GCI frame are ignored. Four signal pins are available in this mode: DCL, FSC, D_{in}, and D_{out}. Control and status information for the MC145572 is provided through the Serial Control Port or the Parallel Control Port. DCL is a 2X bit clock, D_{in} accepts data from the IDL2 interface to be transmitted onto the U–Interface, D_{out} transmits data received from the U–Interface onto the IDL2 interface, and FSC is the 8 kHz frame synchronization pulse. D_{out} is driven only when 2B+D data is output from the MC145572. During all other bit times of the GCI frame D_{out} is high impedance. For applications having a multiplexed GCI frame structure, overlay register OR5 bits 2:0 are used to program the active GCI channel in the multiplex.

MCU MODE ACTIVATION AND DEACTIVATION

Activation or start–up is the process U–Interface Transceivers use to initiate a robust full–duplex communications channel. This process, which may be initiated from either the LT or the NT mode U–Interface Transceiver, is a well–defined sequence of procedures during which the training of the equalizers and echo cancelers at each end of the transmission line takes place. Two types of activation, cold start or warm start, may occur. The MC145572 is capable of automatically supporting both types.

Deactivation is the process used to gracefully end communication between the U–Interface Transceivers at each end of the transmission line. Only the LT mode U–Interface Transceiver may initiate a deactivation procedure.

ACTIVATION SIGNALS FOR NT MODE

When configured as an NT, the MC145572 U–Interface Transceiver can transmit any of the signals shown in Table 9.

ACTIVATION SIGNALS FOR LT MODE

When configured as an LT, the MC145572 U–Interface Transceiver can transmit any of the signals shown in Table 10.

ACTIVATION INITIATION

The MC145572 U–Interface Transceiver can be activated in either of two ways. The external microcontroller can explicitly issue Activation Request (NR2(b3) = 1) or the transceiver detects an incoming 10 kHz wake–up tone. An LT configured U–Interface Transceiver searches for an NT sending the TN wake–up tone. An NT configured U–Interface Transceiver searches for an LT sending the TL wake–up tone. In IDL2 mode the Activation in Progress status bit (NR1(b0)) is set to a 1 when an incoming 10 kHz wake–up tone is detected. In either case, Activation Request being set or a wake–up tone being detected, the U–Interface Transceiver proceeds with activation automatically and signals the result of the activation to the external microcontroller by setting status bits in NR1 to $B.

Table 9. NT Mode Activation Signals

Information Station	Description
TN	A 10 kHz tone consisting of alternating four +3 quats followed by four –3 quats for a time period of 6 frames.
SN0	No signal transmitted.
SN1	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SN2	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SN3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when `act` n M4 bit = 1. When `act` n M4 = 0, transmitted 2B+D data = 1.

Table 10. LT Mode Activation Signals

Information Station	Description
TL	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of 2 frames.
SL0	No signal transmitted.
SL1	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SL2	Synchronization word present, superframe synchronization word (ISW) present, 2B+D = 0, and M = Normal.
SL3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when M4 `act` bit = 1. When M4 `act` = 0, transmitted 2B+D data = 0.

NT DEACTIVATION PROCEDURES AND WARM START

ANSI T1.601 specifies that the NT cannot initiate deactivation. The MC145572 deactivates to a warm start condition when Deactivation Request (NR2(b2)) is set to 1 prior to the LT deactivating the U–Interface. This should be done in response to the M4 channel dea bit being received as 0 by the NT when the loop is active. If Deactivation Request (NR2(b2)) is not set to 1 before the LT deactivates the U–Interface, the MC145572 deactivates to a cold start condition and gives an error indication interrupt. Deactivation Request is automatically set if the M4 maintenance bits are operated with automatic verification of activation and deactivation. See BR9(b5:b4) and OR7(b0) for more information.

LT DEACTIVATION PROCEDURES

ANSI T1.601 specifies that only the LT can deactivate the U–Interface. This is done in the MC145572 by setting Deactivation Request (NR2(b2)) to 1.

Prior to deactivating, the LT should notify the NT of the pending deactivation by clearing the M4 channel dea bit towards the NT for at least three superframes. Then, deactivate the LT by setting Deactivation Request (NR2(b2)) to a 1.

MCU MODE MAINTENANCE CHANNEL OPERATION

When configured for MCU mode operation the MC145572 provides a very flexible interface to the 4 kbps maintenance channel (M–channel) defined in ANSI T1.601–1992. The M–channel consists of 48 bits sent by both the LT and NT configured U–Interface Transceivers during the course of a superframe. These 48 bits are divided into six subchannels designated M1 through M6, each consisting of eight bits per superframe. The Embedded Operations Channel (eoc) consists of M1, M2, and M3. The overhead bits, such as crc, febe, act, and dea, are contained in subchannels M4, M5, and M6.

An external microcontroller can read from or write to the M–channel via the SCP or PCP Interfaces. Interrupts to an external microcontroller can be enabled when an eoc, M4, M5, or M6 channel register is updated. M–channel registers can be configured to update when a new value is detected between successive superframes, when a bit changes, or when two or three successive superframes of a new value are detected. The M4 channel act bit, BR1(b7), can also be configured to automatically enable or disable customer data when in NT or LT mode of operation. The M4 channel dea bit, BR1(b6), can also be configured to automatically issue a deactivation request in NT mode of operation. The M–channel registers are updated only when Superframe Sync, NR1(b1), is set to 1.

GCI MODE FUNCTIONAL DESCRIPTION

The MC145572 is configurable for General Circuit Interface or GCI operation. GCI is a time divison multiplex bus that combines the ISDN 2B+D data and control/status information onto four signal pins. There are two clocks per data bit and a single frame synchronization pulse, FSC.

In GCI mode the MC145572 supports the full set of commands and indications over the Command/Indicate channel. The monitor channel is used for sending and receiving maintenance channel messages and accessing the internal MC145572 registers.

As a GCI slave the MC145572 accepts clock frequencies between 512 kHz and 8.192 MHz. As a GCI master the MC145572 operates at either 512 kHz or 2.048 MHz. Figure 8 is a typical configuration for the MC145572 in GCI mode. The MC145572 is configured for GCI operation when the MCU/GCI pin is tied low. The PAR/SER pin is a don't care but must be tied either high or low.

Table 11. C/I Channel Commands and Indications

C/I Codeword				LT Mode	LT Mode	NT Mode	NT Mode
b4	b3	b2	b1	Command	Indication	Command	Indication
0	**0**	0	0	**DR**	**–**	**–**	**DR**
0	**0**	0	1	**RES**	**DEAC**	**RES**	**–**
0	**0**	1	0	**LTD2**	**–**	**NTD2**	**–**
0	**0**	1	1	**LTD1**	**–**	**NTD1**	**–**
0	**1**	**0**	**0**	**–**	**RSY**	**–**	**RSY**
0	**1**	**0**	**1**	**–**	**EI2**	**–**	**EI2**
0	**1**	**1**	**0**	**–**	**–**	**–**	**–**
0	**1**	**1**	**1**	**UAR**	**UAI**	**–**	**–**
1	**0**	0	0	**AR**	**AR**	**AR**	**AR**
1	**0**	0	1	**–**	**–**	**–**	**–**
1	**0**	1	0	**ARL**	**–**	**–**	**ARL**
1	**0**	1	1	**–**	**–**	**–**	**–**
1	**1**	**0**	**0**	**–**	**AI**	**AI**	**AI**
1	**1**	**0**	**1**	**–**	**–**	**–**	**–**
1	**1**	**1**	**0**	**–**	**–**	**–**	**AIL**
1	**1**	**1**	**1**	**DC**	**DI**	**DI**	**DC**

NOTES:

AI Activation indication
ARL Activation request with local analog loopback
DEAC Deactivation request accepted
DR Deactivation request
LTD1 (LT mode), NTD1 (NT mode) Sets pin “OUT1” high when command is active.
RES Reset
UAI U–Only activation indication
AR Activation request
DC Deactivation confirm
DI Deavtivation indication
EI2 Error indication
LTD2 (LT mode), NTD2 (NT mode) Set pin “OUT2” high when command is active.
RSY Loss of sync – resync. requested
UAR U–Only activation request

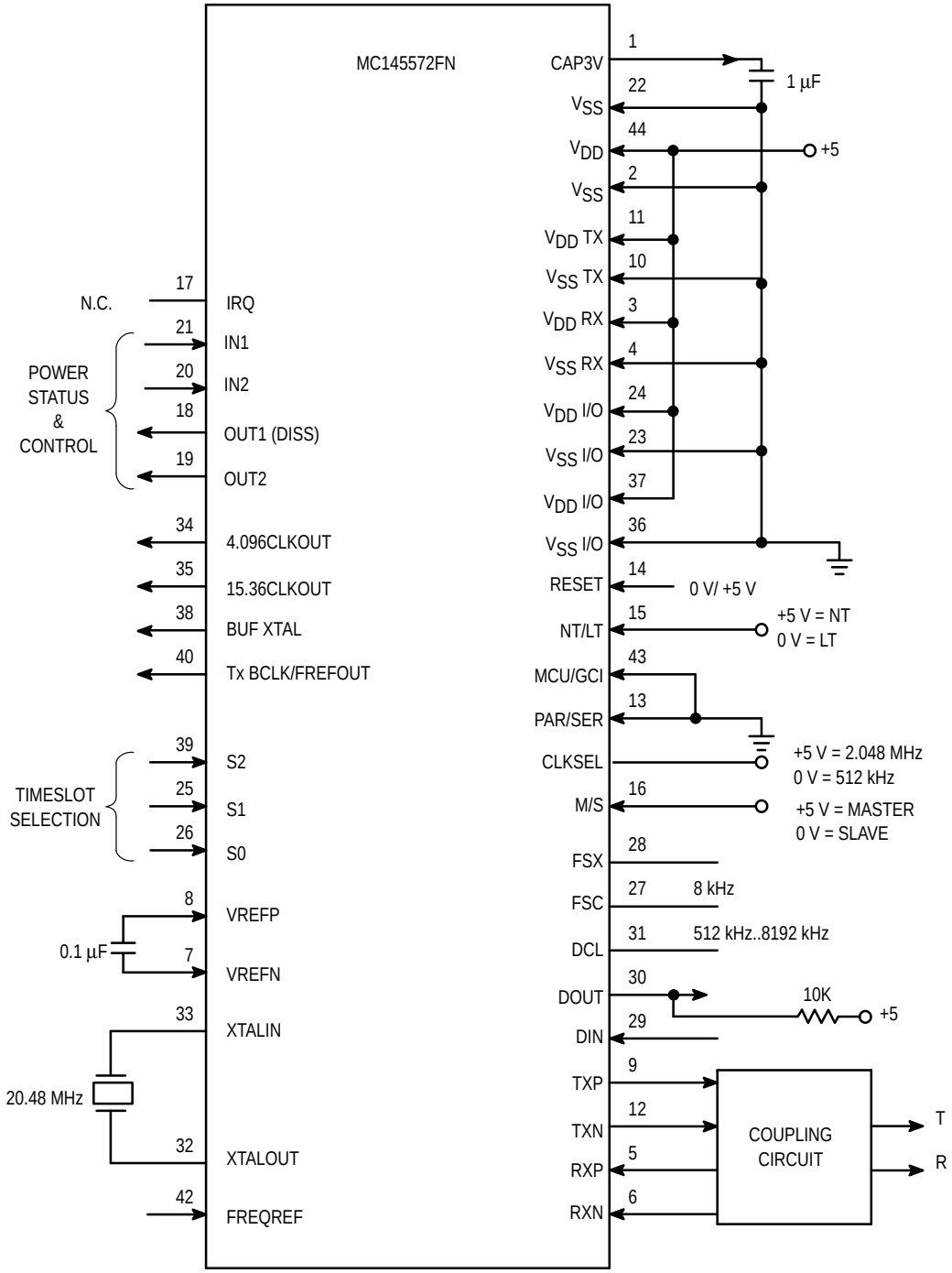


Figure 8. MC145572 Configuration for GCI Operation