MC145537EVK

Advance Information

MC14LC5540 ADPCM Codec Evaluation Kit

The MC145537EVK is the evaluation platform for the MC14LC5540 ADPCM Codec. This board provides the clock generator circuitry and microcontroller interface to facilitate the evaluation of the MC14LC5540.

MC145537EVK Hardware Features

- Supports MC14LC5540 + 5 V or + 3 V Operation
- Handset Interface/Handset Included
- Easy Access to All Analog and Digital Data, Clock, and Enable Signals
- EIA–232–D/ V.28 Terminal Control
- Analog–to–Digital (64 kbps PCM; 32, 24, or 16 kbps ADPCM) Path
- Digital– (64 kbps PCM; 32, 24, or 16 kbps ADPCM) to–Analog Path
- Supports Hardware Loopbacks
  - Analog–to–Analog
  - Digital–to–Digital
- Ability to Connect Two MC145537EVKs Back–to–Back
- Ability to Connect MC145537EVK and MC145536EVK Back–to–Back for + 5 V Operation Only

MC145537EVK Software Features

- MC68HC705C8 Resident Monitor
- Stand Alone or Terminal Operation
- Device Driver for Serial Control Port Interface
- Ability to Read/Write SCP Registers in MC14LC5540
- Registers Can Be Individually Displayed and Modified
- Help Menu

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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GENERAL OVERVIEW

The MC14LC5540 ADPCM Codec is a single–chip implementation of a PCM Codec–Filter and an ADPCM Encoder/Decoder, and therefore provides an efficient solution for applications requiring the digitization and compression of voiceband signals. This device is designed to operate over a wide voltage range, 2.7 to 5.25 V, and as such is ideal for battery powered as well as ac powered applications. The MC14LC5540 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcomputer to exercise many built–in features.

The MC14LC5540 ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721 and ANSI T1.301. It also meets ANSI T1.303 and CCITT Recommendation G.723 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard, CCITT Recommendation G.726. This device also meets the 64 kbps PCM conformance specification of the CCITT G.714 Recommendation.

The MC145537EVK is the evaluation board for the MC14LC5540 ADPCM Codec. This board provides the clock generation that controls both the transfer of PCM and ADPCM data into and out of the MC14LC5540, as well as determining the data compression rate (16 kbps ADPCM, 24 kbps ADPCM, 32 kbps ADPCM, or 64 kbps PCM) for the ADPCM transcoder function. This data compression rate is determined by the duration of the transmit and receive frame synchronization pulses measured in data clock cycles, which are programmed by an 8–position DIP switch. This evaluation board has voltage level shifters that allow the MC14LC5540 to operate at a voltage lower than the + 5 V supply required for the clock generator and microcontroller.

This MC145537EVK has an MC68HC705C8P microcontroller, which is running a monitor routine that interfaces the MC14LC5540 to a 9600 bps EIA–232 port for access by a computer terminal. The microcontroller provides access to the programming registers of the MC14LC5540 for read and write operations. This facilitates exercising both the hardware options for trim gain, sidetone, analog signal routing and charge–pump operation, and the software options of the dual tone generator, noise burst detect and receive gain control. The evaluation board is designed to configure the MC14LC5540 after reset such that the charge–pump is operating and the device is encoding and decoding analog at the rate determined by the clock circuitry. This allows the MC145537EVK to be functional without a computer terminal.

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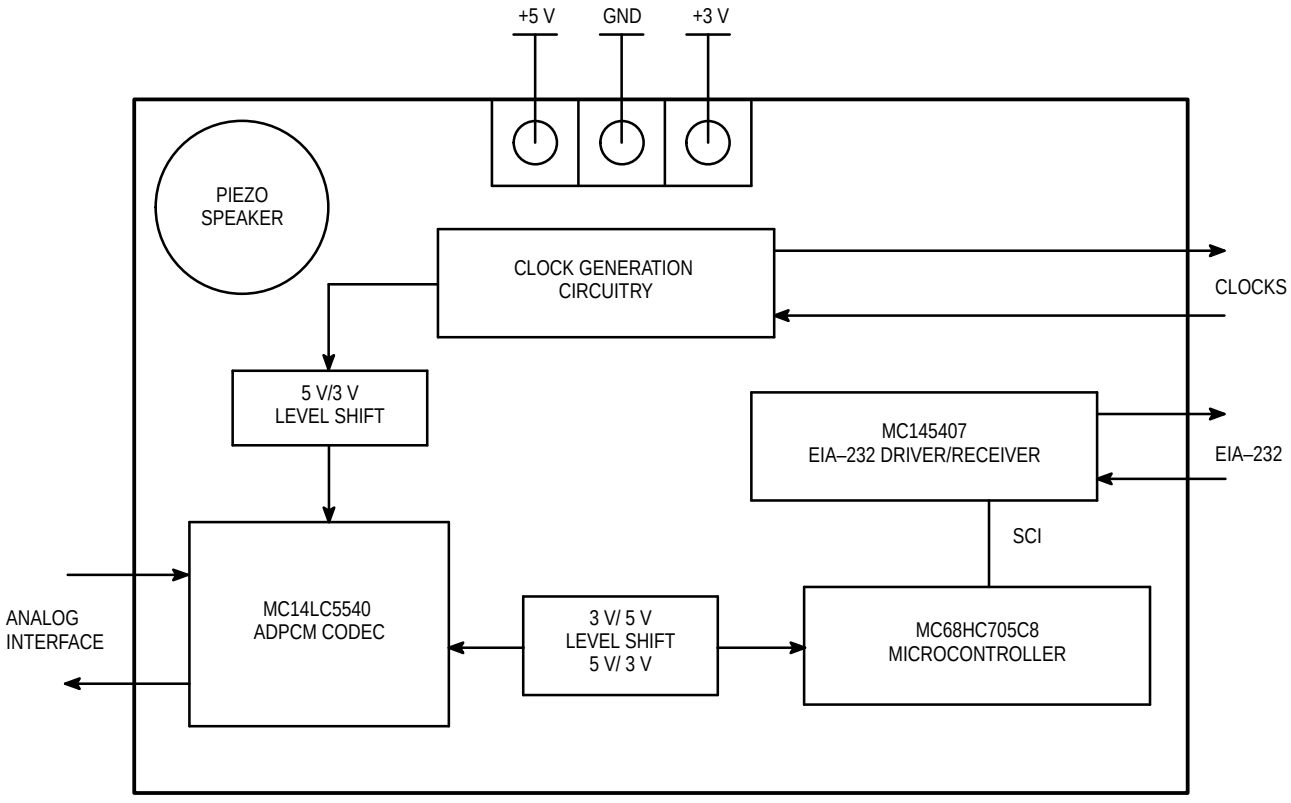

Figure 1. MC145537EVK Block Diagram

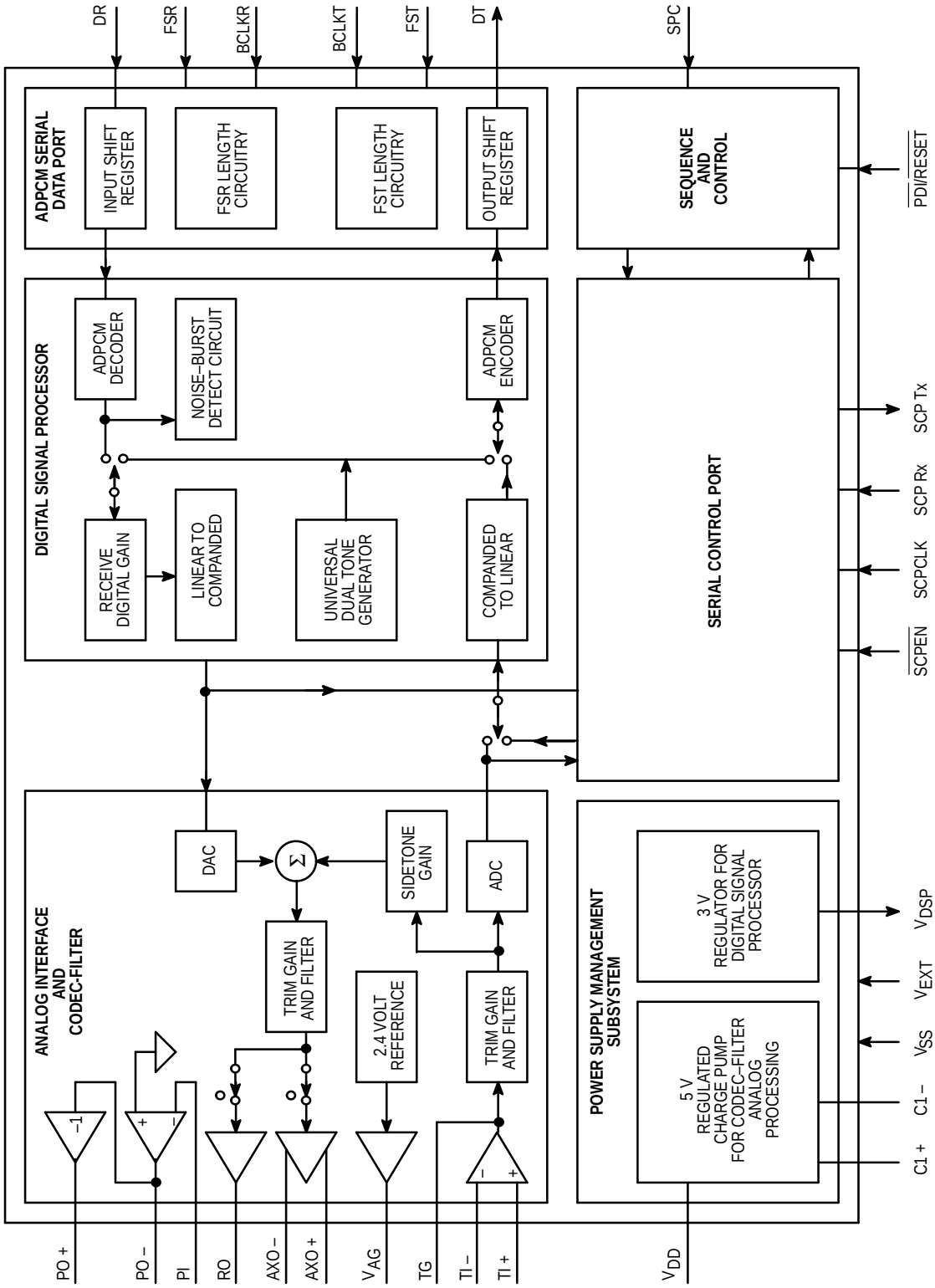

Figure 2. MC14LC5540 ADPCM Codec Block Diagram