MC145472
MC14LC5472

Technical Summary
U-Interface Transceiver

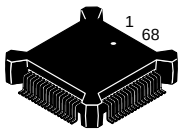
This technical summary provides a brief description of the MC145472 and MC14LC5472 U–Interface Transceivers. A complete data book for the MC145472 and MC14LC5472 is available and can be ordered from your local Motorola sales office. The data book number is MC145472/D.

The MC145472 U–Interface Transceiver is a single chip device intended for the ISDN Basic Access Interface and conforms to the American National Standard known as ANSI T1.601–1992. The MC145472 can be configured for LT or NT applications and performs all necessary Layer 1 functions while utilizing 2B1Q line coding.

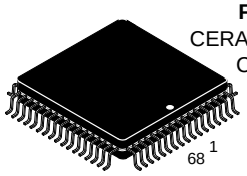
The customer data crossing the U Reference Point consists of two 64 kbps B channels and one 16 kbps D channel in each direction. This data is input to and output from the MC145472 via the industry standard Interchip Digital Link (IDL).

The MC145472 can operate in many different modes. The control of these various modes is provided via special purpose pins and the Serial Control Port (SCP). The SCP conforms to the Motorola Serial Peripheral Interface standard, an industry standard serial microprocessor interface.

The MC14LC5472 supercedes the MC145472. The MC14LC5472 has 500 mW power consumption when activated. In all other respects, it is the same as the MC145472. In this technical summary, MC145472 and MC14LC5472 are used interchangeably.



FU SUFFIX
PQFP
CASE 847

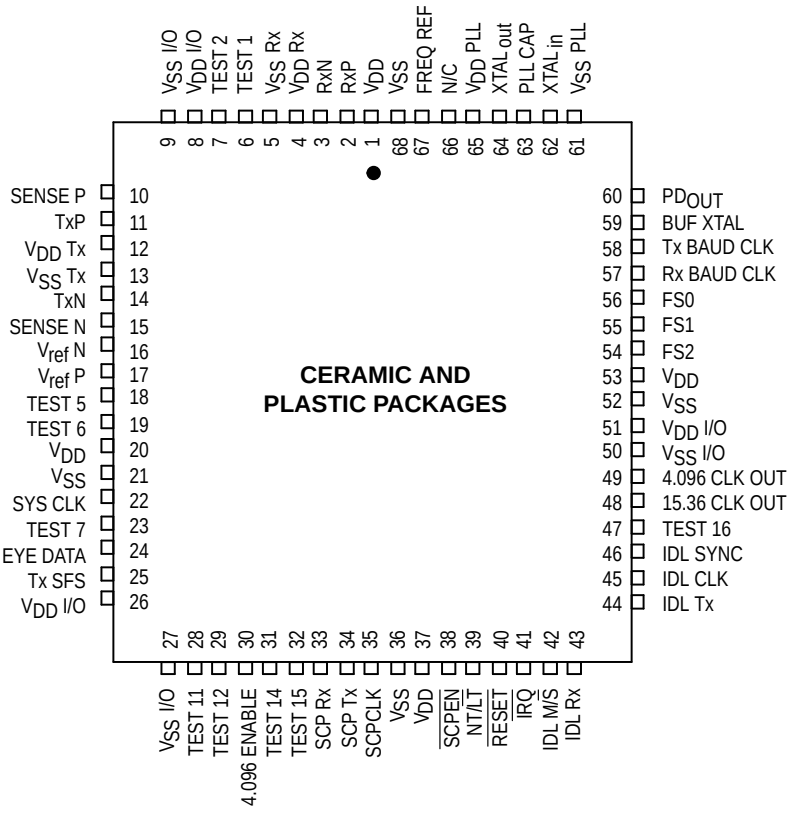


FE SUFFIX
CERAMIC PACKAGE
CASE 847B

ORDERING INFORMATION

MC145472FE	Ceramic Package
MC14LC5472FE	Ceramic Package
MC14LC5472FU	PQFP

PIN ASSIGNMENT



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Also, the MC14LC5472 is available in a 68–lead Plastic Quad Flat Package (PQFP). Both the MC145472 and MC14LC5472 are available in a 68–lead Ceramic Quad Flat Package. The 68–lead PQFP for the MC14LC5472 has a considerably smaller printed circuit board footprint than the 68–lead Ceramic Quad Flat Package. This permits more MC14LC5472s to be placed on a circuit board than would be the case if the MC145472 was used.

Information regarding the generic 2B1Q U–Interface requirement is readily available in standards documents such as ANSI T1.601–1992 and therefore has not been included in this document. The U–Interface equipment designer will find the ANSI document to be a useful reference.

Key features of the MC14LC5472 U–Interface Transceiver include:

- Single Chip 2B1Q Echo Canceling Adaptively Equalized Transceiver
- Conforms to ANSI T1.601–1992, Integrated Services Digital Network (ISDN) Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification) of the American National Standards Institute, Inc.
- Warm Start Capability
- NT Synchronizes to and Operates with 80 kHz ± 32 ppm Received Signal from LT
- IDL Interface Supports Master, Slave, and Slave–Slave Timing Modes
- On–Chip FIFOs for Transmit and Receive Directions
- MC14LC5472 Power Consumption is 500 mW Maximum When Activated
- 2B + D Customer Data Provided by the Industry Standard IDL Interface
- Control, Status, and Extended Maintenance Functions Provided through the SCP
- On–Chip Conformance with Activation and Deactivation as Specified in the American National Standard T1.601
- Automatic Handling of Basic Maintenance Functions
- Automatic Internal Compliance with the Embedded Operations Channel (eoc) Protocol as Specified in the American National Standard
- Extended Maintenance Functions Provided through the SCP
- Complete Set of Loopbacks for Both the IDL and U Reference Point Directions
- Pin Selectable for Line Termination (LT) or Network Termination (NT) Applications
- On–Chip 2.5 V Transmit Driver Meeting 1992 Requirement
- Eight Different Choices of Reference Frequency Input in LT Mode
- High Performance CMOS Process Technology
- 5 V Power Supply
- The MC14LC5494EVK is the Evaluation Platform for the MC14LC5472

ISDN BASIC ACCESS SYSTEM OVERVIEW

ISDN Reference Model

The ISDN Reference Model is shown in Figure 1. This is a general model which can be adapted to many different implementations of the ISDN. The diagram indicates the position of the U Reference Point between the Line Termination (LT) and the Network Termination 1 (NT1) blocks in the model.

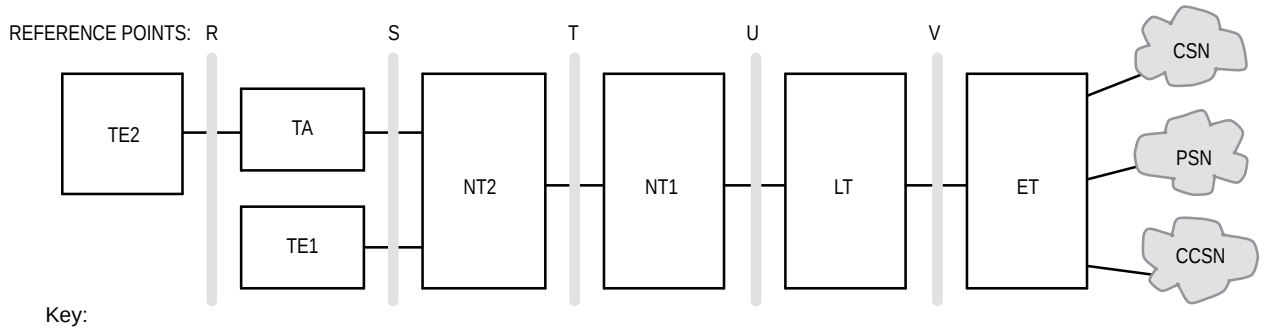
The U–Interface is the physical point of access to the ISDN at the U Reference Point defined in the Reference Model. This interface is a single twisted wire pair supporting full–duplex transmission of digital information at a rate of 160 kbps. The twisted wire pair can extend up to 18,000 feet and may include bridge taps. This interface is often referred to as a Digital Subscriber Line.

U–Interface Transceiver Applications

Some typical ISDN applications of the MC145472 U–Interface Transceiver are shown in Figure 2. This figure shows how Motorola ISDN devices can be configured with other Motorola MCUs and Codecs to implement ISDN equipment such as terminal adapters, NT1s, terminal equipment, line cards, and U–Interface terminals.

A typical non–ISDN pair gain application is shown in Figures 3 and 4. Pair gain is a technique to multiplex two or more analog phone lines over a digital line and recreate them at the customer location.

Figure 5 details how to connect two MC145472 U–Interface transceivers as a U–Repeater.



Key:

CCSN:	Common Channel Signalling Network	NT2:	Network Termination 2 (OSI Layers 2 and 3)
CSN:	Circuit Switched Network	PSN:	Packet Switched Network
ET:	Exchange Termination (C.O. Switch)	TA:	Terminal Adapter
LT:	Line Termination (Line Card)	TE1:	Terminal Equipment 1 (ISDN Terminal)
NT1:	Network Termination 1 (OSI Layer 1 Only)	TE2:	Terminal Equipment 2 (Non–ISDN Terminal)

Figure 1. ISDN Reference Model

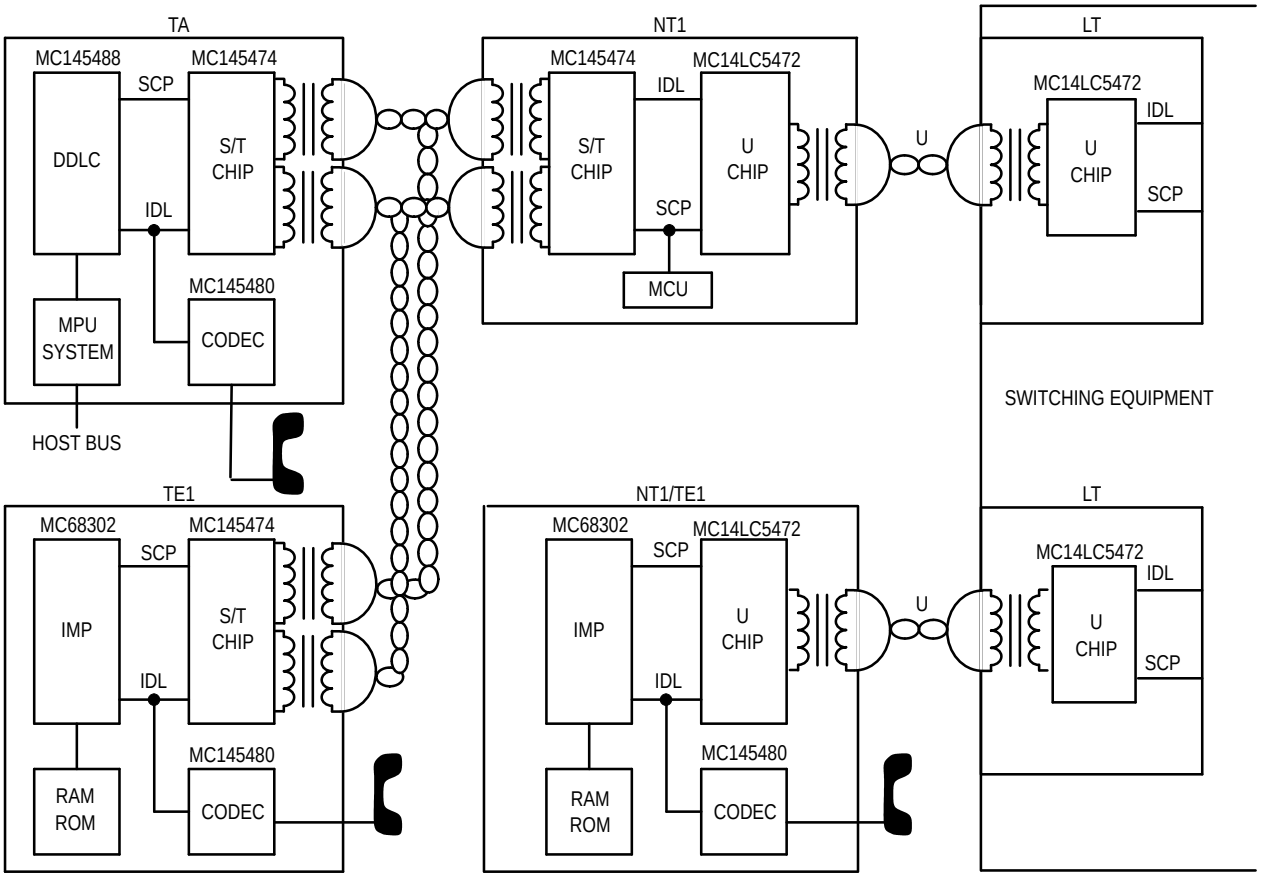


Figure 2. MC14LC5472 Typical ISDN Applications

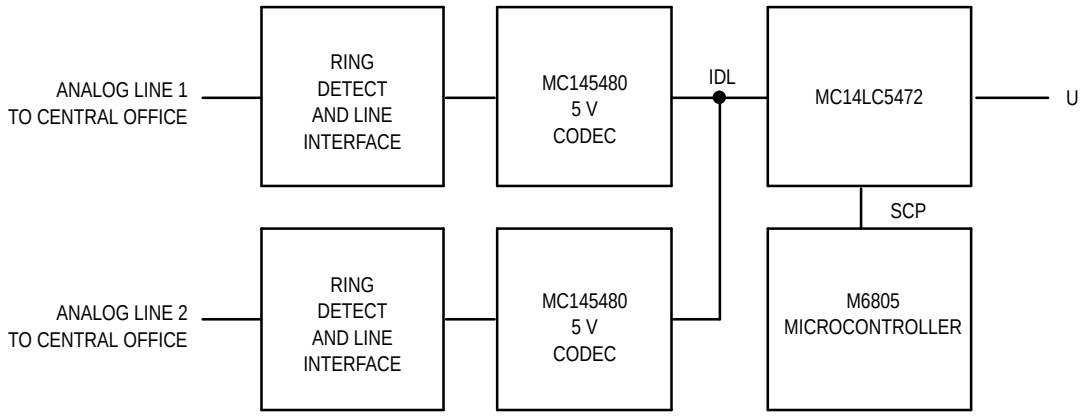


Figure 3. Pair Gain Application, Central Office Terminal

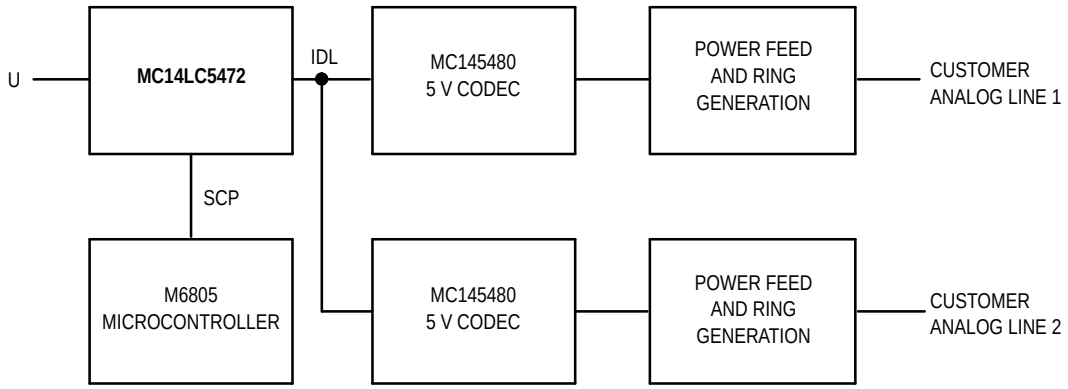
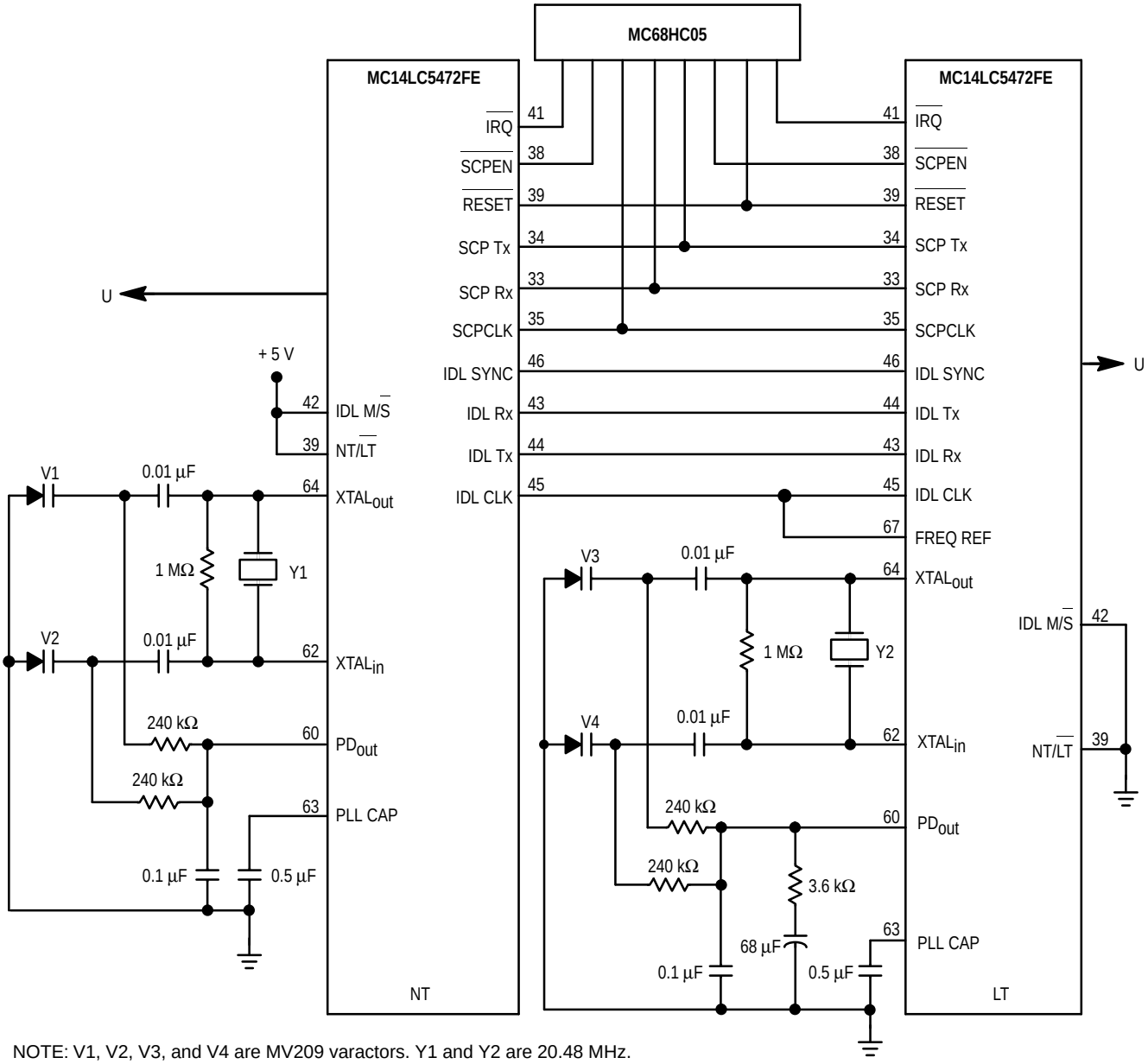


Figure 4. Pair Gain Application, Remote Terminal



NOTE: V1, V2, V3, and V4 are MV209 varactors. Y1 and Y2 are 20.48 MHz.

Figure 5. U Repeater Showing Clock and IDL Connections

DEVICE DESCRIPTION

FUNCTIONAL DESCRIPTION

A functional block diagram of the MC145472 U–Interface Transceiver is shown in Figure 6. The MC14572 utilizes mixed analog and digital signal processing circuit technology to implement an adaptively equalized echo canceling full–duplex transmitter/receiver or transceiver.

2B+D data is input to the device at the IDL Rx input. This data is passed through a FIFO prior to being formatted and scrambled in the Superframe Framer. The resulting 160 kbps binary data stream is converted to an 80 kbaud dibit stream which is subsequently converted to four analog amplitudes by the DAC (digital–to–analog converter). The resulting pulse amplitude modulated signal is band–limited by the Tx Filter prior to entering the Tx Driver which differentially drives the line coupling circuit to the twisted wire pair.

From the twisted wire pair, information from the far end U–Interface Transceiver is coupled through the external line interface circuit to the differential receiver inputs RxP and RxN. (In this two–wire environment, the transmitted signal is also coupled into the receiver inputs.) This combined analog signal is converted to a digital word in a sigma–delta, analog–to–digital converter. After filtering, an adaptively generated replica of the transmitted signal, calculated by the echo canceler, is subtracted from the combined signal leaving only the far end signal. In addition, phase dispersion present in the far end signal is corrected by the Decision Feedback Equalizer. The resulting four level signal is decoded by the slicer to produce a 160 kbps data stream. Timing information is also recovered from the far end signal. The Superframe Deframer descrambles and disassembles the received superframes and passes the received 2B+D data through a FIFO to the IDL Interface where it is available at the IDL Tx output.

Control and status of the device is handled via the SCP, a standard serial microcontroller interface. The SCP provides access to the 4 kbps Maintenance Channel in the U–Interface superframe. In addition, activation and deactivation are handled by an Automatic Activation Controller and the eoc portion of the M channel can be handled automatically with the Automatic eoc Processor.

A crystal oscillator and analog Phase–Locked Loop (PLL) are provided to ease clocking requirements for the device.

U–INTERFACE DATA FORMAT

The data transmitted on the U–Interface is organized into a 12 ms long superframe. This superframe consists of eight basic frames each of 1.5 ms in duration. The first nine bauds of each frame are a synchronization word. The next 108 bauds consists of 12 × 2B+D data. The last three bauds consist of maintenance channel data including a cyclic redundancy check. The first frame of the superframe is identified by its sync word being inverted.

The U–Interface Transceiver transmits a four level 2B1Q, (two binary, one quaternary), line code. Two bits are encoded into each baud. Each basic frame consists of 120 bauds or 240 bits of data. The baud symbols are called + 3, + 1, – 1, and – 3. The B and D channel data is scrambled before being transmitted. Figure 7 gives an example of the 2B1Q line code. Tables 1 and 2 detail the U–Interface superframe formats.

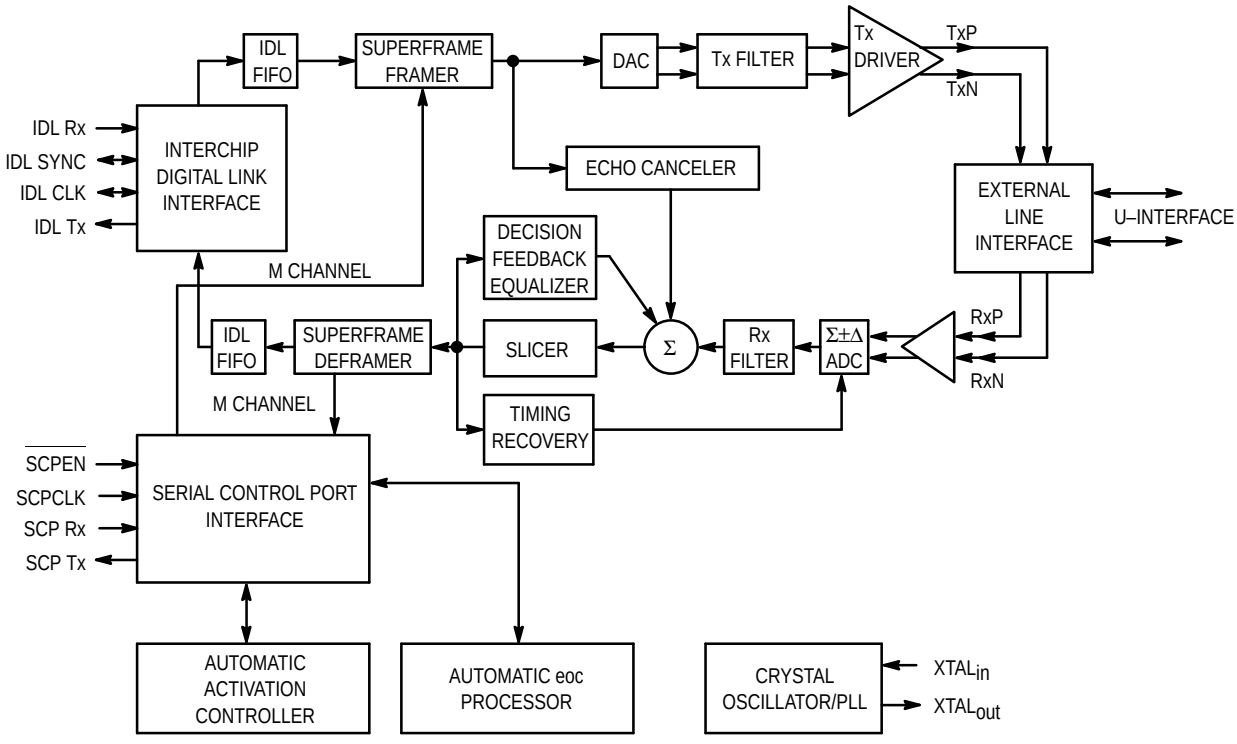


Figure 6. MC14LC5472 Functional Block Diagram

Table 1. Superframe Data Format, LT → NT

	Framing	2B+D	Overhead Bits (M – M6)					
QUAT Positions	1 – 9	10 – 117	118s	118m	119s	119m	120s	120m
Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Basic Frame #	**Sync Word**	**2B+D**	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	dea	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	1	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	1	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	1	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	uoa	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	aib	crc11	crc12

act = start up bit, set = 1 during start up
aib = alarm indication bit (set = 0 to indicate interruption)
crc = cyclic redundancy check: covers 2B+D + M4
dea = turn off bit (set = 0 to indicate turn off)
febe = far end block error
uoa = U–only–activation
1 = reserved bit for future standard (set = 1)
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
i = information bit

Table 2. Superframe Data Format, NT → LT

	Framing	2B+D	Overhead Bits (M1 – M6)					
QUAT Positions	1 – 9	10 – 117	118s	118m	119s	119m	120s	120m
Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Basic Frame #	**Sync Word**	**2B+D**	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	ps1	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	ps2	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	ntm	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	cso	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	sai	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	1	crc11	crc12

act = start up bit, set = 1 during start up.
crc = cyclic redundancy check: covers 2B+D + M4
cso = cold start only (set = 1 for cold start only)
febe = far end block error
ntm = NT in test mode bit (set = 0 to indicate test mode)
sai = S–active indicator bit (optional, set = 1 for S/T activity)
1 = reserved bit for future standard (set = 1)
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
i = information bit
ps1, ps2 = power status bits (set = 0 to indicate power problems)

PIN FUNCTIONALITY

Tables 3 through 7 list the MC145472 pins in functional groups and provide brief pin descriptions. For more detailed information, refer to the MC145472 data book.

MODE SELECTION

These pins are used to select the operating mode of the MC145472 U–Interface Transceiver.

The RESET pin is a Schmitt–trigger input and holds the MC145472 in a hardware reset condition when at logic 0.

The NT/LT input pin selects the operating mode of the MC145472. When at logic 1 the U–Interface Transceiver is in NT mode. When at logic 0 the U–Interface Transceiver is in LT mode.

Figures 8 and 9 show typical LT and NT mode connections, respectively.

INTERCHIP DIGITAL LINK (IDL) INTERFACE

The IDL Interface consists of five pins: IDL M/$\overline{S}$, IDL SYNC, IDL CLK, IDL Tx, and IDL Rx. With the IDL M/S pin the IDL Interface can be configured as an IDL Master (IDL SYNC and IDL CLK are outputs) or an IDL Slave (IDL SYNC and IDL CLK are inputs). The IDL Interface receives 2B+D data on the IDL Rx pin and buffers it through a FIFO to the Superframe Framer (See Figure 6). Simultaneously, this block accepts 2B + D data from the Superframe Deframer, buffers it through a FIFO, and transmits it out the IDL Tx pin. Figure 10 shows the IDL data formats.

Table 3. Quick Reference to Power Supply and Mode Selection Pins

Power Supply Pins		
Pin Name	**Pin No.**	**Pin Description**
V_{DD}	1, 20, 37, 53	Positive power supply, nominally + 5 V.
V_{SS}	21, 36, 52, 68	Negative power supply, nominally ground.
V_{DD} Rx	4	Positive power supply for analog receive circuits, nominally + 5 V.
V_{SS} Rx	5	Negative power supply for analog receive circuits, nominally ground.
V_{DD} Tx	12	Positive power supply for analog transmit circuits, nominally + 5 V.
V_{SS} Tx	13	Negative power supply for analog transmit circuits, nominally ground.
V_{DD} I/O	8, 26, 51	Positive power supply for input and output circuits, nominally + 5 V.
V_{SS} I/O	9, 27, 50	Negative power supply for input and output circuits, nominally ground.
V_{DD} PLL	65	Positive power supply for phase–locked loop circuits, nominally + 5 V.
V_{SS} PLL	61	Negative power supply for phase–locked loop circuits, nominally ground.
Mode Selection Pins		
Pin Name	**Pin No.**	**Pin Description**
RESET	40	Hardware reset when at a logic low, normal operation when at a logic high. This pin has a Schmitt–trigger input.
NT/$\overline{LT}$	39	Hardware selection of LT (logic low) and NT (logic high) operating mode.

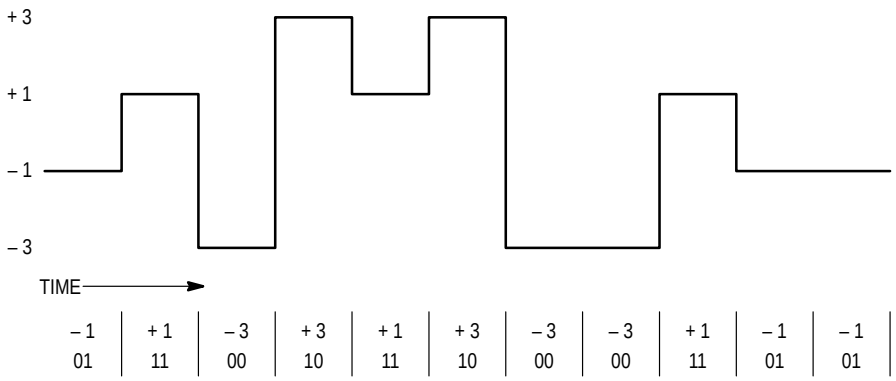


Figure 7. 2B1Q Line Code

Table 4. Quick Reference to IDL and SCP Pins

Interchip Digital Link (IDL) Interface Pins		
Pin Name	**Pin No.**	**Pin Description**
IDL M/S	42	Selects between IDL Master (IDL CLK and IDL SYNC are outputs) and IDL Slave (IDL CLK and IDL SYNC are inputs) modes. Logic high selects IDL Master mode and logic low selects IDL Slave mode.
IDL SYNC	46	8 kHz IDL frame synchronization input (IDL Slave mode) or output (IDL Master mode).
IDL CLK	45	Bit clock input (IDL Slave mode) or output (IDL Master mode) for serial transfer of 2B+D data at IDL Tx and IDL Rx.
IDL Tx	44	This is the IDL output for the 2B+D data.
IDL Rx	43	This is the IDL input for the 2B+D data.
Serial Control Port (SCP) Interface Pins		
Pin Name	**Pin No.**	**Pin Description**
SCPEN	38	SCP Enable Input held low selects the device for a read or write operation to the SCP.
SCPCLK	35	SCP Clock is an input which clocks the SCP data.
SCP Tx	34	SCP data output.
SCP Rx	33	SCP data input.
$\overline{\text{IRQ}}$	41	Open–drain output held low during an interrupt condition.

Table 5. Quick Reference to 2B1Q Interface Pins

2B1Q Interface Pins		
Pin Name	**Pin No.**	**Pin Description**
TxP	11	Positive output of the differential transmit driver.
TxN	14	Negative output of the differential transmit driver.
SENSE P	10	This pin senses the amplitude of the positive transmit driver output.
SENSE N	15	This pin senses the amplitude of the negative transmit driver output.
RxP	2	Positive input to the differential receive circuit.
RxN	3	Negative input to the differential receive circuit.
V_{ref} P	17	Positive input for off chip voltage reference. Connect a 0.1 μF ceramic capacitor between this pin and V_{ref} N.
V_{ref} N	16	Negative input for off chip voltage reference. Connect a 0.1 μF ceramic capacitor between this pin and V_{ref} P.
Tx BAUD CLK	58	This pin provides an 80 kHz clock output corresponding to the transmitted 2B1Q bauds.
Rx BAUD CLK	57	This pin provides an 80 kHz clock output corresponding to the received 2B1Q bauds.
EYE DATA	24	Once per received baud period, this pin outputs at a rate of 10.24 Mbps a serial digital word which represents the recovered 2B1Q signal or eye pattern.
SYS CLK	22	A 10.24 MHz clock output derived from the 20.48 MHz crystal oscillator which may be used to sample EYE DATA.
Tx SFS	25	Generates an output pulse once every transmitted superframe.

Table 6. Quick Reference to Phase–Locked Loop and Test Pins

Phase–Locked Loop and Clock Pins		
Pin Name	**Pin No.**	**Pin Description**
FREQ REF	67	In LT mode this input accepts one of eight possible stable input frequencies which is frequency multiplied to 20.48 MHz, the device's master clock frequency. Connect this pin high or low in NT mode. This pin has a Schmitt–trigger input.
FS0 FS1 FS2	56 55 54	The state of these three inputs indicates the frequency being applied to the FREQ REF pin. Connect these pins low or high in NT mode.
$XTAL_{in}$	62	This is the input of the 20.48 MHz crystal oscillator amplifier.
$XTAL_{out}$	64	This is the output of the 20.48 MHz crystal oscillator amplifier.
BUF XTAL	59	Buffered 20.48 MHz square wave output.
PD_{out}	60	Output of the PLL phase detector.
PLL CAP	63	Connect a 0.1 μF ceramic capacitor from this pin to ground.
15.36 CLK OUT	48	Buffered 15.36 MHz output.
4.096 CLK OUT	49	Buffered 4.096 MHz output.
4.096 ENABLE	30	When tied high this input enables the buffered 4.096 MHz clock output.

Table 7. Quick Reference to Test Pins

Test Pins		
Pin Name	**Pin No.**	**Pin Description**
TEST 5, 7, 11, 12, 14, 15, 16	18, 23, 28, 29, 31, 32, 47	Test pins for Motorola use. These pins should be connected to ground for normal operation.
TEST 1, 2, 6	6, 7, 19	Test pins for Motorola use. These pins should be left open circuit for normal operation.

The IDL interface can operate in IDL slave mode or IDL master mode. This is independent of the transceiver being in LT or NT mode. Normally, IDL slave mode is used when the MC145472 is configured as an LT and IDL master mode is used when the MC145472 is configured as an NT. The MC145472 can be used in slave–slave applications. Refer to the complete MC145472 data book for further details.

SERIAL CONTROL PORT (SCP) INTERFACE

The MC145472 is equipped with an industry standard SCP Interface. The SCP is used by an external controller, such as an MC6805 family microcontroller, MC145488 Dual Data Link Controller, or MC68302 Integrated Multiprotocol Processor, to communicate with the U–Interface Transceiver.

The SCP is a full–duplex, four–wire interface with control and status information passed to and from the U–Interface Transceiver. The SCP Interface consists of a transmit output, a receive input, a data clock, and an enable signal. These device pins are known as SCP Tx, SCP Rx, SCP CLK, and SCPEN, respectively. The SCP Clock determines the rate of exchange of data in both the transmit and receive directions, and the SCP Enable signal governs when this exchange is to take place. The four–wire SCP Interface is supplemented with an interrupt request line, IRQ, for external microcontroller notification of an event requiring service.

The operation and configuration of the MC145472 is controlled by setting the state of its control registers and monitoring its status registers. The control, status, and M channel data registers reside in six 4–bit wide Nibble Registers, one 12–bit wide "Nibble Register", and sixteen 8–bit wide Byte Registers. Figures 11 and 12 are examples of how data is transferred over the SCP.

2B1Q INTERFACE

Figure 13 shows the recommended 2B1Q interface network for connection to the U–Interface and component specifications are shown in Table 8.

NOTE

Motorola continues to qualify several third party sources for the 2B1Q Interface transformer. Contact your local Motorola representative or the Motorola factory applications staff for the latest information regarding component sourcing.

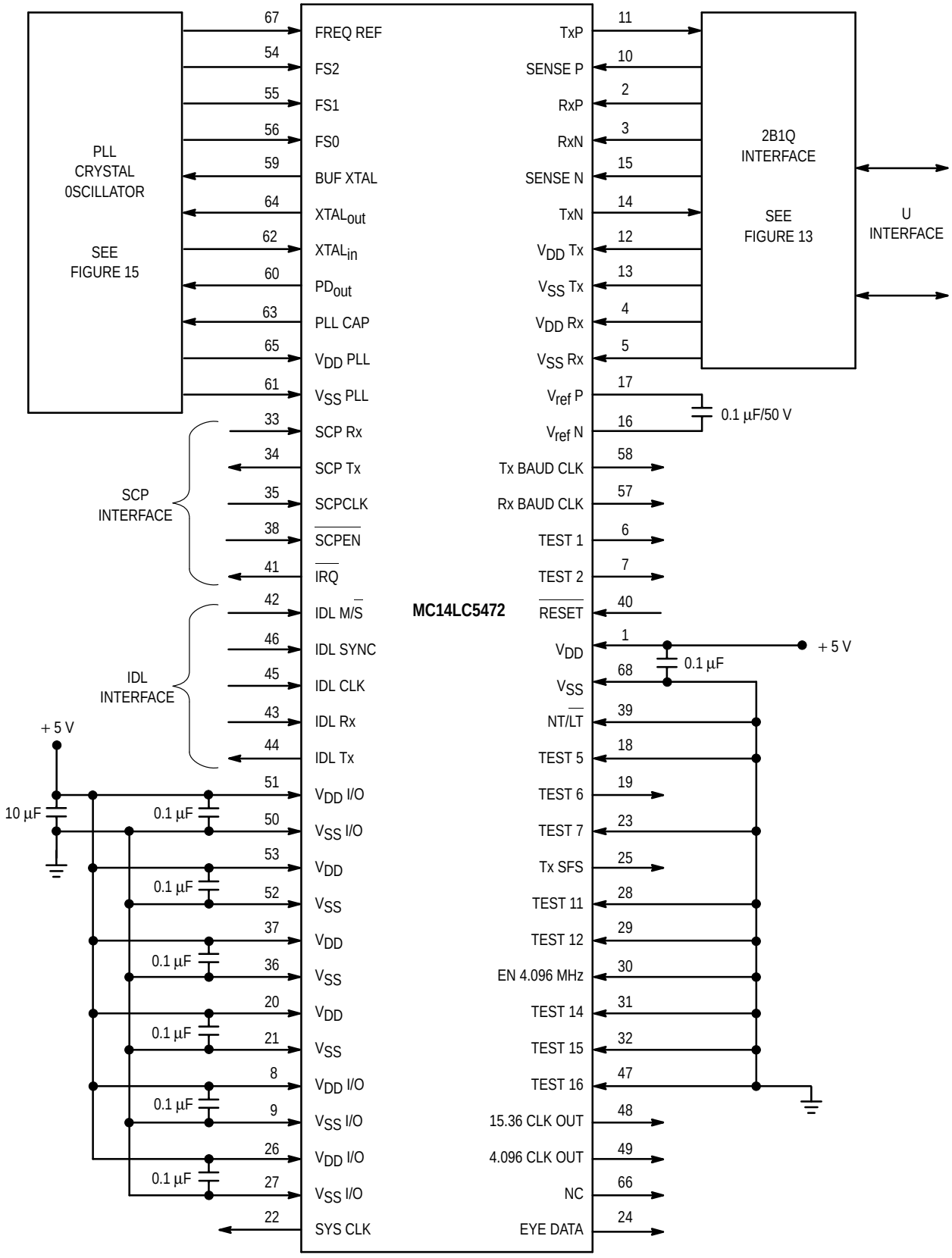


Figure 8. Typical LT Mode Connections

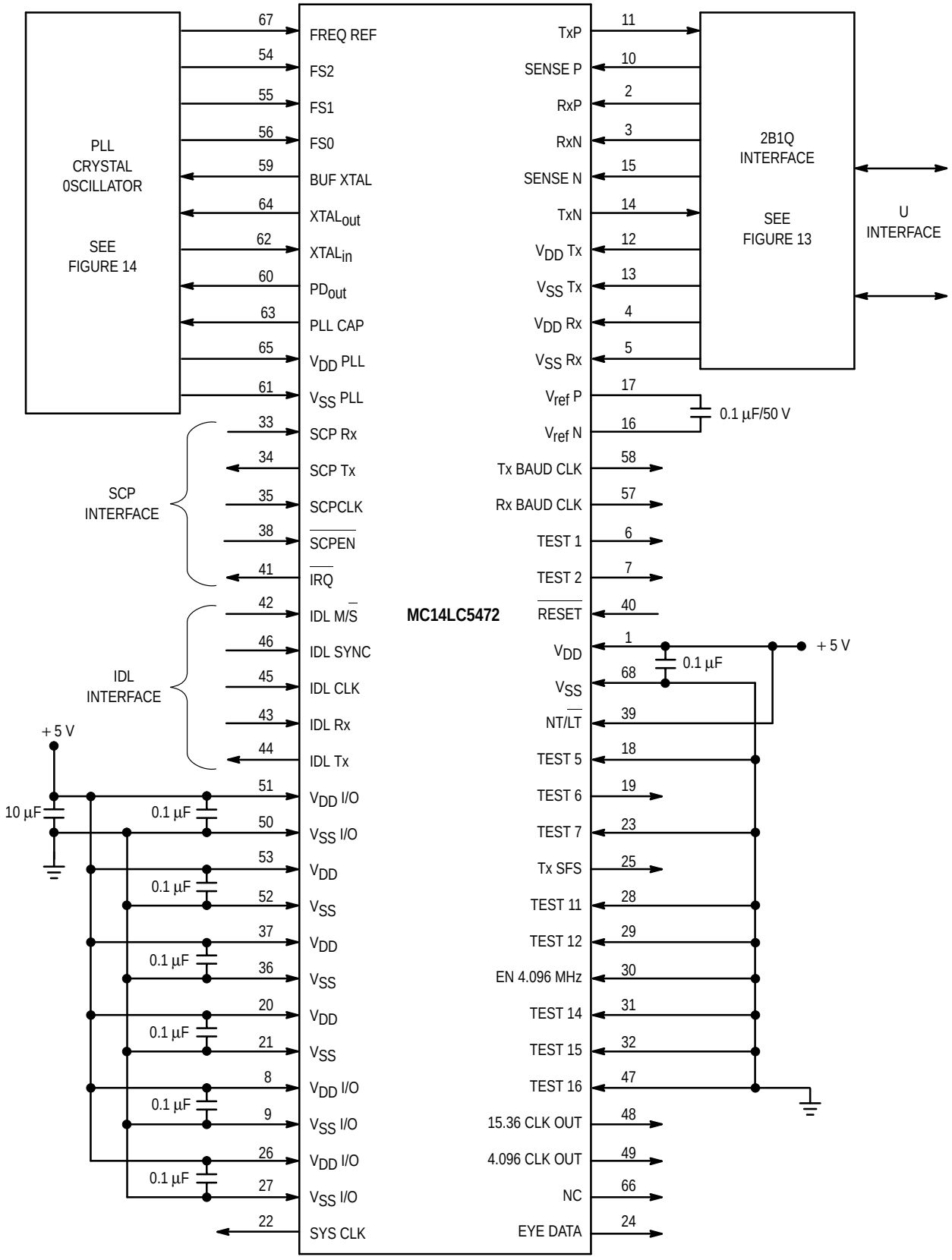
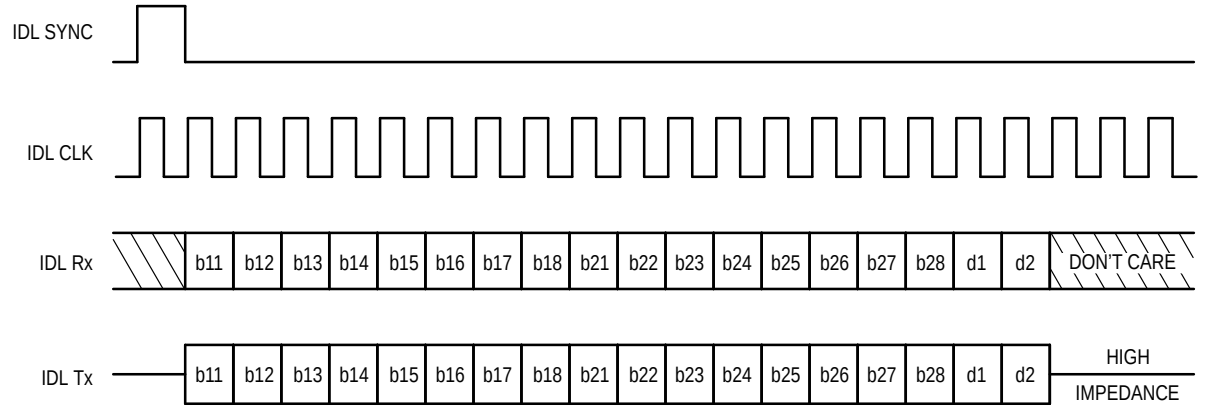
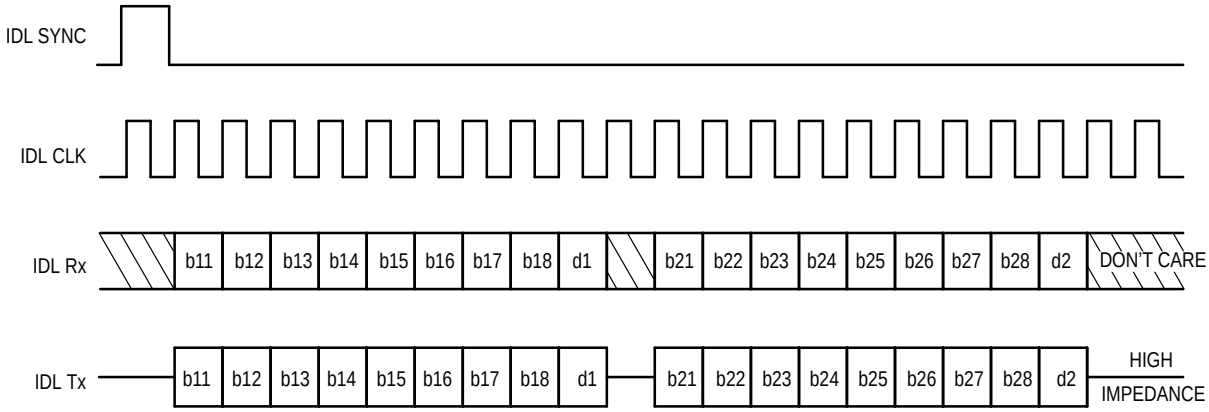


Figure 9. Typical NT Mode Connections



a. IDL Interface Timing in 8–Bit Mode



b. IDL Interface Timing in 10–Bit Mode

Figure 10. IDL Interface Data Formats

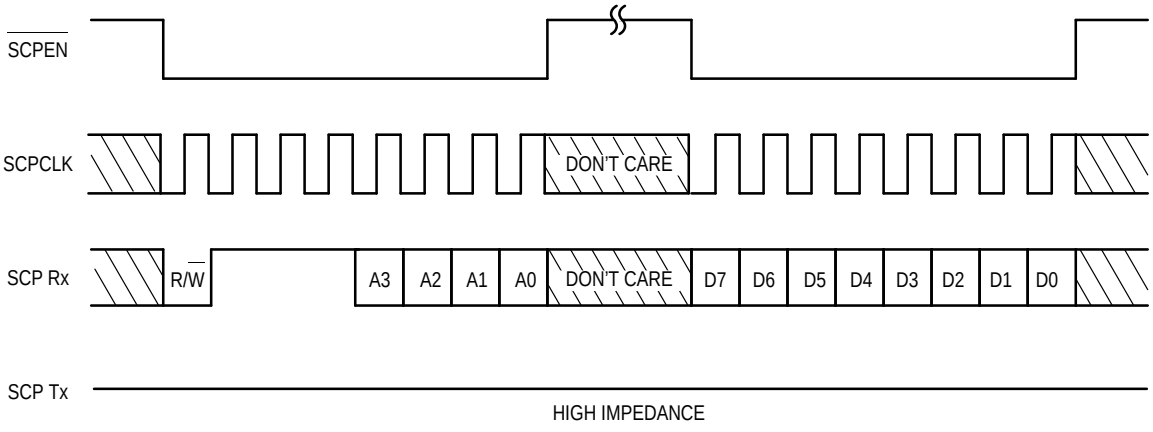


Figure 11. SCP Byte Register Write Operation Using Double 8–Bit Transfer

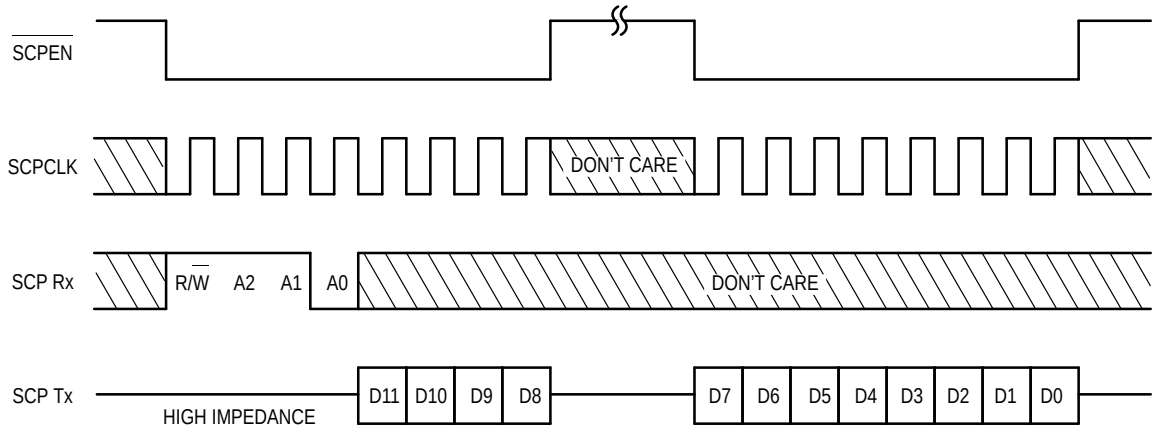


Figure 12. SCP Register R6 Read Operation

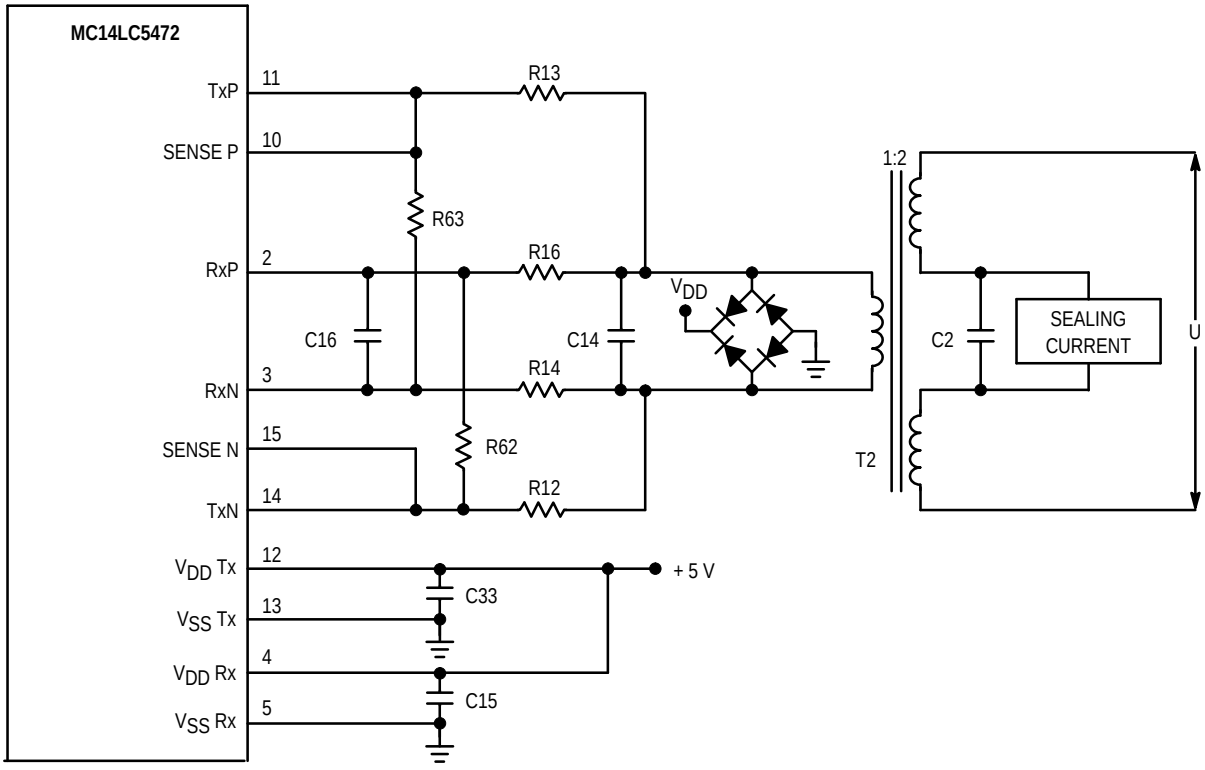


Figure 13. Typical 2B1Q Interface Schematic

Table 8. Line Interface Component Values

Component	Description
C2	1.0 μF, 100 V, 10%, low distortion capacitor
C14	0.033 μF, 50 V, 10%, low distortion capacitor
C15	0.1 μF ceramic, 50 V
C16	270 pF, or nearest commercial value, 10%, silver mica or other low distortion, high quality capacitor
C33	0.1 μF ceramic, 50 V
R12	14.3 Ω, 1%, metal film or other high quality low distortion resistor
R13	14.3 Ω, 1%, metal film or other high quality low distortion resistor
R14	1.00 kΩ, 1% metal film or other high quality low distortion resistor
R16	1.00 kΩ, 1% metal film or other high quality low distortion resistor
R62	1.69 kΩ, 1% metal film or other high quality low distortion resistor
R63	1.69 kΩ, 1% metal film or other high quality low distortion resistor
T2	Pulse transformer, 1:2 turns ratio
Diode Bridge	4 x 1N4001

NOTE: R12, R13, C14, and C16 are specific to Dale transformer part number PT–200–02. Motorola does not warrant this transformer, and in no way suggests that this is the only appropriate transformer.

Crystal Oscillator Or Phase–Locked Loop (PLL)

These pins provide access to the phase detector and crystal oscillator portions of the U–Interface Transceiver PLL. A 15.36 MHz and a 4.096 MHz clock output are available for other devices.

In the LT mode, the PLL synchronizes a 20.48 MHz crystal oscillator to one of eight possible reference frequencies supplied by the switching equipment. This phase–locked clock assures that the transmitted 2B1Q signal is synchronized to the frequency reference supplied at the FREQ REF pin. In addition, the very low frequency response (≈ 1 Hz) of the PLL loop filter limits jitter present in the frequency reference. Refer to Figures 14 and 15 for details of the loop filter network and voltage controlled crystal oscillator and Table 11 for suggested component values.

In the NT mode there is both an analog and a digital PLL. The analog PLL synchronizes the 20.48 MHz crystal oscillator to the recovered 2B1Q signal. The digital PLL synchronizes the IDL clock to the recovered 2B1Q signal and also updates the analog PLL on a regular basis. This ensures that the recovered timing is synchronized to the signal received from the LT. In NT mode the U–Interface Transceiver can lock to 80 kbaud ± 32 ppm receive signals when the recommended VCXO circuit is used.

The FREQ REF pin is a Schmitt–trigger digital input which provides the reference frequency for the phase–locked loop in LT mode. The eight possible frequencies include: 2.048, 2.560, 4.096, 7.680, 8.192, 10.24, 15.36, and 20.48 MHz.

The three frequency select inputs (FS0 – FS2) are used to select one of the eight possible reference frequencies which may be used to drive the Frequency Reference Input when the device is in the LT mode.

$XTAL_{in}$ and $XTAL_{out}$ are the oscillator pins. A 20.48 MHz pullable crystal and other components may be connected to $XTAL_{in}$ and $XTAL_{out}$ to form a voltage controlled crystal oscillator in the LT or NT modes.

PD_{out} is the output of the on–chip phase detector of the PLL. PD_{out} is a current source output of approximately 15 μA and connects to the PLL filter network.

PLL CAP must have a 0.1 μF capacitor connected between it and ground.

Clock Outputs

BUF XTAL is the buffered output from the 20.48 MHz oscillator and can be used to drive the $XTAL_{in}$ pin of other MC145472 devices in the same system. BUF XTAL must not be used as a microprocessor clock since it is turned off after a reset.

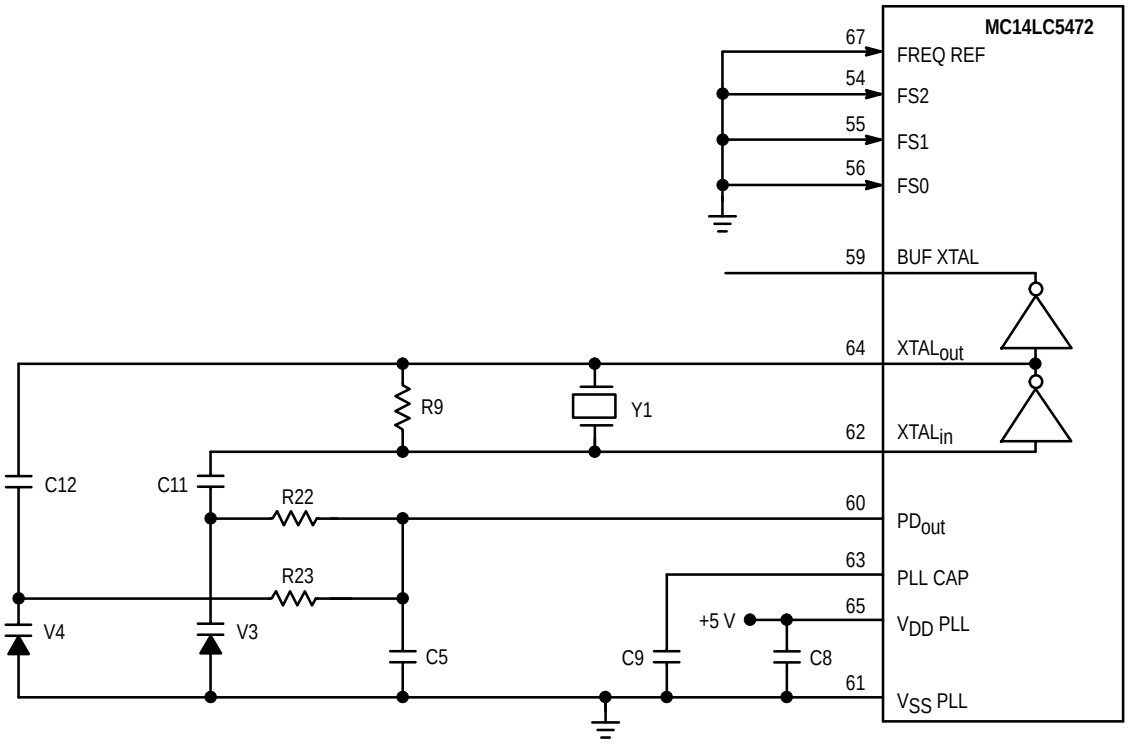
15.36 CLKOUT provides a buffered 15.36 MHz clock output that can be used for the MC145474/75 S/T transceiver clock. This clock is a 20.48 MHz clock with every fourth clock tick removed. Figure 16 shows the 15.36 MHz clock waveform. There may be applications where this clock is inadequate.

4.096 CLKOUT provides a buffered 4.096 MHz clock out–put that can be used for a microcontroller clock. The 4.096 Enable input, (Pin 30), must be high to enable this clock.

Test Pins

The following input pins are utilized by Motorola to test the functionality of the MC145472 during the manufacturing process. These pins should be connected to ground for normal operation:

TEST 5, TEST 7, TEST 11, TEST 12, TEST 14, TEST 15, and TEST 16



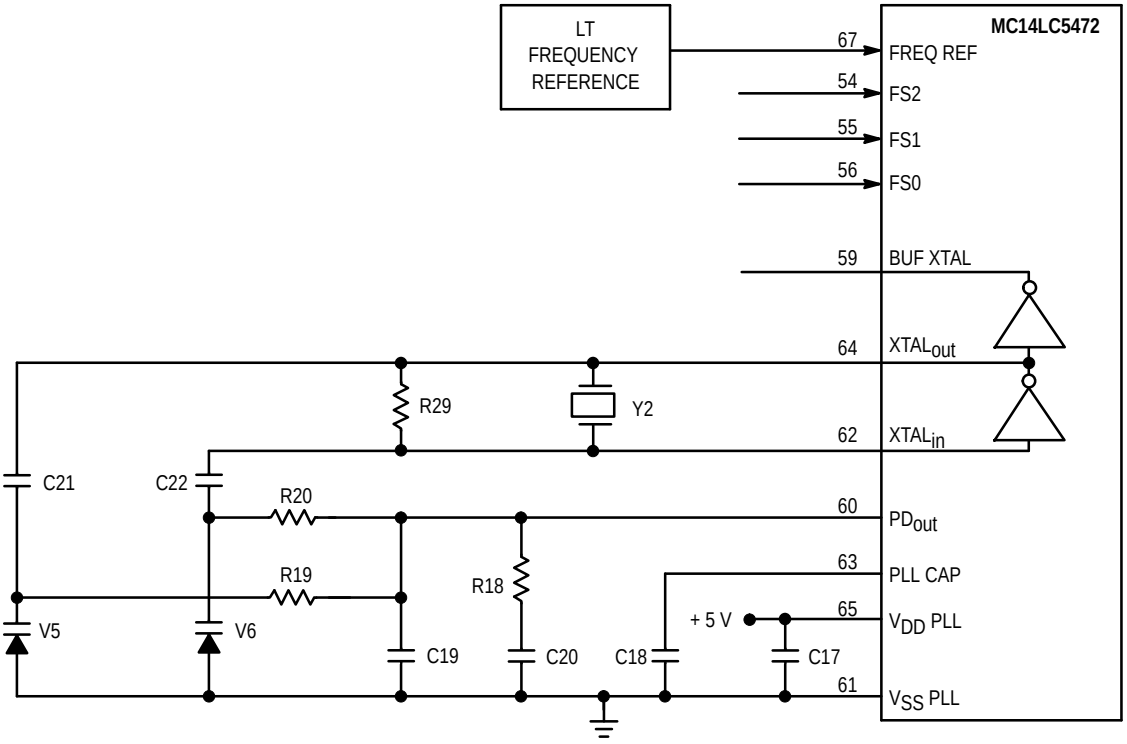
NOTE: See Table 9 for component values.

Figure 14. Typical NT Mode Voltage Controlled Crystal Oscillator Schematic

Table 9. NT Mode Crystal Oscillator Component Values

Component	Description
C5	0.1 µF ceramic, 50 V
C8	0.1 µF ceramic, 50 V
C9	0.1 µF ceramic, 50 V
C11, C12	0.01 µF to 0.1 µF ceramic, 50 V
R22, R23	270 kΩ, 5%
R9	0.5 MΩ to 1.5 MΩ, 5%
V3, V4	MV209 varactor. See complete MC145472 data book for sourcing and specification information.
Y1	20.48 MHz ± 40 ppm, 18 pF, pullable between 240 to 300 ppm over a capacitance range of 12 to 22 pF. See complete MC145472 data book for sourcing.

NOTE: V3, V4 may be combined into a single package.



NOTE: See Table 10 for component values.

Figure 15. Typical LT Mode PLL Crystal Oscillator Schematic

Table 10. LT Mode PLL Crystal Oscillator Component Values

Component	Description
C17	0.1 μF ceramic, 50 V
C18	0.1 μF ceramic, 50 V
C19	0.1 μF ceramic, 50 V
C20	See Table 11 for reference frequency dependent value.
C21	0.01 μF to 0.1 μF ceramic, 50 V
C22	0.01 μF to 0.1 μF ceramic, 50 V
R18	See Table 11 for reference frequency dependent value.
R19	270 kΩ, 5%
R20	270 kΩ, 5%
R29	0.5 MΩ to 1.5 MΩ, 5%
R_B	1 kΩ
R_C	47 kΩ
V5, V6	MV209 varactor diode. See complete MC145472 data book for sourcing and specification information.
Y2	20.48 MHz ± 40 ppm, 18 pF, pullable between 240 to 300 ppm over a capacitance range of 12 to 22 pF. See complete MC145472 data book for sourcing.

The following output pins are utilized by Motorola to test the functionality of the MC145472 during the manufacturing process. These pins should be left open circuit for normal operation.

TEST 1, TEST 2, TEST 6

SCP HIDOM

The MC145472 U–Interface Transceiver has the capability of forcing all outputs (both analog and digital) to the high impedance state. This feature, known as “the serial control port high impedance digital output mode” is provided to allow “in circuit” testing of other circuits or devices resident on the same PCB without requiring the removal of the MC145472.

TEST AND DEBUG

The MC145472 permits an external microcontroller to take control of the transmit framer by writing to control bits in Byte Register 8. This is very useful for debugging prototypes since the MC145472 can be forced to transmit a variety of signals regardless of the presence or lack of presence of a signal on the receive pins. Table 12 summarizes these signals and the control bits.

Table 11. LT PLL Frequency Select Options and Component Values

Reference Frequency (MHz)	FS2	FS1	FS0	R18 (Ω, 5%)	C20 (μF)
15.36	0	0	0	1800	150
10.24	0	0	1	910	330
8.192	0	1	0	2200	150
7.68	0	1	1	3300	100
4.096	1	0	0	2200	150
2.56	1	0	1	3300	100
2.048	1	1	0	3600	68
20.48	1	1	1	360	680

Table 12. Frame Control Modes

Frame Steering	Frame Control 2:0			Superframe Framer Mode of Operation	
b7	b6	b5	b4	NT	LT
1	0	0	0	SN0	SL0
1	0	0	1	Six frames of 10 kHz tone followed by SN1	SL1
1	0	1	0	SN2	SL2
1	0	1	1	SN3	SL3
1	1	0	0	10 kHz tone	
1	1	0	1	40 kHz tone	
1	1	1	0	Generates a single quat every basic frame which alternates over all four of the 2B1Q symbols.	
1	1	1	1	Superframe Framer free runs the scrambler with no synchronization words.	
0	Don’t Care			The Superframe Framer output is determined by the state of the Automatic Activation Controller.	

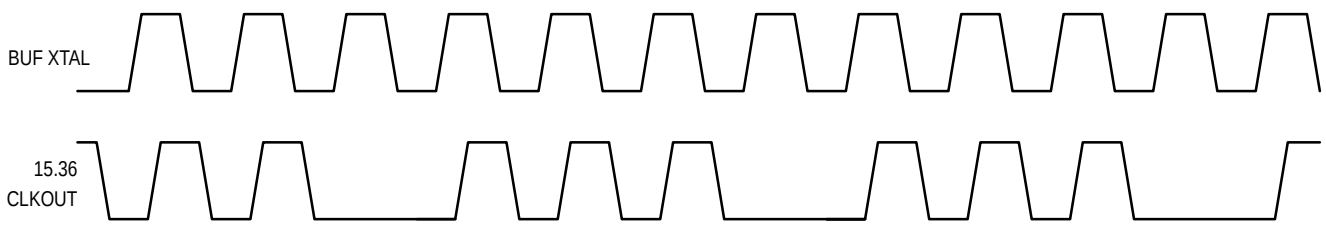


Figure 16. Waveform for 15.36 MHz Clock Output

SERIAL CONTROL PORT REGISTERS

INTRODUCTION

This section summarizes all of the MC145472 U–Interface Transceiver control and status registers available via the SCP Interface. Tables 13 through 15 summarize the registers.

The MC145472 SCP Interface is pin–for–pin identical to that of the MC145474/75 S/T–Interface Transceiver. Using the same interface as the MC145474/75 provides a common interface for applications utilizing both the MC145472 and the MC145474/75 such as an NT1 and for applications which can use either interface device such as line cards or terminal equipment.

In addition to being pin–for–pin compatible, the architecture of the nibble register map and the operation of the SCP Interface is similar to that of the MC145474/75. This is intended to simplify the code development effort and minimize device driver code size for a microcontroller.

See the MC145472 data book for a complete description of the bits in the register map.

The Register Map consists of six 4–bit Nibble Registers, one 12–bit Register, and sixteen 8–bit Byte Registers, designated as NR0 – NR5, R6 (see Tables 13 and 14), and BR0 – BR15 (see Table 15), respectively. Register R6 appears in the nibble register memory map but is a 12–bit register and is used to access the embedded operations channel.

NIBBLE REGISTER DESCRIPTIONS

This section briefly describes the U–chip nibble registers and their uses. The embedded operations channel register R6 appears in the nibble register map even though it is a 12–bit register.

NR0

This register contains read/write control bits. All bits are cleared on Hardware Reset (RESET, Pin 40), but are unaffected by Software Reset (NR0(b3)). This register is write only when the U–Interface Transceiver is in Absolute Power–Down mode (NR0(b1)).

NR1

This register contains device activation status. All bits are cleared on Software Reset or Hardware Reset. If any bit in this register changes from 0 to a 1, or if Linkup, Superframe Sync, or Transparent/Activation in Progress change from a one to a zero, an IRQ 3 (NR3(b3)) is generated.

NR2

Register NR2 contains activation and deactivation control bits. All bits are cleared on Software Reset or Hardware Reset.

NR3

This is the interrupt status register. The register is read only. All bits are cleared on Software Reset or Hardware Reset. Each interrupt status bit in the register operates the same. If it is a 1, and its corresponding interrupt enable is a 1 in Register NR4, the IRQ pin on the chip will become active. IRQ 3 has the highest priority while IRQ 0 has the lowest.

NR4

This is the interrupt mask register. All bits are cleared on Software Reset or Hardware Reset. Each bit operates the same. For example, if bit Enable IRQ 1 is set to 1 by the external microcontroller and the IRQ 1 interrupt bit is set to 1 in NR3, the IRQ pin (Pin 41) becomes active.

NR5

This register contains control bits for the IDL Interface. More IDL controls are in Registers BR6 and BR7. All bits are cleared on Software Reset or Hardware Reset.

Table 13. Nibble Registers Map

	b3	b2	b1	b0
NR0	SOFTWARE RESET	POWER DOWN ENABLE	ABSOLUTE POWER DOWN	RETURN TO NORMAL
NR1	LINKUP	ERROR INDICATION	SUPERFRAME SYNC	TRANSPARENT/ACTIVATION IN PROGRESS
NR2	ACTIVATION REQUEST	DEACTIVATION REQUEST	SUPERFRAME UPDATE DISABLE	CUSTOMER ENABLE
NR3	IRQ 3	IRQ 2	IRQ 1	IRQ 0
NR4	ENABLE IRQ 3	ENABLE IRQ 2	ENABLE IRQ 1	ENABLE IRQ 0
NR5	RESERVED	BLOCK B1	BLOCK B2	SWAP B1/B2

Table 14. Register R6 Map

	b22	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R6	eoc a1	eoc a2	eoc a3	eoc dm	eoc i1	eoc i2	eoc i3	eoc i4	eoc i5	eoc i6	eoc i7	eoc i8

Table 15. Byte Register Map, BR0 – BR15A

	b7	b6	b5	b4	b3	b2	b1	b0
BR0	M40	M41	M42	M43	M44	M45	M46	M47
BR1	M40	M41	M42	M43	M44	M45	M46	M47
BR2	M50	M60	M51	febe INPUT	RESERVED	RESERVED	RESERVED	RESERVED
BR3	M50	M60	M51	RECEIVED febe	COMPUTED nebe	VERIFIED act	VERIFIED dea	SUPERFRAME DETECT
BR4	febe COUNTER 7	febe COUNTER 6	febe COUNTER 5	febe COUNTER 4	febe COUNTER 3	febe COUNTER 2	febe COUNTER 1	febe COUNTER 0
BR5	nebe COUNTER 7	nebe COUNTER 6	nebe COUNTER 5	nebe COUNTER 4	nebe COUNTER 3	nebe COUNTER 2	nebe COUNTER 1	nebe COUNTER 0
BR6	U–LOOP B1	U–LOOP B2	U–LOOP 2B+D	U–LOOP TRANSPARENT	IDL–LOOP B1	IDL–LOOP B2	IDL–LOOP 2B+D	IDL–LOOP TRANSPARENT
BR7	BR15A SELECT	RESERVED	RESERVED	IDL INVERT	IDL FREE RUN	IDL SPEED	IDL M/S INVERT	IDL 8/10
BR8	FRAME STEERING	FRAME CONTROL 2	FRAME CONTROL 1	FRAME CONTROL 0	crc CORRUPT	MATCH SCRAMBLER	RECEIVE WINDOW DISABLE	NT/LT INVERT
	FRAME STATE 3	FRAME STATE 2	FRAME STATE 1	FRAME STATE 0	RESERVED	RESERVED	RESERVED	NT/LT MODE
BR9	eoc CONTROL 1	eoc CONTROL 0	M4 CONTROL 1	M4 CONTROL 0	M5/M6 CONTROL 1	M5/M6 CONTROL 0	febe/nebe CONTROL	RESERVED
BR10	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
BR11	ACTIVATION CONTROL 6	ACTIVATION CONTROL 5	ACTIVATION CONTROL 4	ACTIVATION CONTROL 3	ACTIVATION CONTROL 2	ACTIVATION CONTROL 1	ACTIVATION CONTROL 0	ACTIVATION TIMER DISABLE
	ACTIVATION STATE 6	ACTIVATION STATE 5	ACTIVATION STATE 4	ACTIVATION STATE 3	ACTIVATION STATE 2	ACTIVATION STATE 1	ACTIVATION STATE 0	ACTIVATION TIMER EXPIRE
BR12	ACTIVATION CONTROL STEER	INTERPOLATE ENABLE	LOAD ACTIVATION STATE	STEP ACTIVATION STATE	HOLD ACTIVATION STATE	JUMP SELECT	RESERVED	FORCE LINKUP
	EPI 18	EPI 17	EPI 16	EPI 15	EPI 14	EPI 13	EPI 12	EPI 11
BR13	ENABLE MEC UPDATES	ACCUM EC OUTPUT	ENABLE EC UPDATES	FAST EC BETA	ACCUM DFE OUTPUT	ENABLE DFE UPDATES	FAST DFE/ARC BETA	CLEAR ALL COEFF'S
	EPI 10	EPI 9	EPI 8	EPI 7	EPI 6	EPI 5	EPI 4	EPI 3
BR14	RESERVED	ro/wo TO r/w	RESERVED	FRAMER TO DEFRAMER LOOP	±1 TONES	RESERVED	RESERVED	ENABLE CLKs
BR15	RESERVED	RESERVED	RESERVED	MASK 4	MASK 3	MASK 2	MASK 1	MASK 0
BR15A	FREQ ADAPT	JUMP DISABLE	RESERVED	RESERVED	ENABLE Tx SFS	ENABLE 15.36 MHz	ENABLE 20.48 MHz	ENABLE EYE DATA AND BAUD CLK
				RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

R6

This register is 12 bits long to match the length of the eoc message. Operation of Register R6 depends on the setting of the eoc control bits in BR9(b7:b6) and BR14(b6). This register is double buffered.

In the default mode (BR14(b6) is 0), R6 performs as a read only/write only register. Data that is read from R6 by the external microcontroller is the eoc message that the Superframe Deframer stores according to the eoc Control register, BR9(b7:b6). Data that is written to R6 is stored in a latch contained in the Superframe Framer and is subsequently transmitted beginning on the next transmit eoc frame boundary. The Superframe Framer latches are set to ones on hardware or software resets.

BYTE REGISTER DESCRIPTIONS

This section briefly describes the U–chip byte registers and their uses.

BR0

This register contains the M4 channel bits that are framed and sent by the Superframe Framer. The bits that are written to this register are sent out on the next transmit superframe boundary. This register is double buffered. All bits are set to 1s following a Hardware Reset (RESET, Pin 40) or Software Reset (NR0(b3)).

BR1

By reading this register, the external microcontroller obtains a buffered copy of the M4 bits that are parsed from the received superframe by the Superframe Deframer. The values in the register are valid when Superframe Sync, NR1(b1), is a one. BR1 is updated based on the mode set in Register BR9(b5:b4). This register is double buffered. The receive M4 channel byte can be read at any time during the Superframe prior to the next update.

BR2

This register contains the reserved M5 and M6 bits that are sent by the Superframe Framer. The bits that are written to the register are sent out on the next transmit superframe boundary, provided Superframe Updated Disable (NR2(b1)) is set to 0. All bits are set to 1s following a Hardware Reset or Software Reset. The febe input bit is used to indicate how the returning febe bit is calculated. Bits b7, b6, and b5 are double buffered. The state of the Reserved bits BR2(b3:b0) is inconsequential.

BR3

This register contains the ANSI T1.601–1992 reserved M5 and M6 bits that are received by the Superframe Deframer, occurring in basic frames 1 and 2 of the superframe, and four other Superframe Deframer status bits. The M5 and M6 values in the register are valid when the Superframe Sync bit (NR1(b1)) is a 1. M50, M51, and M60 are updated based on the mode set in Register BR9(b3:b2). Bits b7, b6, b5 are double buffered. They can be read at any time during the superframe prior to the next update.

BR4

This register contains the current febe count. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it. If the febe bit is active in a superframe, the counter will increment at the end of the received superframe. The count does not wrap around from FF to 00 The counter will not increment unless Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are both 1s.

BR5

This register contains the current nebe count. A nebe occurs whenever the received crc message does not match the computed crc or when Linkup (NR1(b3)) is a 1 and Superframe Sync (NR1(b1)) is a 0. Superframe timing to increment the nebe counter during times when Superframe Sync is a 0 is maintained by the Superframe Framer. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it. If the Superframe Deframer detects a crc error in the received superframe, the counter will increment at the end of that superframe. The count does not wrap around from FF to 00.

BR6

This register contains the loopback controls. Loopbacks can be directed towards the U–Interface or towards the IDL interface. For normal (no loopback) operation all bits should be 0. BR6 is cleared by a Software Reset, Hardware Reset, or when the Return to Normal bit (NR0(b0)) is set. When a bit is set to a 1 the appropriate loopback is enabled.

BR7

This register is used to configure the IDL interface. By setting bits in this register the IDL interface can be configured as master or slave, 8– or 10–bit data format, or the IDL clock rate can be selected when in master mode. BR7 is cleared on Hardware Reset or Software Reset. All bits in this register are read/write.

BR8

This register contains controls that are used for maintenance operations such as external loopbacks, Superframe Framer Control and State information, and NT/LT mode control. All write capable bits are cleared on a Software Reset or Hardware Reset. Bits b7 – b4, and b0, are read only/write only. To read the write only bits, it is necessary to set BR14(b6) to a one.

BR9

This register contains mode control over the Deframer's updating of the received maintenance bits. The register is cleared on Software Reset or Hardware Reset.

BR10

This register is RESERVED.

BR11

This register contains activation state and control data. All the bits are cleared on Hardware Reset and Software Reset. The register is a read only/write only register. Setting BR14(b6) to a 1 permits the external microcontroller to read back the write portion of the register.

BR12

This register is read only/write only. The write only portion controls the U–Interface Transceiver's Central Processing Unit (CPU) and activation controller. The read portion contains the eight most significant bits of the Error Power Indicator (EPI) register in the CPU. By setting BR14(b6) to a 1, the external microcontroller can read back the setting of the control bits. These bits are cleared on a Hardware Reset or Software Reset.

BR13

This register contains several bits that control the internal operation of the U–Interface Transceiver. These bits are cleared on a Hardware Reset or Software Reset.

BR14

This register is used for setting various diagnostic modes. This register is cleared on a Hardware Reset or Software Reset. When all of these bits are 0, the register map is in the default mode.

BR15

This register contains the revision number of the particular U–Interface Transceiver device in bits 0 – 4. BR15 is accessed by an SCP transfer when BR7(b7) is a 0 and the byte address in the SCP transfer is 15.

BR15A

This register is used to enable clock and test data outputs. All writeable bits in this register are cleared to 0 after a reset. BR15A is accessed by an SCP transfer when BR7(b7) is a 1 and the byte address in the SCP transfer is 15.

ACTIVATION AND DEACTIVATION

INTRODUCTION

Activation or start–up is the process that U–Interface Transceivers use to initiate a robust full–duplex communications channel. This process, which may be initiated from either the LT or the NT mode U–Interface Transceiver, is a well–defined sequence of procedures during which the training of the equalizers and echo cancelers at each end of the transmission line takes place. Two types of activation, cold start or warm start, may occur. The MC145472 is capable of automatically supporting both types.

Deactivation is the process used to gracefully end communication between the U–Interface Transceivers at each end of the transmission line. Only the LT mode U–Interface Transceiver may initiate a deactivation procedure.

The internal register set of the MC145472 is detailed in Tables 13 through 15.

ACTIVATION SIGNALS FOR NT MODE

When configured as an NT, the U–Interface Transceiver can transmit any of the signals shown in Table 16. The actual procedure undertaken by the device using these five signals is described later in this section.

ACTIVATION SIGNALS FOR LT MODE

When configured as an LT, the U–Interface Transceiver can transmit any of the signals shown in Table 17. The actual procedure undertaken by the device using these five signals is described later in this section.

Table 16. NT Mode Activation Signals

Information Station	Description
TN	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of 6 frames.
SN0	No signal transmitted.
SN1	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SN2	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SN3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when M4 act bit = 1. When M4 act = 0, transmitted 2B+D data = 1.

Table 17. LT Mode Activation Signals

Information Station	Description
TL	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of 2 frames.
SL0	No signal transmitted.
SL1	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SL2	Synchronization word present, superframe synchronization word (ISW) present, 2B+D = 0, and M channel bits active.
SL3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when M4 act bit = 1. When M4 act = 0, transmitted 2B + D data = 0.

ACTIVATION INITIATION

The U–Interface Transceiver can be activated in either of two ways. The external microcontroller can explicitly set the Activation Request bit, NR2(b3), to a 1 or the transceiver can detect an incoming 10 kHz wake–up tone from the far end.

An LT configured U–Interface Transceiver looks for an NT sending the TN wake–up tone. An NT configured U–Interface Transceiver looks for an LT sending the TL wake–up tone. In either case, Activation Request being set or a wake–up tone being detected, the U–Interface Transceiver proceeds with activation automatically and signals the result of the activation to the external microcontroller by setting status bits in NR1.

ACTIVATION INDICATION

The activation status is indicated in Nibble Register 1. This register indicates whether the MC145472 is not activated, is in the process of activating or fully activated. This register also is used to provide error status.

LT DEACTIVATION PROCEDURES

ANSI T1.601–1992 specifies that only the LT can deactivate the U–Interface. This is done in the MC145472 by setting Deactivation Request (NR2(b2)) to 1.

NT DEACTIVATION PROCEDURES

ANSI T1.601–1992 specifies that the NT cannot initiate deactivation. The MC145472 deactivates to a warm start condition when Deactivation Request (NR2(b2)) is set to 1 prior to the LT deactivating the U–Interface. This should be done in response to the M4 dea bit changing from a 1 to a 0 at the NT when the loop is active.

M CHANNEL BITS

The eoc, M4, M5, and M6 channel bits are available at the SCP Interface once activation has been attained. All of the maintenance channel bits appear in the register map of the MC145472. These bits can be programmed by an external microcontroller to operate as defined in the ANSI T1.601 specification. The MC145472 has several operating modes for the M channel bits including a mode that automatically implements the embedded operations channel function in NT mode. Due to the M channel bits being register accessible they can also be redefined for proprietary applications.

SCP INTERFACE INDICATION OF TRANSMIT STATES

The four SCP bits, FS3 – FS0 BR8(b7:b4), indicate the current state of the Superframe Framer. See Table 12 for frame control modes.

MAINTENANCE CHANNEL

INTRODUCTION

The MC145472 provides a very flexible interface to the 4 kbps Maintenance Channel (M channel) defined in ANSI T1.601–1992. The M channel consists of 48 bits sent by both the LT and NT configured U–Interface Transceivers during the course of a superframe. These 48 bits are divided into six channels designated M1 – M6, each consisting of eight bits per superframe. The Embedded Operations Channel (eoc) consists of M1, M2, and M3. The overhead bits, such as crc, febe, act, and dea, are contained in channels M4, M5, and M6.

An external microcontroller can read from or write to the M channel via the SCP Interface. Interrupts to an external microcontroller can be enabled when an eoc, M4, M5, or M6 channel register is updated. M channel registers can be configured to update when a new value is detected between successive superframes, when a bit changes, or when two or three successive superframes of a new value are detected. The M4 channel act bit (BR1(b7)) can also be configured to automatically enable or disable customer data when in NT or LT mode of operation. The M4 channel dea bit (BR1(b6)) can also be configured to automatically issue a deactivation request in NT mode of operation. The M channel registers are updated only when Superframe Sync (NR1(b1)) is set to 1.

Figures 17 and 18 detail Maintenance Channel interrupt times with respect to the U–Interface for both NT and LT modes.

EMBEDDED OPERATIONS CHANNEL (eoc)

The eoc consumes 2 kbps of the 4 kbps Maintenance Channel (M4 channel). The eoc channel is used by the central office (LT) to initiate maintenance operations at the NT. The MC145472 can be configured to automatically perform the standard ANSI T1.601 eoc operations when in NT mode. The MC145472 can also be configured to permit an external microcontroller to service eoc commands. This permits extensions of the eoc command set to be implemented as the ANSI T1.601 standard is changed or proprietary solutions can be implemented for non–ISDN applications. Byte Register BR9 is used to configure the operating mode of the eoc. An interrupt is generated when the eoc register R6 is updated and Enable IRQ 2 (NR4(b2)) is set to 1.

M4 CHANNEL

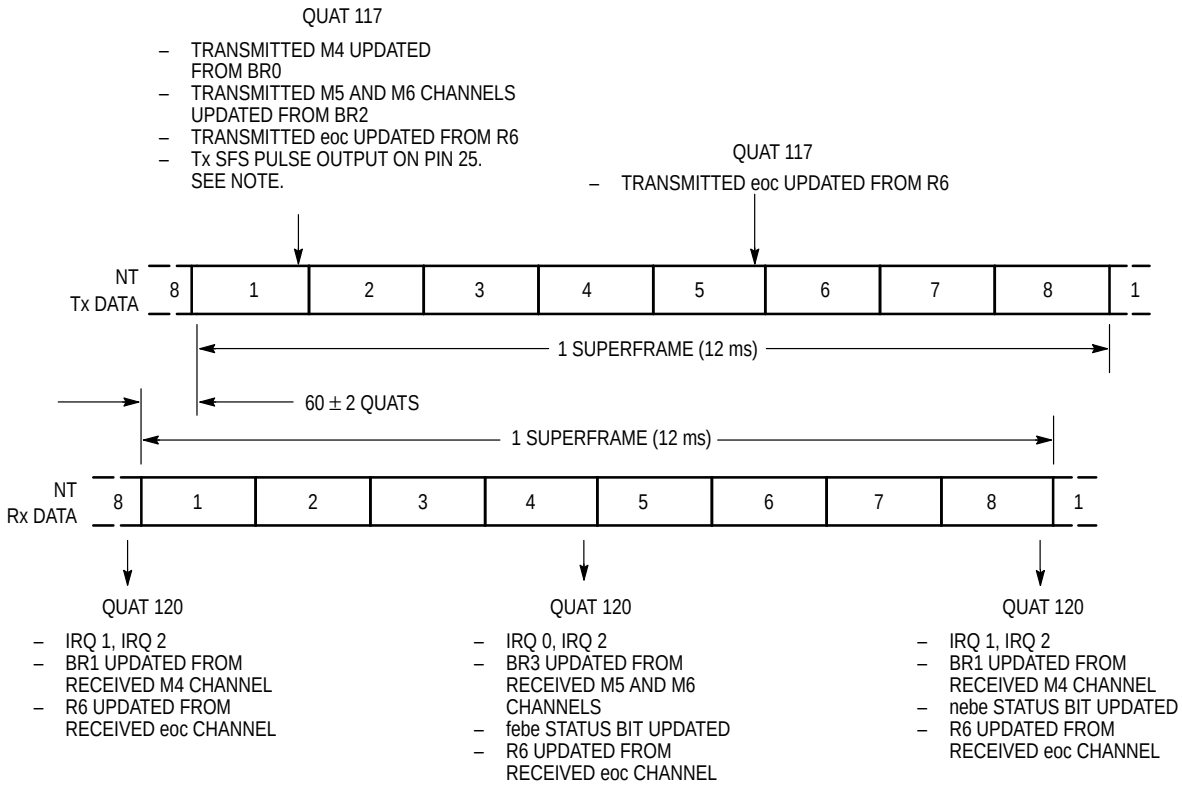
The M4 channel is used for signaling maintenance and system status between the NT and the LT. Typical information will be power status sent from the NT to the LT or the LT letting the NT know that the LT will deactivate the loop. The MC145472 provides four different modes that the M4 channel can operate in. A system designer can select whichever mode best fits the application. The received M4 data from the Superframe Deframer is available in BR0. The transmitted M4 channel data is written to Byte Register BR1. Byte Register BR9 is used to configure the operating mode of the M4 channel. An interrupt is generated when BR0 is updated and Enable IRQ 1, NR4(b1), is set to 1.

M5 AND M6 CHANNELS

The M5 and M6 channels are similar to the M4 channel. At this time the ANSI T1.601 specification defines all bits in these two channels as reserved bits. The MC145472 provides full access to these channels so they can be used in non–ISDN applications. The received M5 and M6 data from the Superframe Deframer is available in BR2. The transmitted M5/M6 channel data is written to Byte Register BR3. Register BR9 is used to configure the operating mode of the M5/M6 channels. These channels are configured as a pair. An interrupt is generated when BR2 is updated and Enable IRQ 0 (NR4(b0)) is set to 1.

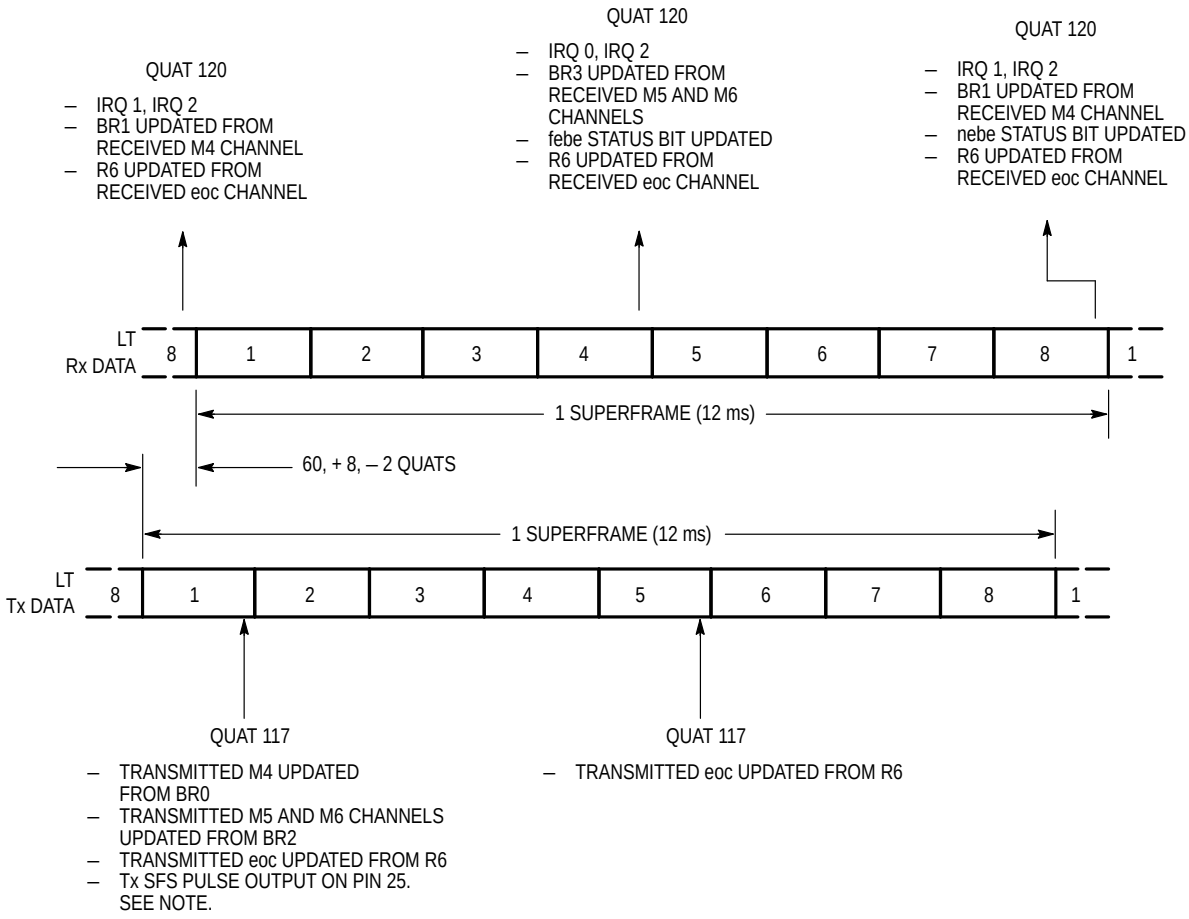
febe AND nebe BITS

The MC145472 has extensive febe (Far End Block Error) and nebe (Near End Block Error) maintenance capabilities. The state of the received computed nebe and of the received febe is available through the SCP Interface. Also, independent febe and nebe counters are available for performance monitoring purposes.



NOTE: Due to internal superframe delays the actual sync word marker on the TxP and TxN pins occurs 8 quats prior to the Tx SFS pulse. This causes the Tx SFS pulse to appear during Quat 113 at pin 25. Internal to the MC145472 the Tx SFS pulse is generated during Quat 117.

Figure 17. NT Mode Maintenance Channel Updates



NOTE: Due to internal superframe delays the actual sync word marker on the TxP and TxN pins occurs 8 quats prior to the Tx SFS pulse. This causes the Tx SFS pulse to appear during Quat 113 ± 1 at pin 25. Internal to the MC145472 the Tx SFS pulse is generated during Quat 117.

Figure 18. LT Mode Maintenance Channel Updates

LOOPBACK MODES

INTRODUCTION

The MC145472 U–Interface Transceiver supports four different loopback types, each having various modes. The four types are: 1) U–Interface Loopback, 2) IDL Interface Loopback, 3) Superframe Framer–to–Defframer Loopback, and 4) External Analog Loopback. Each of these loopback modes is selected by setting bits in the appropriate SCP register(s). Any combination of loopbacks may be invoked, including simultaneous loopbacks toward the U–interface and toward the IDL Interface. These loopbacks are available with transparency or non–transparency. “Transparent” means that a loopback passes the data on through to the other side as well as looping it back and “non–transparent” means that the data is blocked from being passed downstream and is replaced with the idle code (all 1s).

U–INTERFACE LOOPBACK

U–Interface Loopback is shown in Figure 19. As the shaded portion of the block diagram shows, this loopback mode exercises virtually the entire U–Interface Transceiver. 2B1Q symbols are received from the far end transmitter, recovered, passed through the IDL Interface block, and transmitted back to the far end receiver.

IDL INTERFACE LOOPBACK

IDL Interface Loopback is shown in Figure 20. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the IDL Rx pin and sends the same data back out the IDL Tx pin.

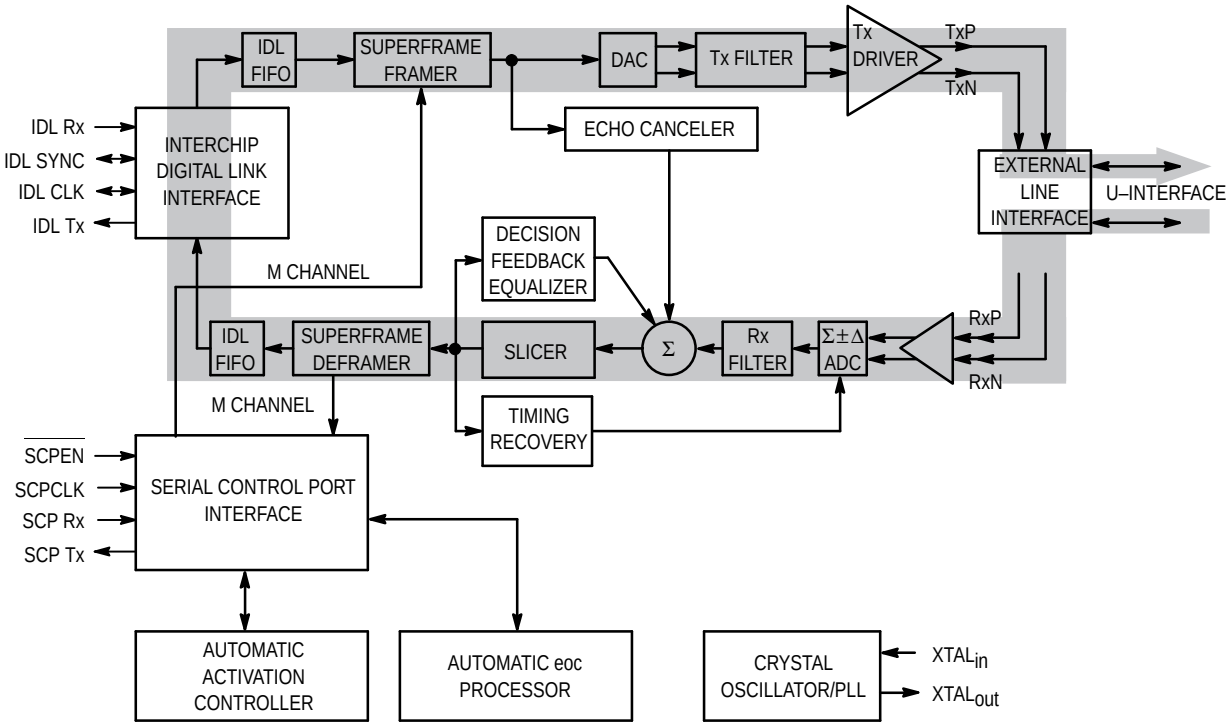


Figure 19. U–Interface Loopback Block Diagram

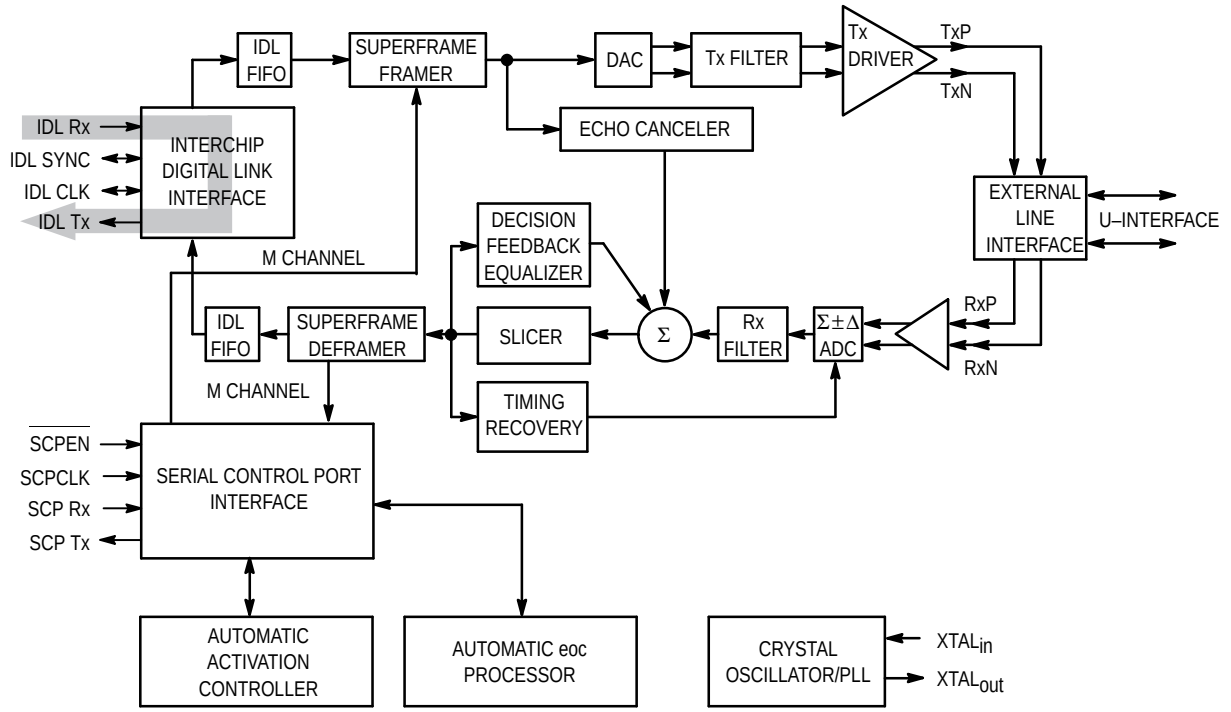


Figure 20. IDL Interface Loopback Block Diagram

Superframe Framer–to–Deframer Loopback

Superframe Framer–to–Deframer Loopback is shown in Figure 21. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the IDL Rx pin and M channel data via the SCP, performs all of the superframe framing and subsequent deframing functions, and sends the same data back out the IDL Tx pin and SCP. This loopback mode is intended primarily for diagnostic purposes.

External Analog Loopback

External Analog Loopback is shown in Figure 22. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the IDL Rx pin and transmits the data out the Tx Driver pins. The 2B1Q signal passes through the external line interface circuitry and back into the receiver input pins. The signal is then recovered and sent out the IDL Tx pin. Note that the external line interface has been physically disconnected from the U–Interface twisted wire pair.

Since the entire 2B1Q superframe is being looped back, loopback data includes the 2B+D channels and all of the M channels. For instance, data written by an external microcontroller to the eoc, M4, and M5/M6 registers, (R6, BR0, and BR2), is looped back and can be read from the eoc, M4, and M5/M6 registers, (R6, BR1, and BR3).

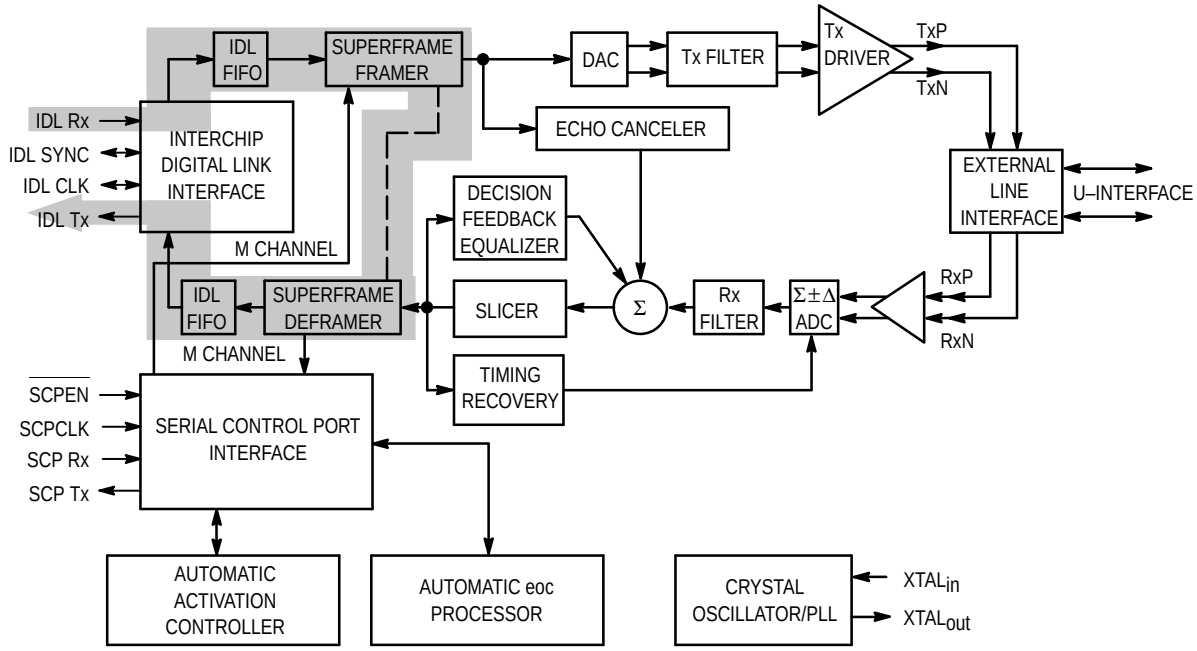


Figure 21. Superframe Framer–to–Deframer Loopback Block Diagram

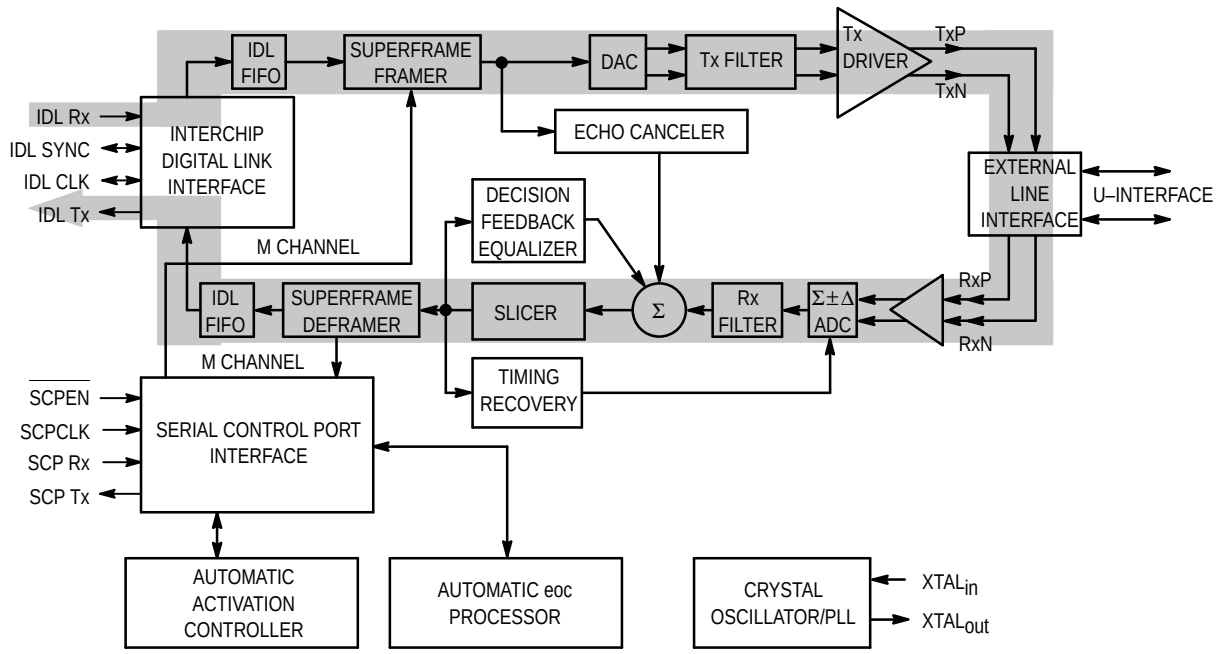


Figure 22. External Analog Loopback Block Diagram