MC14544B

BCD-to-Seven Segment Latch/Decoder/Driver for Liquid Crystals

CMOS MSI (Low–Power Complementary MOS)

The MC14544B BCD–to–seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4–bit storage latch and an 8421 BCD–to–seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. The Ripple Blanking Input (RBI) and the Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes.

For other types of readouts, such as light–emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

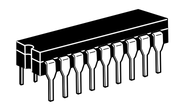
Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capability for Suppression of Non–significant zero
- Capable of Driving Two Low–power TTL Loads, One Low–power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

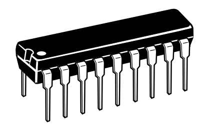
MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Input Current per Pin	I_{in}	± 10	mAdc
Operating Temperature Range	T_A	– 55 to + 125	°C
Power Dissipation, per Package†	P_D	500	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} I_{OLmax}	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} P_{OLmax}	70	mW

* $P_{OHmax} = I_{OH} (V_{OH} – V_{DD})$ and $P_{OLmax} = I_{OL} (V_{OL} – V_{SS})$
* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 726



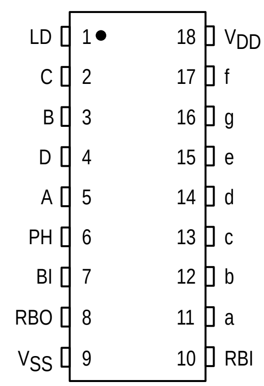
P SUFFIX
PLASTIC
CASE 707

ORDERING INFORMATION

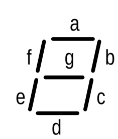
MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic

T_A = – 55° to 125°C for all packages.

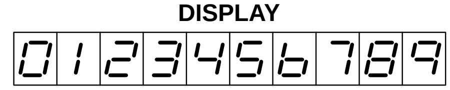
PIN ASSIGNMENT



1	LD	18	V_{DD}
2	C	17	f
3	B	16	g
4	D	15	e
5	A	14	d
6	PH	13	c
7	BI	12	b
8	RBO	11	a
9	V_{SS}	10	RBI



DISPLAY



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

REV 3
1/94

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage	“0” Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0			10	—	0.05	—	0	0.05	—	0.05	
			15	—	0.05	—	0	0.05	—	0.05	
	“1” Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage #	“0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	—	4.0	—	6.75	4.0	—	4.0	
	“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)			15	11	—	11	8.25	—	11	—	
Output Drive Current		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)			5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 0.5 Vdc)			10	—	—	—	– 10.1	—	—	—	
(V_{OH} = 9.5 Vdc)			10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)			15	– 4.2	—	– 3.4	– 8.8	—	– 2.4		
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 9.5 Vdc)			10	—	—	—	10.1	—	—	—	
(V_{OL} = 1.5 Vdc)			15	4.2	—	3.4	8.8	—	2.4		
Input Current		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current		I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
(Per Package) V_{in} = 0 or V_{DD},			10	—	10	—	0.010	10	—	300	
I_{out} = 0 µA			15	—	20	—	0.015	20	—	600	
Total Supply Current**†		I_T	5.0	I_T = (1.6 µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent,			10	I_T = (3.1 µA/kHz) f + I_{DD}							
Per Package)			15	I_T = (4.7 µA/kHz)f + I_{DD}							
(C_L = 50 pF on all outputs, all buffers switching)											

#Noise immunity specified for worst–case input combination.

Noise Margin for both “1” and “0” level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

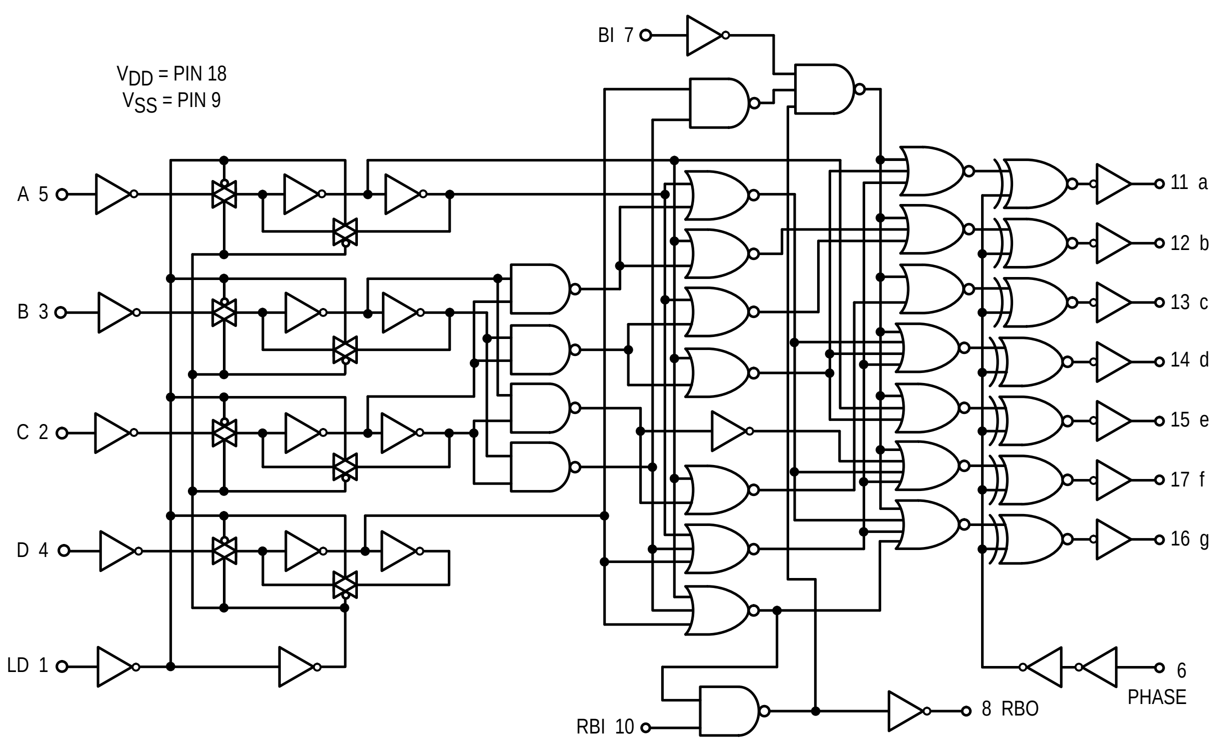
* The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	—	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	—	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	—	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	—	40	80	
Turn–Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 520 ns		5.0	—	605	1210	
t_{PLH} = (0.66 ns/pF) C_L + 217 ns		10	—	250	500	
t_{PLH} = (0.5 ns/pF) C_L + 160 ns		15	—	185	370	
Turn–On Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	—	505	1650	
t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	—	205	660	
t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	—	155	495	
Setup Time	t_{su}	5.0	0	– 40	—	ns
		10	0	– 15	—	
		15	0	– 10	—	
Hold Time	t_h	5.0	80	40	—	ns
		10	30	15	—	
		15	20	10	—	
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0	250	125	—	ns
		10	100	50	—	
		15	80	40	—	

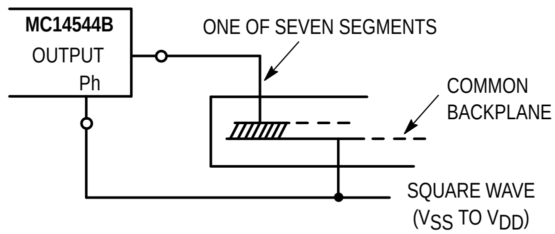
* The formulas given are for the typical characteristics only.

LOGIC DIAGRAM

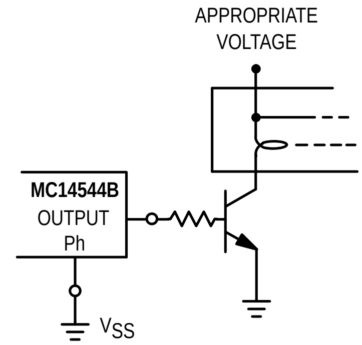


CONNECTIONS TO VARIOUS DISPLAY READOUTS

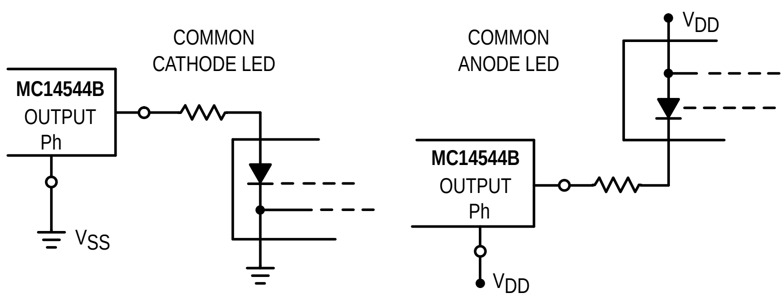
LIQUID CRYSTAL (LC) READOUT



INCANDESCENT READOUT

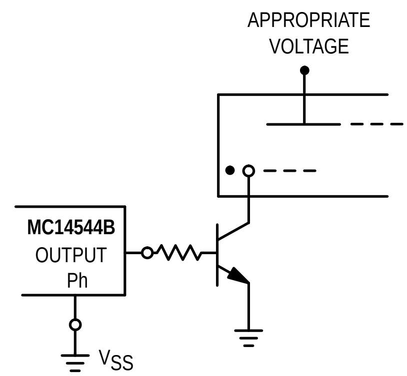


LIGHT EMITTING DIODE (LED) READOUT



NOTE: Bipolar transistors may be added for gain (for $V_{DD} \leq 10$ V or $I_{out} \geq 10$ mA).

GAS DISCHARGE READOUT



TRUTH TABLE

Inputs								Outputs								
RBI	**LD**	**BI**	**Ph***	**D**	**C**	**B**	**A**	**RBO**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**Display**
X	X	1	0	X	X	X	X	#	0	0	0	0	0	0	0	Blank
1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
X	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1
X	1	0	0	0	0	1	0	0	1	1	0	1	1	0	1	2
X	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1	3
X	1	0	0	0	1	0	0	0	0	1	1	0	0	1	1	4
X	1	0	0	0	1	0	1	0	1	0	1	1	0	1	1	5
X	1	0	0	0	1	1	0	0	1	0	1	1	1	1	1	6
X	1	0	0	0	1	1	1	0	1	1	0	0	0	0	0	7
X	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	8
X	1	0	0	1	0	0	1	0	1	1	1	1	0	1	1	9
X	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	0	0	0	X	X	X	X	#	**							**
†	†	†	1	†				†	Inverse of Output Combinations Above							Display as above

X = Don't Care

† Above Combinations

* For liquid crystal readouts, apply a square wave to Ph. For common cathode LED readouts, select Ph = 0. For common anode LED readouts, select Ph = 1.

** Depends upon the BCD Code previously applied when LD = 1.

RBO = RBI • ($\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$)

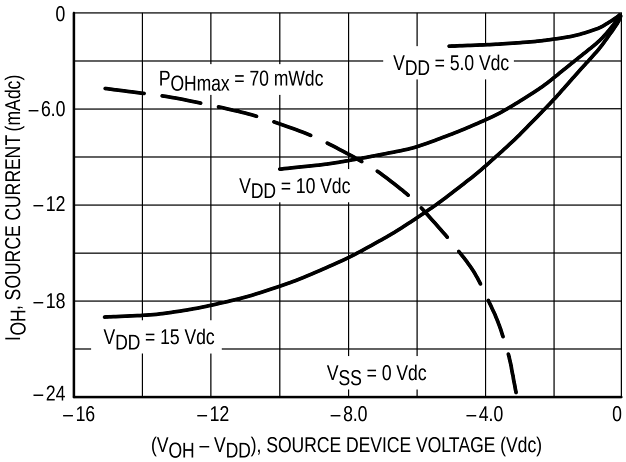


Figure 1. Typical Output Source Characteristics

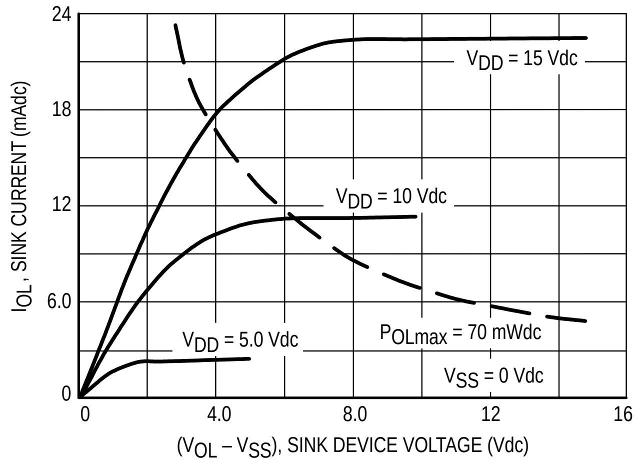


Figure 2. Typical Output Sink Characteristics

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

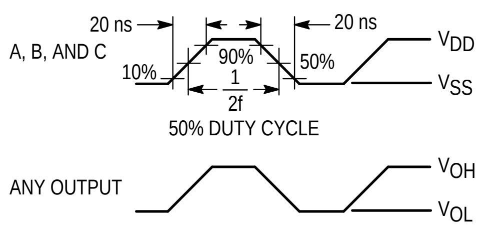


Figure 3. Dynamic Power Dissipation Signal Waveforms

(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.

(b) Inputs D, Ph, and BI low, and Inputs A and B high.

(c) Data DCBA strobed into latches

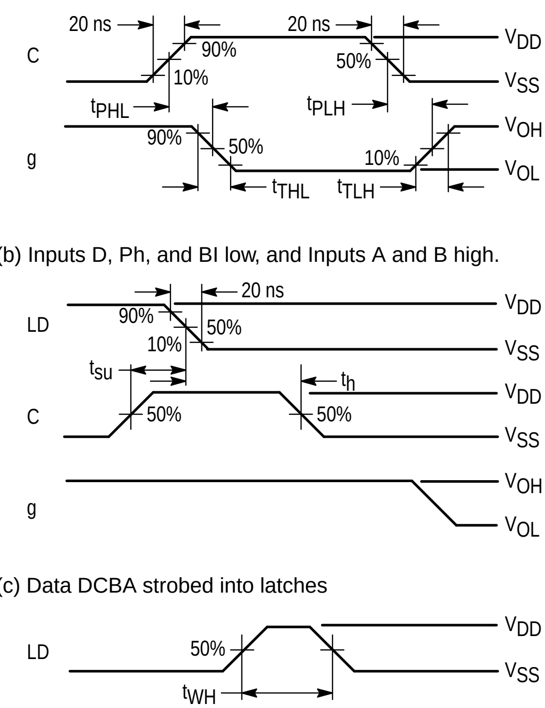
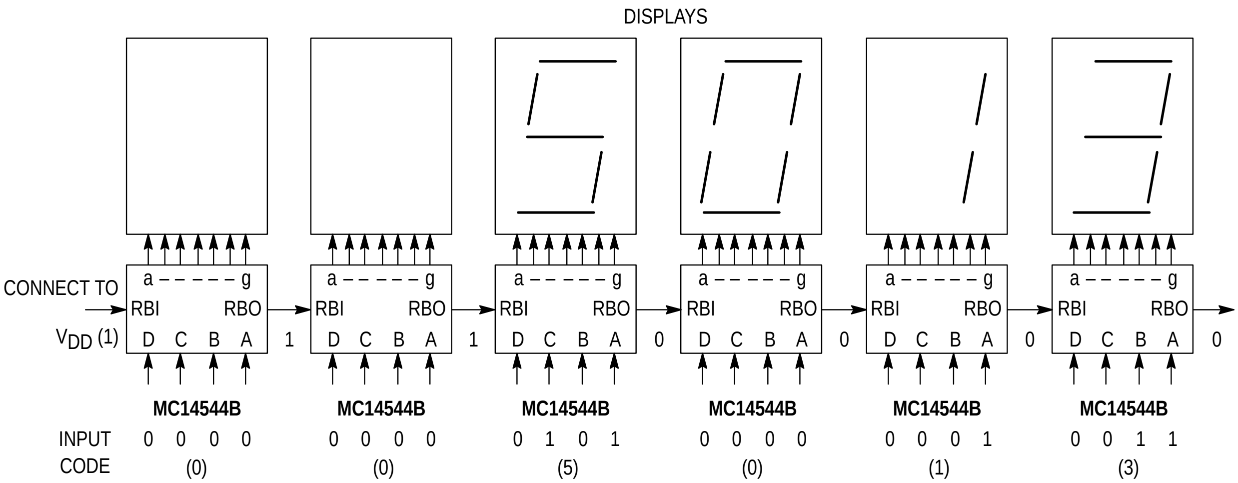


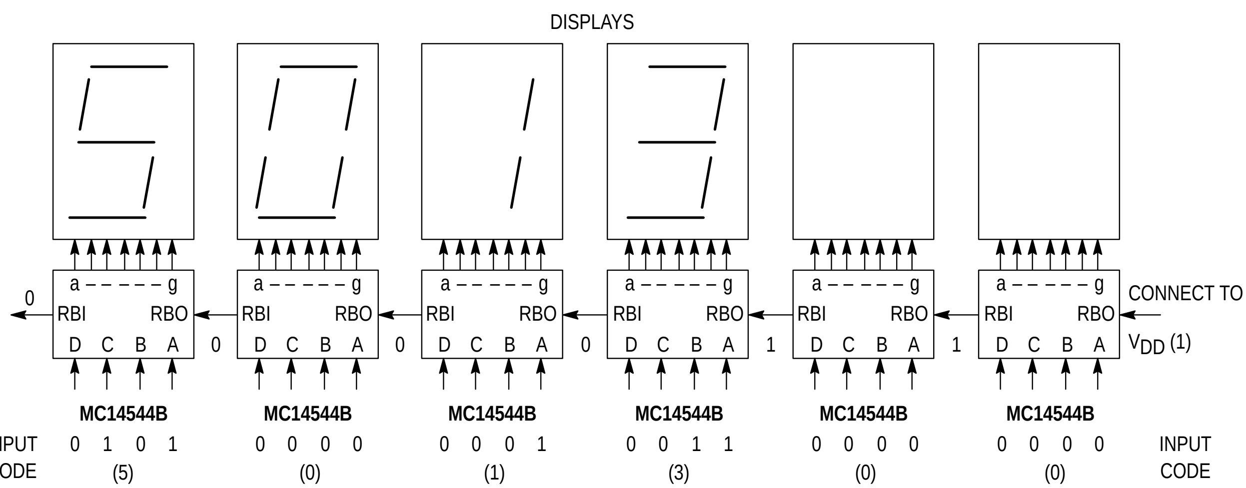
Figure 4. Dynamic Signal Waveforms

TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION

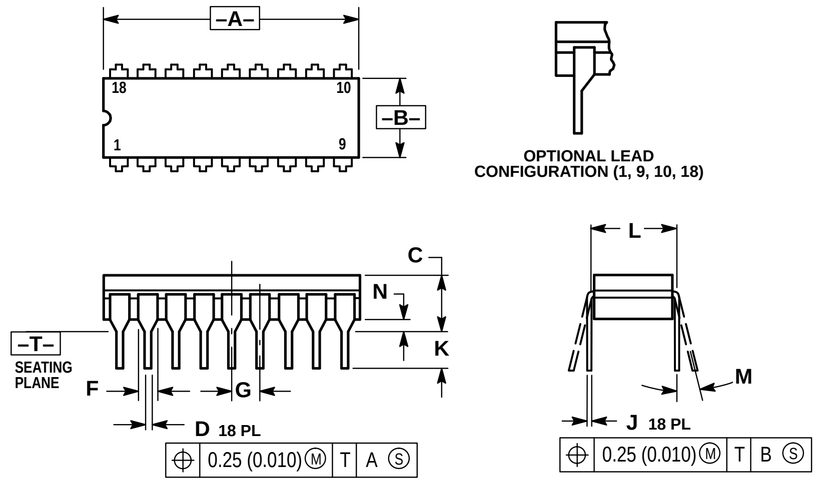


TRAILING EDGE ZERO SUPPRESSION



OUTLINE DIMENSIONS

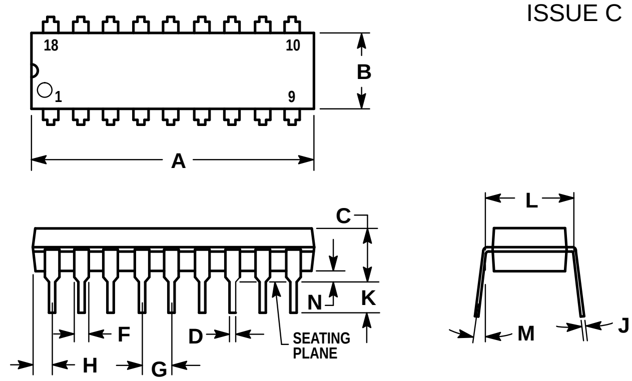
L SUFFIX
CERAMIC DIP PACKAGE
CASE 726–04
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.880	0.910	22.35	23.11
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.021	0.38	0.53
F	0.055	0.070	1.40	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.170	3.18	4.32
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

P SUFFIX
PLASTIC DIP PACKAGE
CASE 707–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298