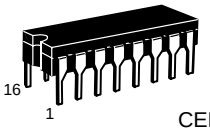
MC145402

Advance Information

Serial 13-Bit Linear Codec (A/D and D/A)



L SUFFIX
CERAMIC PACKAGE
CASE 620

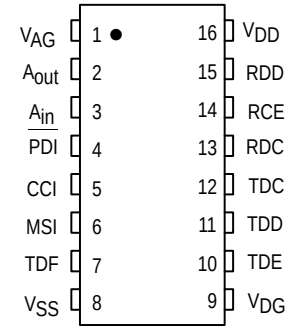
ORDERING INFORMATION

MC145402L Ceramic Package

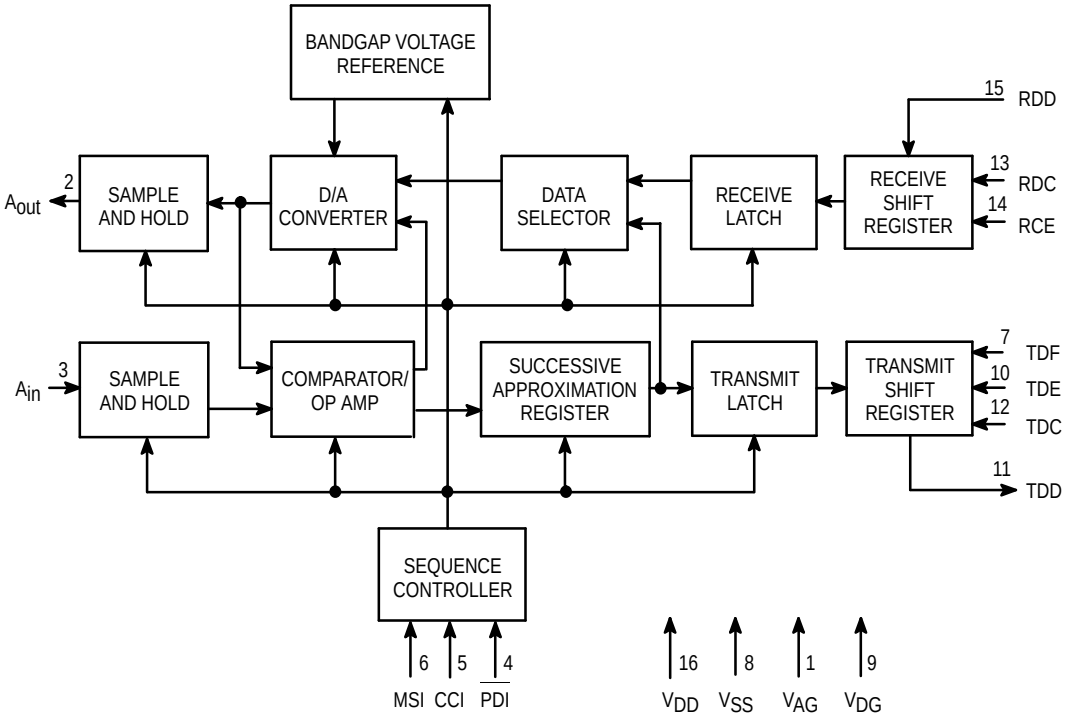
The MC145402 is a 13–bit linear monotonic digital–to–analog and analog–to–digital converter implemented in a single silicon–gate CMOS IC. Potential applications include analog interface for Digital Signal Processor (DSP) applications, high speed modems, telephone systems, SONAR, Adaptive Differential Pulse Code Modulation (ADPCM) converters, echo cancellers, repeaters, voice synthesizers, and music synthesizers.

- 60 dB Signal–to–(Noise Plus Distortion) Ratio Typical
- On–Chip Precision Voltage Reference
- Serial Data Ports
- Two's Complement Coding
- ± 5 V Supply Operation
- Sample Rates from 100 Hz to 16 kHz (Both A/D and D/A), 100 Hz to 21.3 kHz (A/D Only), and 100 Hz to 64 kHz (D/A Only)
- Input Sample and Hold Provided On–Chip
- 5 V CMOS Inputs; Outputs Capable of Driving Two LSTTL Loads
- Available in a 16–Pin DIP
- Low Power Consumption: 50 mW Typical, 1 mW Power–Down

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	– 0.5 to 11	V
Voltage, Any Pin to VSS	V	– 0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ on analog inputs/outputs and $V_{DG} \le (V_{in}$ or $V_{out}) \le V_{DD}$ on digital inputs/outputs. Reliability of operation is enhanced if unused digital inputs are tied to an appropriate logic voltage level (e.g., either V_{DG} or V_{DD}) and unused analog Inputs are tied to V_{AG}.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage	V_{DD} to V_{SS}	9.5	10	10.5	V
Power Dissipation, $\overline{PDI}$ = 1	V_{DD} to V_{SS}	—	50	80	mW
Power Dissipation, $\overline{PDI}$ = 0	V_{DD} to V_{SS}	—	1	5	mW
Conversion Rate Full Cycle A/D and D/A Short Cycle A/D Short Cycle D/A	MSI	0.1 0.1 0.1	— — —	16 21.3 64	kHz
Conversion Sequence Rate	CCI	3.2	—	512	kHz
Data Rate	TDC, RDC	16 x f_{MSI}	—	4096	kHz
Full Scale Analog Levels (Referenced to 600 Ω)	AI, AO	— —	3.27 9.5	— —	Vp dBm

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = – 5 V, V_{AG} = V_{DG} = 0 V, T_A = 0 to 70°C)

Characteristic			Symbol	Min	Max	Unit
High Level Input Voltage			V_{IH}	3.5	—	V
Low Level Input Voltage			V_{IL}	—	1.5	V
Input Current			I_{in}	—	± 1.0	μA
Input Capacitance			C_{in}	—	10	pF
High Level Output Voltage	TDD	I_{out} = – 20 μA I_{out} = – 1 mA	V_{OH}	4.9 4.3	— —	V
Low Level Output Voltage	TDD	I_{out} = – 20 μA I_{out} = – 1 mA	V_{OL}	— —	0.1 0.4	V

CODER AND DECODER PERFORMANCE (V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%, V_{AG} = V_{DG} = 0 V,
0 dBm0 = 1.60 Vrms = 6.30 dBm (600 Ω), T_A = 0 to 70°C, MSI = TDE = RCE = 8 kHz, TDC = RDC = 2.048 MHz, CCI = 256 kHz)

Characteristic		Coder (A/D)			Decoder (D/A)			Unit
		Min	Typ	Max	Min	Typ	Max	
Resolution		13	—	13	13	—	13	Bits
Conversion Time	Full Cycle A/D and D/A	62.5	—	10,000	62.5	—	10,000	µs
	Short Cycle A/D	46.9	—	10,000	—	—	—	
	Short Cycle D/A	—	—	—	15.6	—	10,000	
Differential Nonlinearity		—	—	± 1	—	—	± 1	LSB
Gain Error		– 0.35	—	+ 0.35	– 0.35	—	+ 0.35	dB
Offset		– 15	—	+ 15	—	—	—	LSB
		—	—	—	– 20	—	+ 20	mV
Idle Channel Noise, 3 kHz Low–Pass		—	– 75	—	—	– 79	—	dBm0
Signal–to–Noise	3.2 dBm0	—	61	—	—	62	—	dB
(Referenced to 1.02 kHz through	0 dBm0	—	60	—	—	60	—	
a f_{MSI}/2 Low–Pass Filter)	– 10 dBm0	—	57	—	—	59	—	
	– 20 dBm0	—	50	—	—	52	—	
	– 30 dBm0	—	40	—	—	42	—	
	– 40 dBm0	—	30	—	—	32	—	
	– 50 dBm0	—	20	—	—	22	—	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%, V_{AG} = V_{DG} = 0 V,
0 dBm0 = 1.60 Vrms = 6.30 dBm (600 Ω), T_A = 0 to 70°C, MSI = TDE = RCE = 8 kHz, TDC = RDC = 2.048 MHz, CCI = 256 kHz)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input Current	AI	I_{in}	—	0.01	± 1	µA
AC Input Impedance	AI	Z_{in}	0.5	—	—	MΩ
Input Capacitance	AI	C_{in}	—	—	15	pF
Output Voltage Range	AO	V_{out}	– 3.4	—	3.4	V
Power Supply Rejection Ratio (100 mV RMS on V_{DD} or V_{SS}, 0 – 50 kHz)	AO, TDD	PSRR	—	40	—	dB
Crosstalk, A_{in} to A_{out} and RDD to TDD Referenced to 0 dBm0 @ 1.02 kHz	AO, TDD	—	—	– 90	– 75	dB
Slew Rate	AO	SR	1.5	3	—	V/µs
Settling Time (Full Scale)	AO	t_{settle}	—	8	—	µs

SWITCHING CHARACTERISTICS

(V_{DD} = + 5 V ± 5%, V_{SS} = – 5 V ± 5%, V_{AG} = V_{DG} = 0 V, T_A = 0 to 70°C, C_L = 50 pF, See Figure 1)

Characteristic		Symbol	Min	Max	Unit
Input Rise Time	RCE, RDC, TDC, TDE, CCI, MSI	t_r	—	100	ns
Input Fall Time	RCE, RDC, TDC, TDE, CCI, MSI	t_f	—	100	ns
Output Rise Time	TDD	t_r	—	80	ns
Output Fall Time	TDD	t_f	—	80	ns
Pulse Width High	RDC, MSI, CCI, TDC, RCE	t_{wH}	100	—	ns
Pulse Width Low	TDE, MSI, TDC, RCE, RDC	t_{wL}	100	—	ns
CCI Pulse Width Low		t_{wL}	500	—	ns
MSI Clock Frequency		f_{MSI}	0.1	64	kHz
CCI Clock Frequency		f_{CCI}	3.2	512	kHz
TDC and RDC Clock Frequency		f_{DC}	16 x f_{MSI}	4.1	MHz
TDC Rising Edge to TDD Data Valid During TDE High		t_{p1}	—	150	ns
TDE Rising Edge to TDD Data Valid During TDC High		t_{p2}	—	150	ns
TDE Rising Edge to TDD Low–Impedance Propagation Delay		t_{p3}	0	100	ns
TDE Falling Edge to TDD High–Impedance Propagation Delay		t_{p4}	—	40	ns
TDE Rising Edge to TDC Falling Edge Setup Time		t_{su1} t_{su2}	20 100	— —	ns
RDC Bit 0 Falling Edge to Last CCI Falling Edge Prior to MSI		t_{su3}	20	—	ns
MSI Rising Edge to CCI Falling Edge Setup Time		t_{su4} t_{su5}	20 100	— —	ns
Last CCI Rising Edge (Prior to MSI) to TDE Rising Edge		t_{su6}	100	—	ns
Last CCI Rising Edge (Prior to MSI) to First TDC Rising Edge		$t_{su6'}$	100	—	ns
First TDC Falling Edge to Last CCI Rising Edge Prior to MSI		t_{su7}	0	—	ns
RCE Rising Edge to RDC Falling Edge Setup Time		t_{su8} t_{su9}	20 100	— —	ns
RDD Valid to RDC Falling Edge Setup Time		t_{su10}	60	—	ns
RDD Hold Time from RDC Falling Edge		t_h	100	—	ns

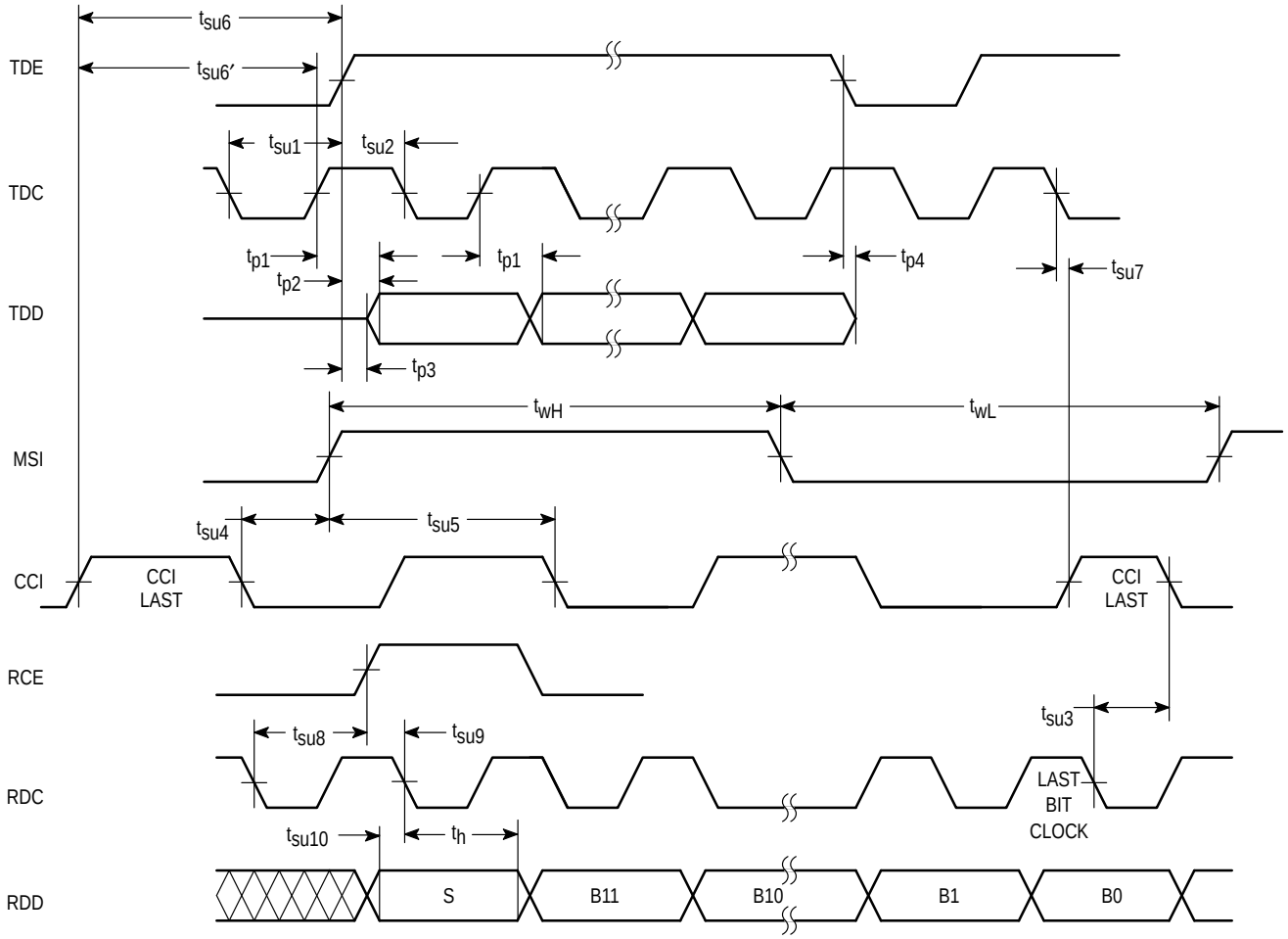


Figure 1. AC Timing Diagram

PIN DESCRIPTIONS

V_{DD}
Positive Supply (Pin 16)

The most positive power supply, typically + 5 V in split power supply configurations, or + 10 V in single supply systems.

V_{SS}
Negative Supply (Pin 8)

The most negative power supply, typically – 5 V in split power supply configurations, or 0 V in single supply systems.

V_{AG}
Analog Ground (Pin 1)

This is the analog signal reference point. This pin is normally tied to 0 V in split supply operation or $V_{DD}/2$ in single supply systems.

V_{DG}
Digital Ground (Pin 9)

This is the ground reference for all of the digital input and output pins. CMOS compatible logic signals swing from V_{DG} to V_{DD} where V_{DG} can be established anywhere from V_{DD} – 4.75 V to V_{SS}.

A_{out}
Analog Output (Pin 2)

This is the output of the decoder's sample and hold circuit and is a 100% duty cycle analog output of the last digital word received and decoded by the decoder. A_{out} is updated approximately 60 ns after the rising edge of the last CCI prior to MSI (see Figure 2). A_{out} is capable of driving a 10 kΩ, 50 pF load.

A_{in}
Analog Input (Pin 3)

This is the high–impedance input to the coder. An A/D cycle begins on the first falling edge of CCI following the rising edge of MSI. A_{in} is sampled approximately 50 ns after the rising edge of CCI prior to the start of the A/D cycle.

$\overline{PDI}$
Power–Down Input (Pin 4)

In normal operation this Input should be tied high. A logic low on this input puts the device into a minimum power dissipation mode. During power–down, all functions stop. Two complete MSI conversion cycles are required to establish normal operation after leaving the power–down mode.

CCI
Convert Clock Input (Pin 5)

This input controls the complete conversion sequence during one MSI cycle and must receive a clock which is 32 times the frequency of MSI. The only exception to 32 times the frequency of MSI is during short–cycle operation. See **General Modes of Operation** section. CCI must be synchronous and approximately rising edge aligned with MSI.

MSI
Master Sync Input (Pin 6)

This pin determines the conversion rate for both the coder and the decoder. One A/D and D/A conversion takes place during each period of the digital clock applied to this input (except in short–cycle operation, see **General Modes of Operation** section). MSI must be synchronous and approximately rising edge aligned with CCI.

TDC
Transmit Data Clock (Pin 12)

Digital data from the coder is serially transmitted from TDD on rising TDC edges whenever TDE is a logic high. TDC must be approximately rising edge aligned with TDE. Generally, if TDC is low when TDE rises, the first rising edge of TDC clocks the first data bit. If TDC is high when TDE rises, the first bit will be clocked by TDE and the first rising edge of TDC after TDE rises will clock out the second data bit.

TDE
Transmit Data Enable (Pin 10)

This pin is used to initiate the serial transfer of data from the coder and provides three–state control of the TDD pin. The rising edge of TDE (or TDC if it follows TDE) signals the start of data transfer from the TDD pin. A resulting high logic level on TDE also releases TDD from its high–impedance state. TDE must remain high throughout the data transfer to keep TDD in the low–impedance state and must return to a low state prior to each data transfer. If TDE remains high for more than 16 TDC clocks, the 16 bits of TDD data will be recirculated. (Note: The A/D cycle begins on the first falling edge of CCI after the rising edge of MSI. The internal transmit latch is updated one and one half CCI periods prior to the start of the A/D cycle. A pulse generated by the logical AND of TDE and the first TDC transfers data to the transmit shift register, and this pulse must not occur when the transmit latch is updated. See Figure 2 and see t_{su6}, $t_{su6'}$, and t_{su7} of Figure 1.

TDD
Transmit Digital Data (Pin 11)

This is the three–state output data pin from the coder and is controlled by the TDE and TDC pins. TDD is in the high–impedance state whenever TDE is a logic low. The first data bit is output from TDD on the rising edge of TDE (or TDC if it follows TDE) and each subsequent bit is output on rising edges of TDC. Two output data formats are available as described in the TDF pin description below.

TDF
Transmit Data Format (Pin 7)

The 13–bit digital output of the coder is available in one of two 16–bit two's complement formats as determined by the state of this pin. A logic 0 at this pin causes the data from TDD to be in a 16–bit sign–extended format as follows: SSSSM ... L where S, M, and L represent the sign, most significant bit, and the least significant bit, respectively. A logic 1 on this pin formats the data as follows: SM ... LSSS (see Figure 3). RDD data is not affected by the state of this pin and if a "digital loopback" is needed (TDD data looped back into RDD), this pin should be high.

RDC
Receive Data Clock (Pin 13)

Receive digital data is accepted by the decoder on the first 13 falling edges of RDC after an RCE rising edge.

RCE
Receive Clock Enable (Pin 14)

This pin identifies the beginning of a data transfer into the RDD pin of the decoder. The first 13 falling edges of RDC after an RCE rising edge will clock data into the decoder data input, RDD. RCE must return low prior to each data transfer. Since receive data is latched into the receive latch on the last CCI falling edge prior to MSI, data transfers may not span this falling edge of CCI without loss of data.

RDD
Receive Digital Data (Pin 15)

This pin is the data input to the decoder and is controlled by the RDC and RCE pins described above. Two's complement data are loaded in the following sequence: SM ... L where S, M, and L represent the sign, most significant bit, and the least significant bit, respectively. Only the first 13 bits clocked by RDC after RCE rises will be accepted for decoding. Any additional bits will be ignored (see Figure 3).

GENERAL INFORMATION

GENERAL MODES OF OPERATION

The MC145402 has three modes of operation; a "full" cycle mode and two ''short" cycle modes. The full cycle mode allows simultaneous analog–to–digital (A/D) and digital–to–analog (D/A) operation. The short cycle modes allow either A/D only or D/A only operation. Two MSI cycles are required for the MC145402 to detect which operating mode has been selected. See Figure 2 for full versus short cycle clocking.

Full Cycle Operation

When operating in the full cycle mode, the MC145402 performs a 13–bit A/D conversion followed by a 13–bit D/A con–version. Full cycle operation is selected by using a CCI frequency that is 32 times the frequency of MSI. MSI is the sample rate frequency.

Short Cycle Analog–to–Digital Operation

If CCI is 24 times the frequency of MSI, short cycle analog–to–digital operation is selected. This allows a 13–bit A/D conversion only. In this mode, the D/A is not operational and any data applied to the RDD input is ignored.

Short Cycle Digital–to–Analog Operation

Short cycle digital–to–analog operation is selected by using a CCI clock frequency that is eight times the MSI sample rate. During short cycle D/A operation, A/D operation is disabled and digital data read from TDD is not valid.

CLOCKING RECOMMENDATIONS

For optimum differential nonlinearity performance, all data transitions on TDD and RDD should be limited to the first four CCI cycles following the rising edge of MSI. This may be achieved by setting MSI = TDE = RCE having a duration of 16 data clock cycles, and TDC = RDC ≥ 4 x CCI clock frequency. Figure 6 shows a circuit that generates this clocking configuration; see **Application Circuits** section.

SIGNAL TO DISTORTION RATIO

Figures 4 and 5 show graphs of typical signal to distortion ratios versus signal level for the MC145402. The presented data is referenced to a 1020 Hz input sinusoidal frequency with signal levels referenced to 600 Ω and transmission level point adjusted (e.g., 0 dBm0 at 600 Ω with a TLP of 6.30 dB is 4.53 V peak–to–peak). For comparison, ideal signal to noise ratios for 9–, 10–, 11–, 12–, and 13–bit A/D and D/A converters are also shown. The equation used for an ideal RMS to RMS signal to distortion ratio is:

$$S/D = N \times 6\ dB + 1.76\ dB$$

where N is the number of bits of resolution, 6 dB per bit, and $1.76 = 20_{log}\ (\sqrt{3}/\sqrt{2})$.

$(\sqrt{3}/\sqrt{2})$ is approximately the RMS to RMS ratio of a sine wave to white noise.

The signal to noise plus distortion ratio is measured through a brickwall low–pass filter set to the Nyquist frequency of the A/D and D/A sample rate. For an 8 kHz sample rate, the low–pass filter is set to block all signals above 4 kHz.

APPLICATION CIRCUITS

Figure 6 shows a typical circuit for generating the clock frequencies for the MC145402. This circuit uses an MC74HC4040 and a 2.048 MHz crystal to generate the 256 kHz frequency for internal sequencing, 1.024 MHz for the date clocks, and an 8 kHz sample frequency. A 4.096 MHz crystal could be used for a sample rate of 16 kHz.

Figure NO TAG shows the MC145402 interfaced to the DSP56000 digital signal processor. The DSP56000 can internally generate the clocks for the MC145402 using the SSI serial interface. SCK provides the sequencing and data clocks (non–gated continuous dock) and SC2 (setup as the Frame Sync Out, FSL = 0) provides the sample rate and data enables for the MC145402. The divide–by–four circuit to generate the CCI clock is recommended for optimum MC145402 performance, and allows the DSP56000 to clock data in and out of the MC145402 quickly, leaving time available for processing by the DSP before another sample is available. SC0 and SC1 could be used to gate the enables to select up to four devices on the SSI bus.

TELEPHONE SYSTEM TRANSMISSION LEVEL POINT FOR A LINEAR A/D OR D/A CONVERTER REFERENCED TO MU–LAW COMPANDING

Mu–Law companding, as specified by AT&T and CCITT, requires 8159 quantization levels to implement both A/D and D/A conversion schemes. This is to be mirrored about signal ground for the negative part of the wave form.

To implement a 13–bit (± 12–bit) linear converter scheme requires 8192 quantization levels mirrored about signal ground. To specify this converter such that it can be used to interface with, or as an alternative to, telephony based Mu–Law applications, the following is an explanation of the gain translation.

A 13–bit linear converter scheme has 8192 quantization levels. The goal is to be able to convert between these two encoding schemes with minimal distortion. This dictates setting the LSBs to the same level. For this to be achieved requires the reference voltage of the linear converter to be

8192/8159 times the reference voltage of the Mu–Law converter. The peak amplitude of a Mu–Law converter is 3.17 dBm0. The peak level of the linear converter will be 8192/8159 times the peak level of the Mu–Law converter, which is 8192/8159 x 3.17 dBm0. However, you cannot multiply a gain factor by a dBm value without using common term units and math (i.e., we must convert this gain factor to a dB equivalent), which is:

$$20 \log_{10} (8192/8159) = 0.03 \text{ dB}$$

With the gain factor in dB, we can add it to the Mu–Law peak level:

$$3.17 \text{ dBm0} + 0.03 \text{ dB} = 3.20 \text{ dBm0}$$

Therefore, the linear converter peak level is 3.20 dBm0.

This is another way of saying the 0 dBm0 level for the linear converter is 3.20 dB below the maximum amplitude.

To determine the absolute 0 dBm0 level for the linear converter from the peak level, we calculate the peak level in dBm by:

$$10 \log_{10} \frac{3.27 \text{ VpK} / \sqrt{2}) / (600\ \Omega)}{1 \text{ mW}} = 9.50 \text{ dBm } (600\ \Omega)$$

and 3.20 dB below this level is the 0 dBm0 absolute amplitude, which is

$$9.50 \text{ dBm} - 3.20 \text{ dB} = 6.30 \text{ dBm } (600\ \Omega)$$

Therefore, the calibration level, or transmission level point (TLP), for this part is 6.30 dBm (600 Ω), which is 1.6 Vrms based on the reference voltage of 3.27 V.

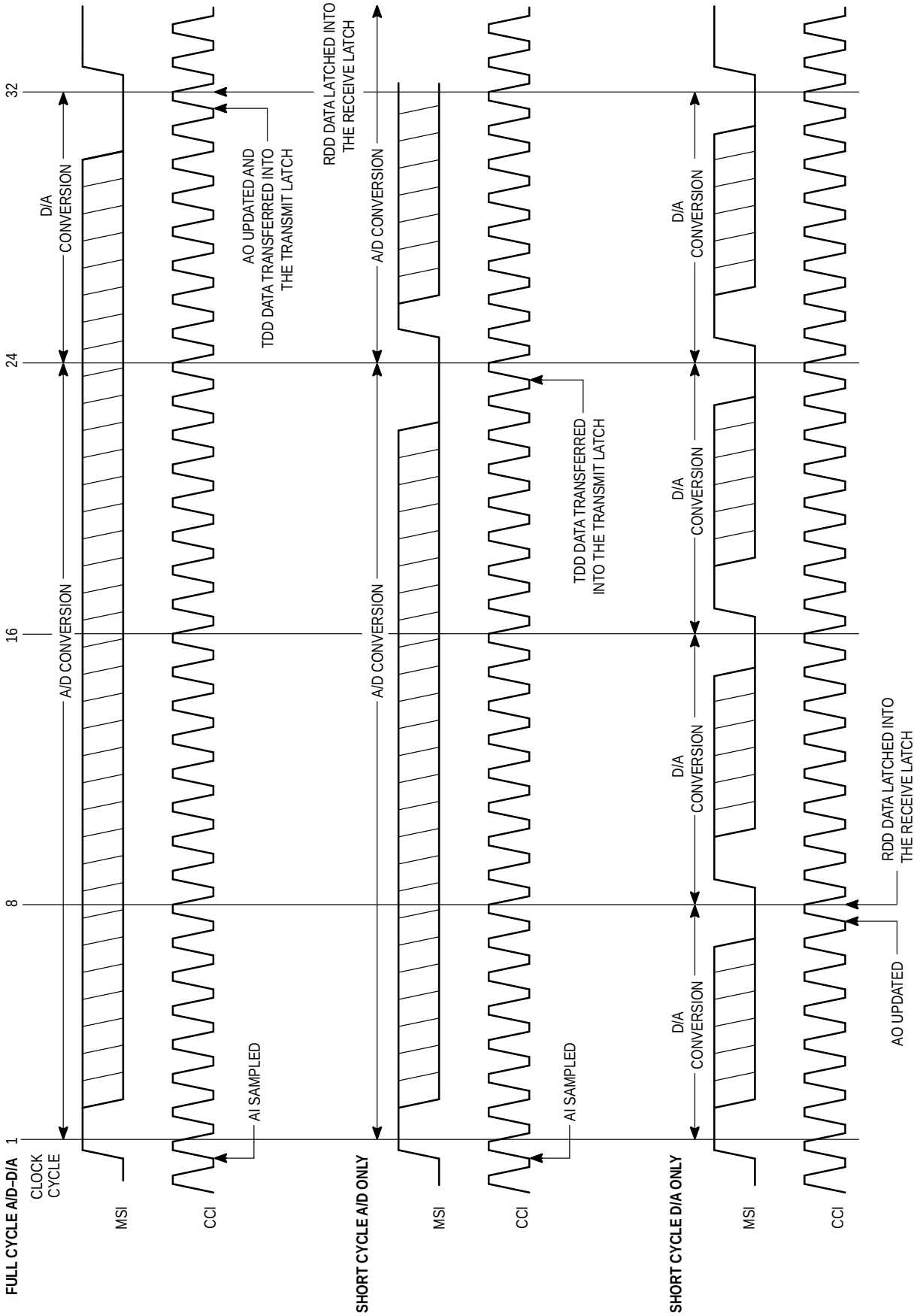


Figure 2. MC145402 Full and Short Cycle Timing

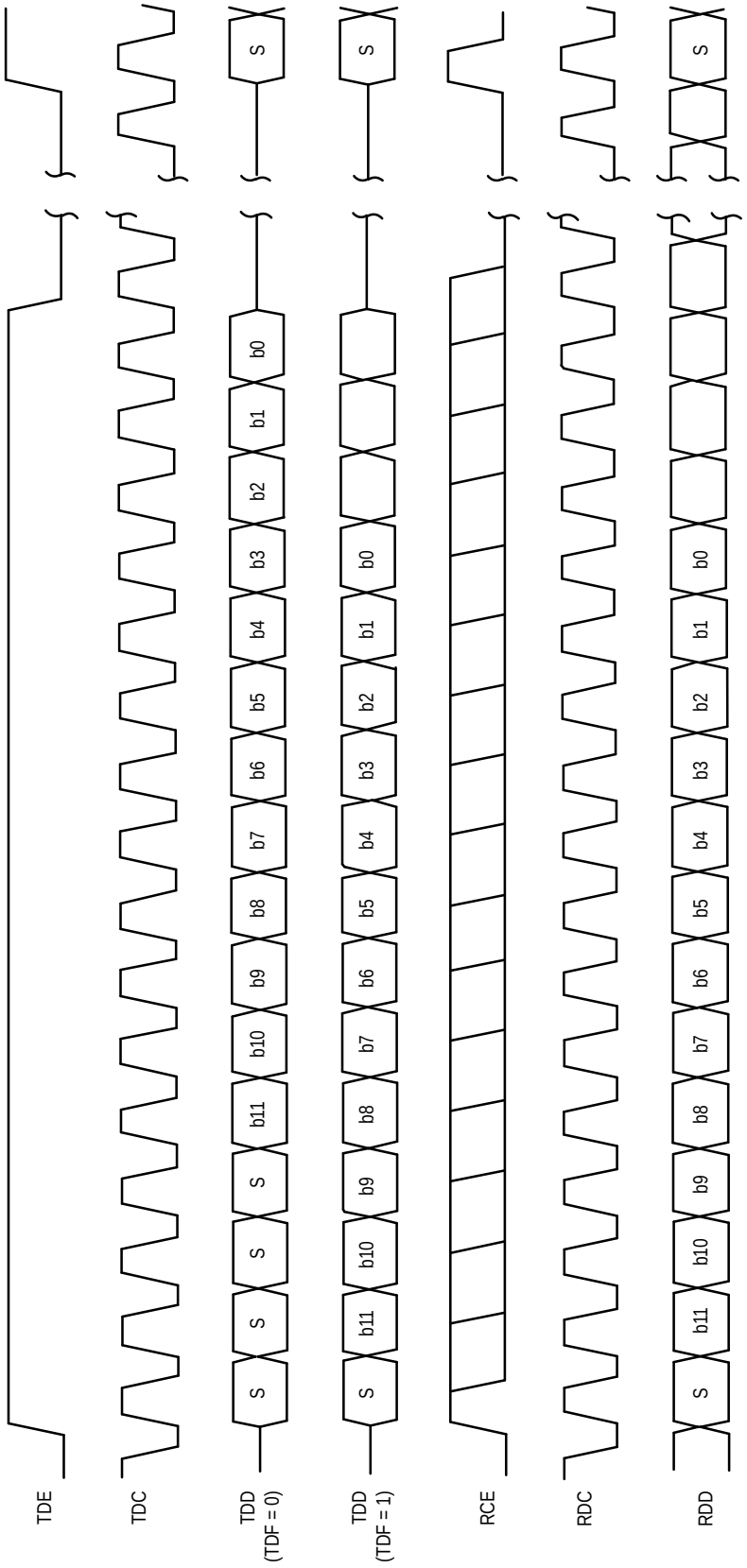


Figure 3. MC145402 Digital Data Timing

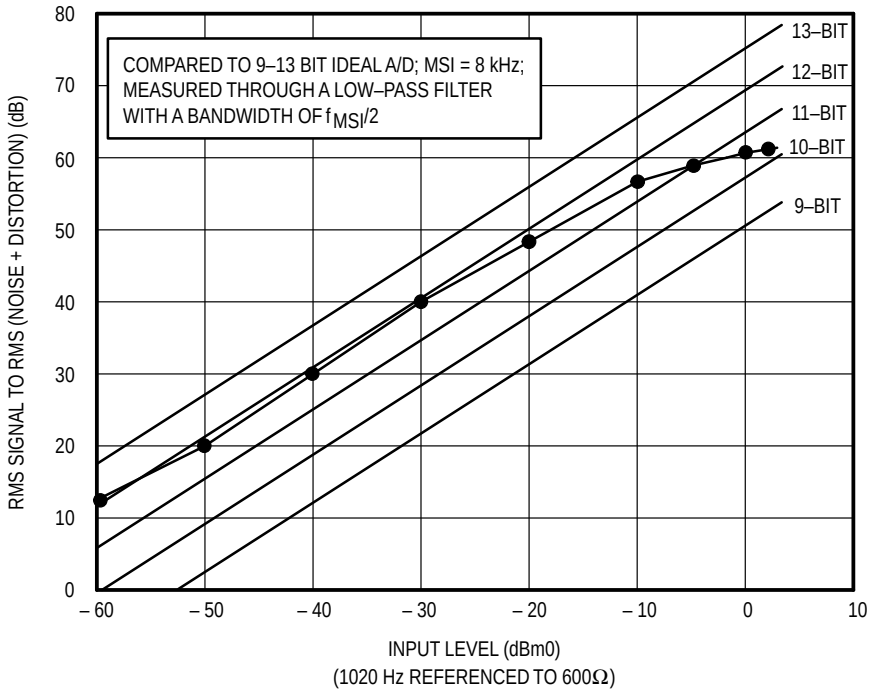


Figure 4. MC145402 Encoder (A/D) Signal to Noise Plus Distortion Ratio

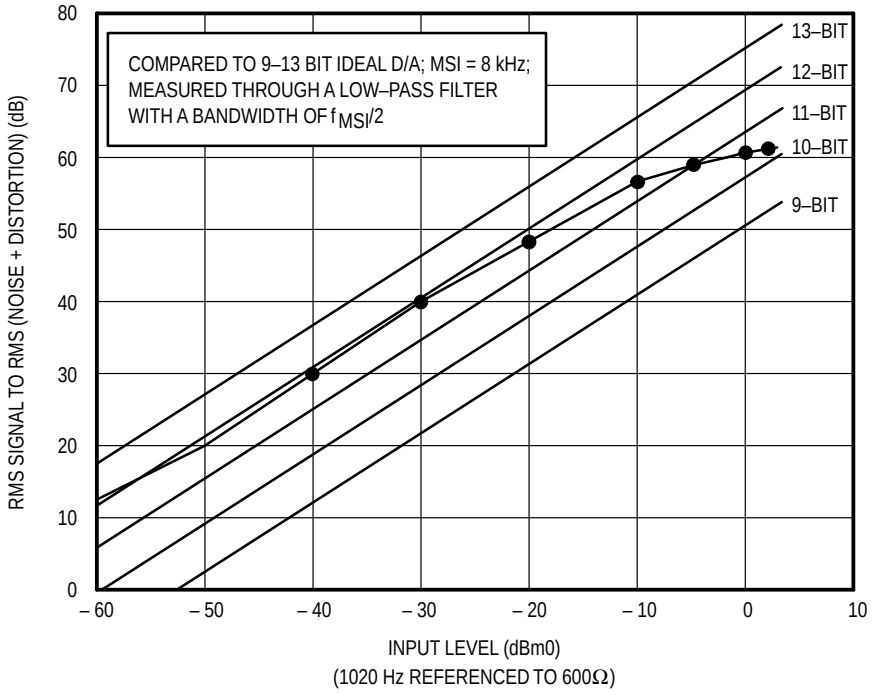


Figure 5. MC145402 Decoder (D/A) Signal to Noise Plus Distortion Ratio

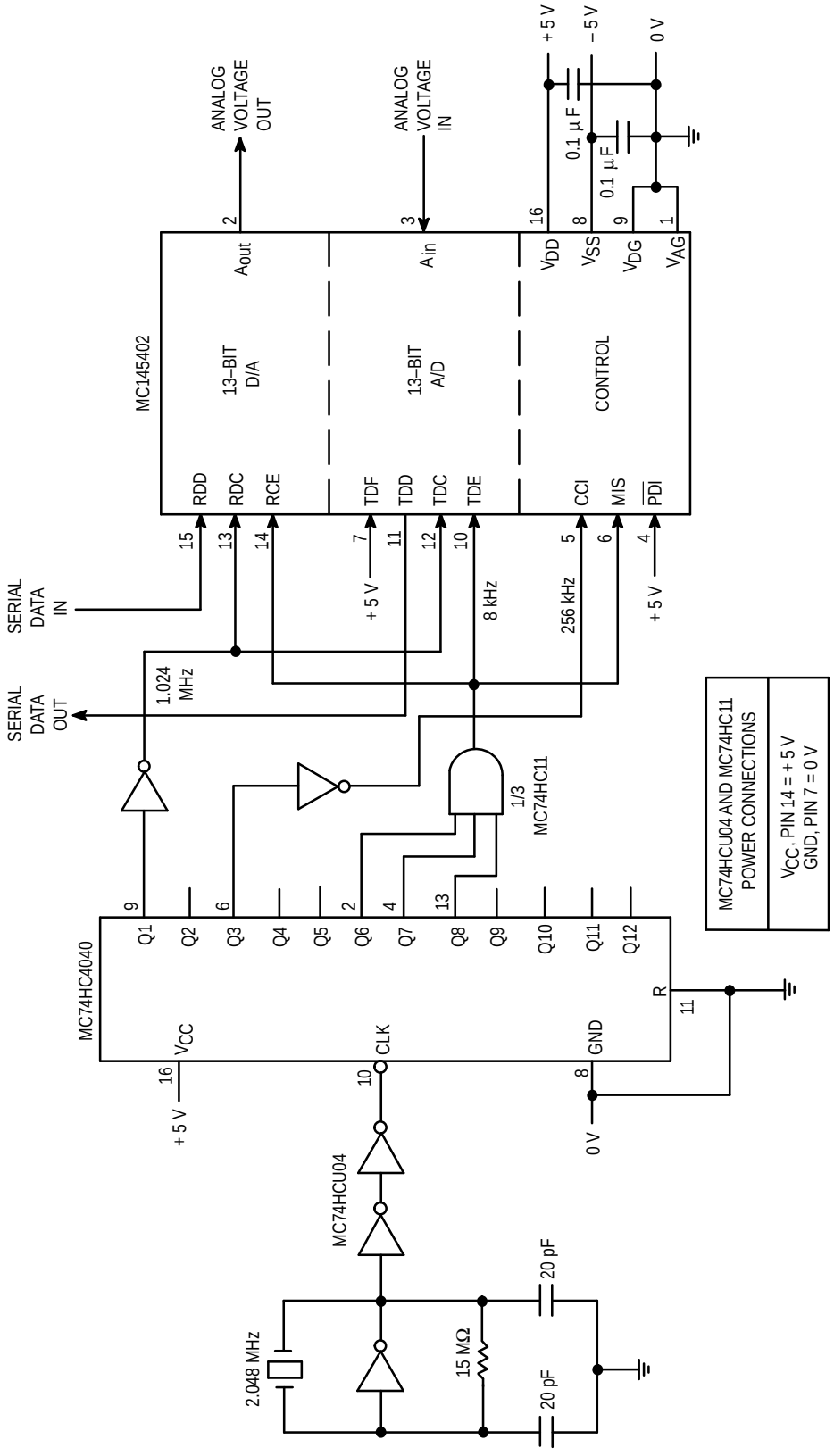


Figure 6. Typical MC145402 Configuration

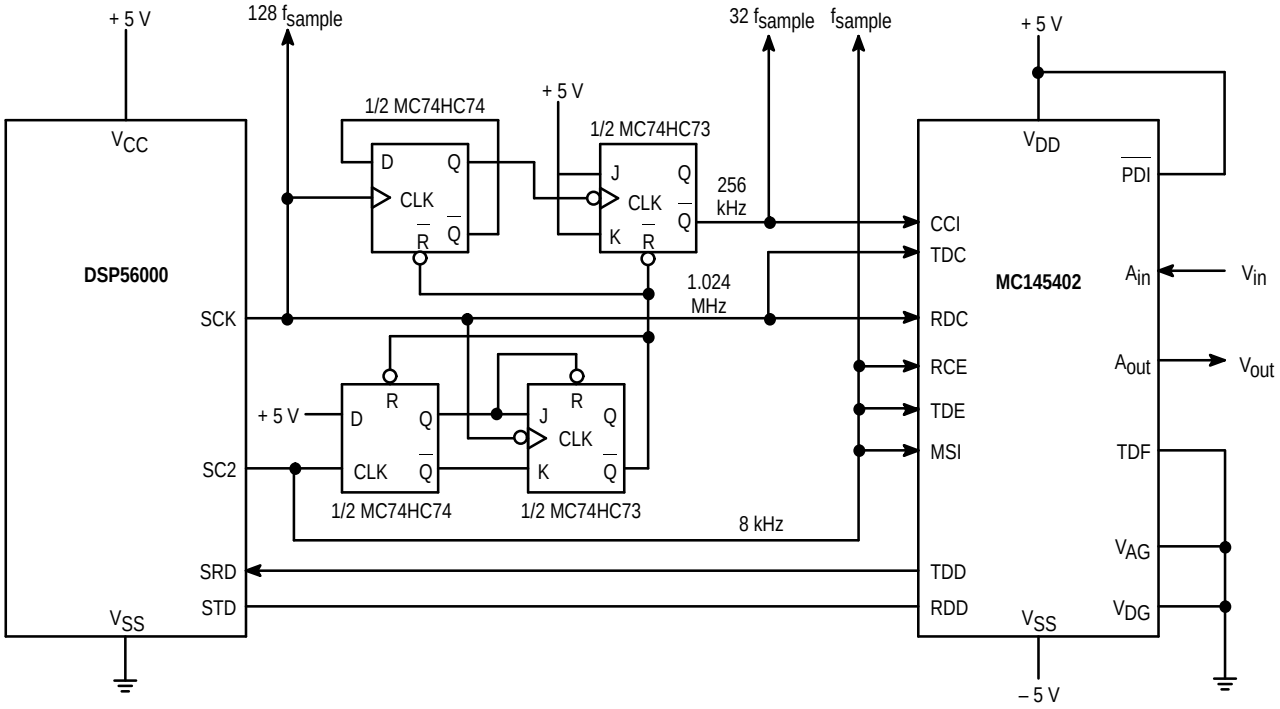
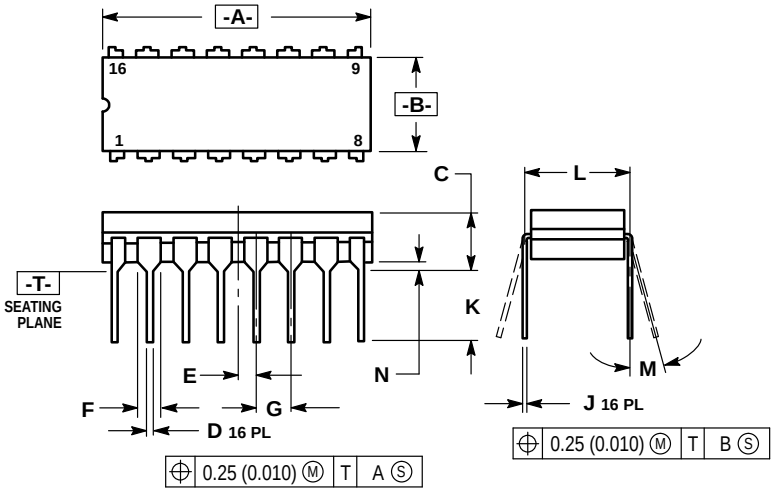


Figure 7. The MC145402, 13–Bit Linear Codec, Interfaced to a Motorola DSP56000, Digital Signal Processor, SSI Port

PACKAGE DIMENSIONS

L SUFFIX
CERAMIC
CASE 620–09



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.770	19.05	19.55
B	0.240	0.290	6.10	7.36
C	—	0.165	—	4.19
D	0.015	0.021	0.39	0.53
E	0.050 BSC		1.27 BSC	
F	0.055	0.070	1.40	1.77
G	0.100 BSC		2.54 BSC	
J	0.009	0.011	0.23	0.27
K	—	0.200	—	5.08
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.035	0.39	0.88

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