# **12-Bit Parity Tree**

The MC14531B 12–bit parity tree is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data–bit inputs (D0 thru D11), and even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12–bits can be accommodated by cascading other MC14531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Variable Word Length
- · Diode Protection on All Inputs

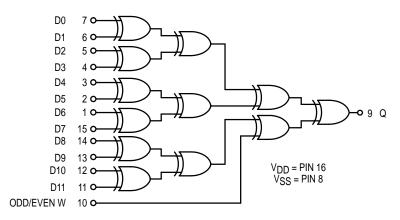
## MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

<sup>\*</sup> Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating:

Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

#### LOGIC DIAGRAM



 $Q = D0 \oplus D1 \oplus D2 \oplus \cdots \oplus D11 \oplus W$ 

# MC14531B



L SUFFIX CERAMIC CASE 620



P SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751B

#### ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

 $T_A = -55^{\circ}$  to 125°C for all packages.

## **TRUTH TABLE**

Inputs								Output
w	D11	D10		D2	D1	D0	Decimal (Octal) Equivalent	Q*
0	0	0		0	0	0	0 (0)	0
0	0	0		0	0	1	1 (1)	1
0	0	0		0	1	0	2 (2)	1
0	0	0		0	1	1	3 (3)	0
0	0	0		1	0	0	4 (4)	1
0	0	0		1	0	1	5 (5)	0
0	0	0		1	1	0	6 (6)	0
0	0	0		1	1	1	7 (7)	1
*	*	*	*	*	*	*	*	*
*	*	*	l	*	*	*	*	*
*	*	*	*	*	*	*	*	*
1	1	1.		0	0	0	8184 (17770	) 0
1	1	1		0	0	1	8185 (17771	) 1
1	1	1		0	1	0	8186 (17772	) 1
1	1	1		0	1	1	8187 (17773	) 0
1	1	1		1	0	0	8188 (17774	) 1
1	1	1		1	0	1	8189 (17775	0
1	1	1		1	1	0	8190 (17776	
1	1	1		1	1	1	8191 (17777	) 1

\*0 = Even Parity 1 = Odd Parity

NOTE: May redefine to suit application by manipulating W and/or other available D's.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

			V <sub>DD</sub>	- 55°C		25°C			125°C		
Characteristic		Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level	VOL	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
$V_{in} = 0$ or $V_{DD}$	"1" Level	VOH	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level	V <sub>I</sub> L	5.0 10 15	_ _ _	1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	Vdc
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level	VIH	5.0 10 15	3.5 7.0 11	_	3.5 7.0 11	2.75 5.50 8.25	_	3.5 7.0 11	=	Vdc
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	ІОН	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	_ _ _ _	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	_ _ _ _	- 1.7 - 0.36 - 0.9 - 2.4	_ _ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	lOL	5.0 10 15	0.64 1.6 4.2	_ _ _	0.51 1.3 3.4	0.88 2.25 8.8	_ _ _	0.36 0.9 2.4	_ _ _	mAdc
Input Current		l <sub>in</sub>	15	_	± 0.1	_	±0.00001	± 0.1	_	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)		C <sub>in</sub>	_	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)		IDD	5.0 10 15	_ _ _	5.0 10 20	=	0.005 0.010 0.015	5.0 10 20	_ _ _	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiesco Per Package) (C <sub>L</sub> = 50 pF on all outp buffers switching)	·	ΙΤ	5.0 10 15			$I_T = (0$	.25 μA/kHz) .50 μA/kHz) .75 μA/kHz)	f + I <sub>DD</sub>	•		μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$  Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

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<sup>\*\*</sup> The formulas given are for the typical characteristics only at 25  $^{\circ}\text{C}.$ 

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

# SWITCHING CHARACTERISTICS\* ( $C_L = 50 \text{ pF}, T_A = 25^{\circ}C$ )

Characteristic	Symbol	V <sub>DD</sub>	Min	Тур#	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL}$ = (1.6 ns/pF) $C_L$ + 25 ns $t_{TLH}$ , $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns $t_{TLH}$ , $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns	tTLH, tTHL	5.0 10 15	_ _ _	100 50 40	200 100 80	ns
Propagation Delay Time Data to Q  tp_H, tpHL = (1.7 ns/pF) C <sub>L</sub> + 355 ns  tp_H, tpHL = (0.66 ns/pF) C <sub>L</sub> + 142 ns  tp_H, tpHL = (0.5 ns/pF) C <sub>L</sub> + 95 ns  Odd/Even to Q	tPLH, tPHL	5.0 10 15	_ _ _	440 175 120	1320 525 360	ns
$t_{PLH}$ , $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 165 ns $t_{PLH}$ , $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 67 ns $t_{PLH}$ , $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 45 ns		5.0 10 15	_ _ _	250 100 70	750 300 210	

<sup>\*</sup> The formulas given are for the typical characteristics only at 25°C.

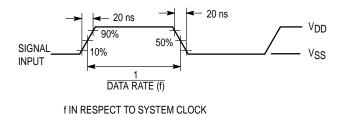


Figure 1. Dynamic Power Dissipation Signal Waveform

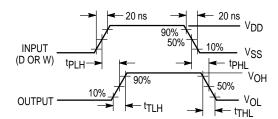
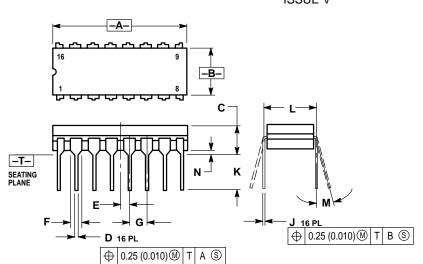


Figure 2. Dynamic Signal Waveforms

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# **OUTLINE DIMENSIONS**

# **L SUFFIX** CERAMIC DIP PACKAGE CASE 620-10 ISSUE V



#### NOTES:

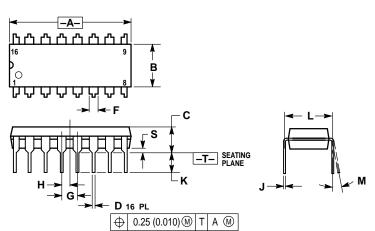
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

- ANSI Y14.5M, 1982.
  CONTROLLING DIMENSION: INCH.
  DIMENSION L TO CENTER OF LEAD WHEN
  FORMED PARALLEL.
  DIMENSION F MAY NARROW TO 0.76 (0.030)
  WHERE THE LEAD ENTERS THE CERAMIC

	INC	HES	MILLIN	IETERS	
DIM	MIN	MIN MAX		MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
С		0.200		5.08	
D	0.015	0.020	0.39	0.50	
Е	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	) BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62	BSC	
М	0°	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	

# **P SUFFIX**

PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: INCH.

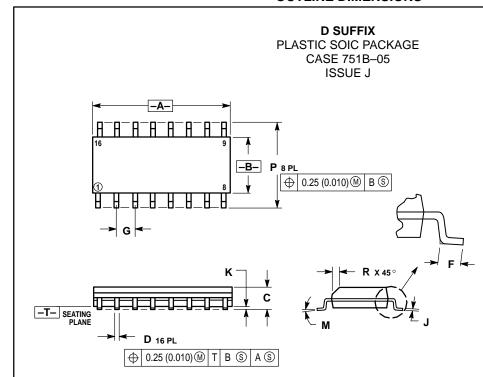
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

  5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10°	0°	10 °	
S	0.020	0.040	0.51	1.01	

### **OUTLINE DIMENSIONS**



- DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

  MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
М	0°	7°	0°	7°	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

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