MC145190EVK
MC145191EVK
MC145200EVK
MC145201EVK

Technical Summary

MC145190, MC145191, MC145200 and MC145201 Evaluation Board Manual

INTRODUCTION

The MC145190EVK, ’191EVK, ’200EVK, and ’201EVK are versions of one board with a few component changes. They allow users to exercise features of the four devices and to build PLLs which meet individual performance requirements. The control program works with any board and can be used with other Motorola PLL devices (MC145192, MC145202, MC145220*). (NOTE: The MC145220 is not available with Rev. 3.0 software.) It will select frequency defaults that apply to each. All board functions are controlled through the printer port of an IBM PC. Up to three different EVKs may be controlled at the same time from one printer port. The functional block diagram is given in Figure 1.

This manual is divided into two sections. Section 1 describes the hardware and Section 2 covers the software control program.

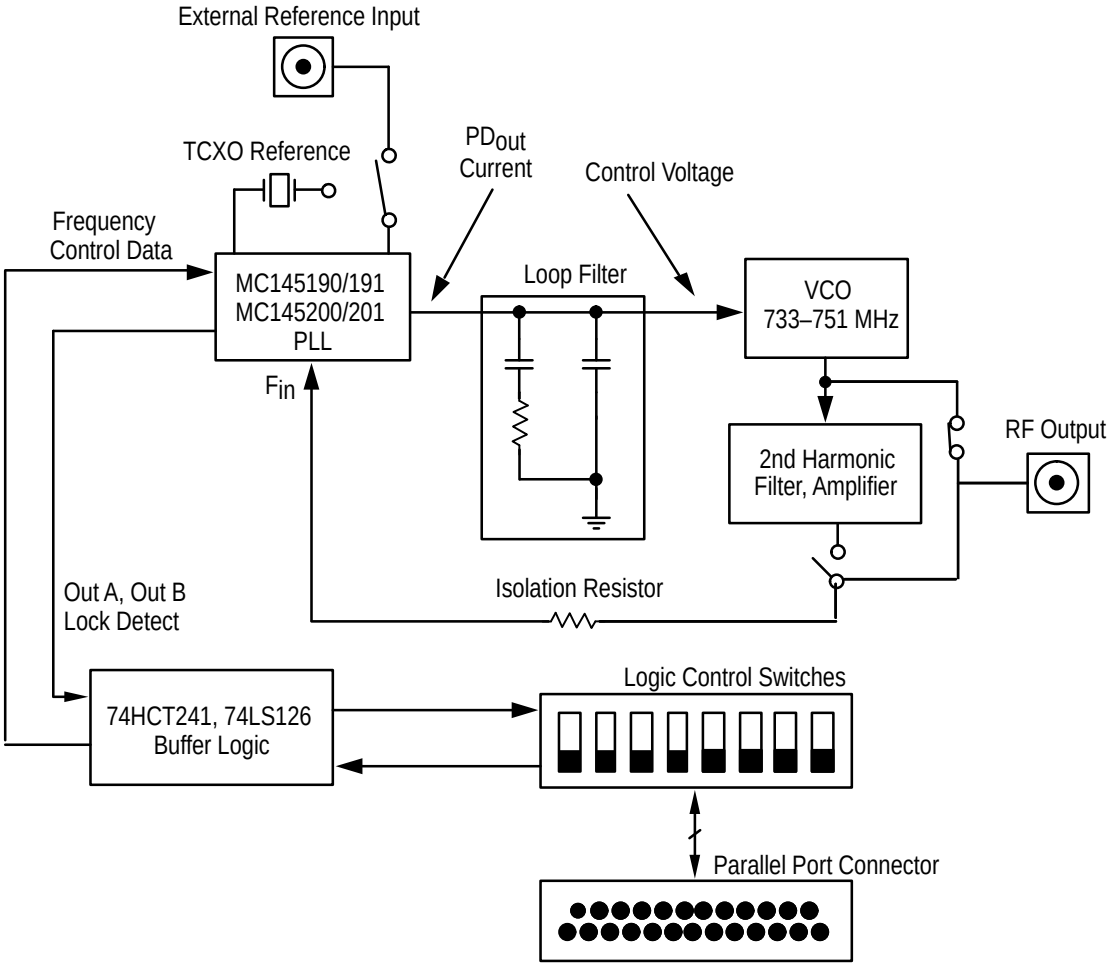

Figure 1. Evaluation Kit Block Diagram

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SECTION 1 – HARDWARE

FEATURES

1. The EVK is a complete working synthesizer, including VCO.
2. Control program is written in Turbo Pascal.
3. Board is controlled by an IBM PC–compatible computer through the printer port.
4. Up to three boards can be operated independently through one printer port.
5. A prototype area and mounting holes are provided for VCOs, mixers, and amplifiers.
6. External reference input can be used.
7. Five element loop filter is included.
8. Frequency range of operation, step size and reference frequency can be changed in the control program.
9. Lock Detect, Out A, and Out B on any single board are accessible through the printer port.

CONTENTS OF EVALUATION KIT

1. Assembled evaluation board.
2. Nine–foot flat cable with four DB–25 male connectors.
3. MC145190/191/200/201 EVK manual.
4. 3.5″ PC–compatible disk containing compiled program.
5. PLL device data sheets.

GETTING STARTED

To perform basic functions, do the following:

1. Plug in 12 volts at J6, observing the polarity marked on the board.
2. Short circuit section 1 of the DIP switch (S1) and open circuit all other sections.
3. Connect the supplied flat cable between the computer printer port and the DB–25 connector on the board (J5).
4. Type PLLDEMO at the DOS prompt. Then press enter.
5. Type the number that corresponds with the type of board given in the on–screen menu. Then press Q.

You should now see the main menu displayed. There should be a signal present at J8 on the current output frequency given in the main menu. If the signal is not on the correct frequency, check to see if your printer card address is $278 (hexadecimal 278). If not, then select the P menu item and enter the correct address. After returning to the main menu, select the I menu item to send data to the board. You should now be on frequency.

MODIFICATIONS

The user may modify the hardware, such as utilizing a different VCO, by using the prototyping area of the board. After such modifications are made, the default values in the software may need to be changed. This is facilitated from screen #2 ‘Select from the available options’ screen.

Note that the on–board voltage regulators allow for maximum control voltage to the VCO of approximately 7.8 V for the MC145190EVK and MC145200EVK. The maximum VCO control voltage is approximately 4.3 V for the MC145191EVK and MC145201EVK. The minimum voltage for all four devices is 0.5 V.

TYPICAL PERFORMANCE

Common to all four kits, unless noted.

Supply Voltage (J6)	11.5 – 12.5 V
Supply Current (J6) (Note 1)	120 mA
Available Current (Note 2)	60 mA
Frequency Range (’190)	741 – 751 MHz
Frequency Range (’191)	733 – 743 MHz
Frequency Range (’200)	1482 – 1502 MHz
Frequency Range (’201)	1466 – 1486 MHz
Reference Frequency	14.4 MHz
Temperature Stability (– 30°C to + 85°C)	< ± 2 ppm
TCXO Aging	< ± 1 ppm / year
Step Size (’190, ’191)	100 kHz
Step Size (’200, ’201)	200 kHz
Power Output	5 – 8 dBm
2nd Harmonic Level (’190, ’191)	< – 18 dB
Fundamental Level (’200, ’201)	< – 28 dB
3rd Harmonic Level	< – 18 dB
Frequency Accuracy (’190, ’191)	± 1.5 kHz
Frequency Accuracy (’200, ’201)	± 3.0 kHz
Reference Sidebands	– 70 dB
Phase Noise (100 Hz, ’190, ’191)	– 69 dBc/Hz
Phase Noise (100 Hz, ’200, ’201)	– 64 dBc/Hz
Phase Noise (10 kHz, ’190, ’191) (Note 3)	– 99 dBc/Hz
Phase Noise (10 kHz, ’200, ’201) (Note 3)	– 92 dBc/Hz
Switching Time (Note 4)	2.6 ms

NOTES:

1. Supply current is current the board requires without user modifications.
2. Available current is the sum of currents available to the user (in the prototype area) from the 5 V and 8.5 V supply. The 12 V supply is not regulated. Current at 12 V is limited by the external power supply. If the on–board VCO and amplifier are disconnected from the power bus, more current can be drawn in the prototype area. The current flowing into U3 (the 8.5 V regulator) should not exceed 180 mA. This will limit temperature rise in U3.
3. 10 kHz phase noise is limited by the PLL device noise. For low noise designs, the loop bandwidth is made more narrow and the VCO is relied upon to provide the 10 kHz phase noise. This can be seen on the EVKs since the VCO has much lower noise.
4. 10 MHz step, within ± 1 kHz of final frequency (’190, ’191).
   20 MHz step, within ± 2 kHz of final frequency (’200, ’201).

SUPPORT MATERIAL

To provide further information, the following documents are included:

1. Schematic diagram of ’190/191/200/201EVK.
2. Separate Bill of Materials for each board.
3. Parts layout diagram.
4. Mechanical drawing of board.
5. MC145190/191 and MC145200/201 data sheets.
6. Printer port diagram.
7. Typical signal plots for each type of EVK.

PRODUCTION TEST

After assembly is complete, the following alignment and test is performed on ’190 and ’191EVK (’200 and ’201EVK):

1. The control program is started in single board ’190EVK (’200EVK) mode.
2. L menu item is selected.
3. Power is applied to the board. DIP switch section 1 is closed circuit with all others being open circuit.
4. After attaching computer cable, menu item I is selected.
5. Trim resistor VR1 is adjusted to obtain an output frequency at J8 of 740.999 – 741.001 MHz (1481.998 – 1482.002 MHz).
6. Voltage at the control voltage test point is measured. It must be 2.8 – 3.6 V.
7. When testing more than 1 board, steps 3 – 6 are repeated.

If in step 5 it isn’t possible to obtain a signal on frequency, menu item P should be selected and the correct printer port address entered. Menu item I would then be selected to reload the data.

BOARD OPERATION

A computer is connected to the DB–25 connector J5. Data is output from the printer port. The printer card is in slot 0 using the default address in the control program. Data is sent to the PLL device (U1) through the DIP switch (S1), and 74HCT241 buffer (U5). A ’190/191/200/201 PLL has three output lines which are routed through a 74LS126 line driver (U2) to the computer.

U5, the 74HCT241, provides isolation, logic translation and a turn–on delay for PLL input lines. Logic translation is needed from the TTL levels on the printer port to the CMOS levels on the ’190/191 inputs. Turn–on delay is used to ensure the power–on reset functions properly. The clock line to the PLL must be held low during power up.

A 12 V power supply should be used to power the board at J6 (Augat 2SV–02 connector). The 2SV–02 will accept 18–24 AWG bare copper power leads. No tools are needed for connection. If power is properly connected, LED D2 will be lit.

Power passes from J6 to U3 (78M08 regulator) configured as an 8.5 V regulator. D1 increases output voltage of the regulator by 0.6 V. In the ’190 and ’200 boards, 8.5 V is routed through J3 to the charge pump supply, VCO, and RF amplifier. The ’191 and ’201 boards use 8.5 V to power the VCO and RF amplifier. J3 is a cut–trace and jumper. If it is desired to power the 8.5 V circuits directly, the trace under J3 can be cut, J3’s shorting plug is removed, and 8.5 V is applied through J7 (2SV03 power connector).

Power for the 5 V logic is provided by U4 (78M05). U4 steps down the 8.5 V from U3. Output voltage from U4 passes through J4, the 5 V cut–trace and jumper. To supply separate power to logic, the trace under J4 is cut, J4 shorting plug is removed, and 5 V is applied to J7. U3 and U4 are cascaded to lower their individual voltage drops. This lowers the power dissipated in the regulators.

The PLL loop is composed of the PLL device (U1), 733 – 751 MHz VCO (M1), passive loop filter (R11, R12, C4, C5, C6) and second harmonic filter amplifier (U6). A passive loop filter was used to keep the design simple, reduce noise, and reduce the quantity of traces susceptible to stray pickup. About 56 dB rejection of fundamental and 23 dB gain is provided by the harmonic filter amplifier. This allows the ’200 or ’201 to lock at 1466 – 1502 MHz. The harmonic filter amplifier is bypassed on the ’190 and ’191.

A single VCO model is used for all boards. It is an internal Motorola part which is not sold for other applications. The ’190 and ’191 have different frequency ranges. This is due to the lower charge pump supply voltage of the ’191. A common 10 MHz tune range allows the same loop filter components to be used. For the same reason, the ’200 and ’201 tune range is 20 MHz with double the step size of the ’190 or ’191. RF is fed to the PLL chip F_{in} input through a voltage divider. These two resistors terminate the PLL chip RF input with 50 ohms and provide isolation.

All boards use a phase detector current of 2 mA. J1 and J2 are removable jumpers and cut traces. They are used as connection points for a current measurement of V_{PD} or V_{CC}. J11 and J12 are wire jumpers that select 5 V or 8.5 V for V_{PD}. A potentiometer VR1 is used to set M2 (14.4 MHz TCXO) on frequency.

COMPONENTS UNIQUE TO EACH EVK

Components that are not the same on all EVKs are given in the following table:

	’190 EVK	**’191 EVK**	**’200 EVK**	**’201 EVK**
U1	MC145190	MC145191	MC145200	MC145201
R2	47 kΩ	22 kΩ	47 kΩ	22 kΩ
R8	0 Ω	0 Ω	not used	not used
C22	not used	not used	1.0 pF	1.0 pF
J11	connected	not used	connected	not used
J12	not used	connected	not used	connected

EXTERNAL REFERENCE INPUT

As shipped, all boards are configured for a 14.4 MHz TCXO (supplied). To use an external reference, disconnect J13 and connect J9. Use a reference signal at J10 which complies with data sheet requirements. Then modify the reference frequency in the program main menu to reflect the changes made ([F] menu item).

DATA TRANSFER FROM COMPUTER TO EVK

To control the serial input EVK with the parallel printer port, a conversion is done. Printer cards are designed to output 8 bits through eight lines. A bit mask is used to obtain the bit combination for the three required output lines (Data, Clock, Load). As bytes are sent to the printer card in sequence, it appears to be a serial transfer. The printer port was used because data transfer using the serial port would have been much slower. A standard IBM PC can support a parallel port data rate of 4.77 MHz.

IBM PCs and compatibles can accept up to three printer port cards. These ports are called LPT1, LPT2 and LPT3. Each printer card has jumpers or DIP switches on it to set a unique address. Two sets of addresses are in common use. One set applies to IBM PC XT, AT, and clones. The other is for the PS 2 line. To load data into the EVK, the correct address must be selected. The program default is $278, which is LPT1 in a clone. If $278 is not the address in use, it must be modified by entering the O menu item in the main menu. All allowed addresses given in hexadecimal are as follows:

Label	IBM PC and Clones	PS 2
LPT1	278	3BC
LPT2	378	378
LPT3	3BC	278

Up to three EVK boards can operate independently from one printer port. All lines on the printer port are connected to every EVK. Even with three boards operating, only three output lines (Clock, Data and Load) from the printer card are used. If two boards are controlled together, data for the second board is received from the Output A of the first. Output A is a configurable output on 190/191/200/201 devices, which in this case is used to shift data through chip 1 into chip 2. Output A and Data are connected using a printer port input line. This was done to avoid connecting extra wires. Fortunately not all port input lines are needed for computer input. Load and Clock are common to both boards.

A three–board cascade is handled similarly to a two–board cascade. Out A on the first board is fed to Data on the second. Out A on the second connects to Data on the third. Instructing the program on the quantity of boards connected together allows it to modify the number of bits sent.

All boards have a DIP switch S1 which gives each a unique address. The configuration menu is used to tell the program what type of board is connected at a board address. Switch positions for all possible addresses are given in Figure 2.

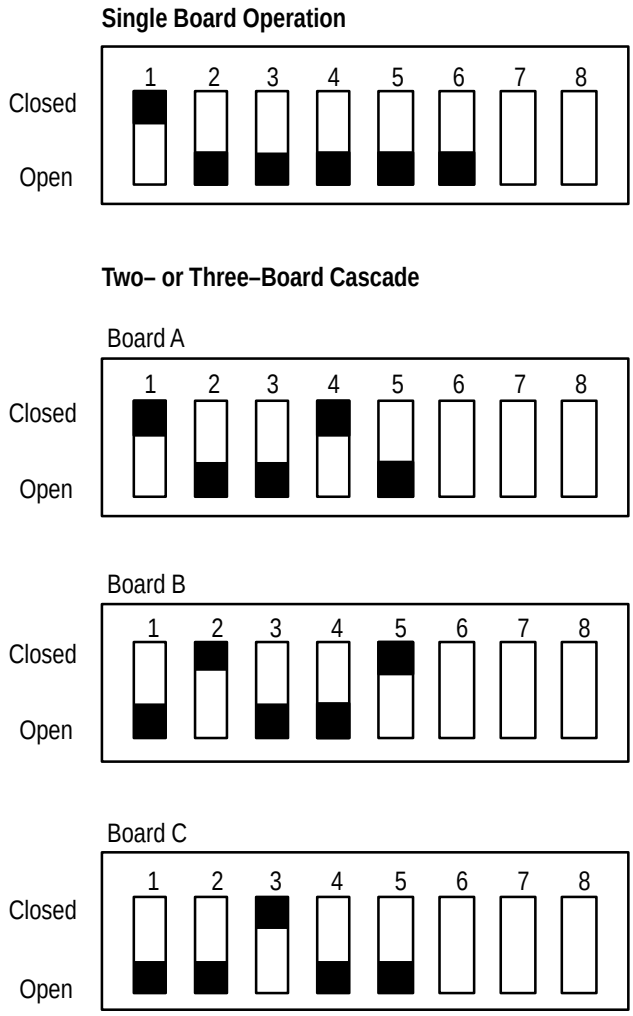

Figure 2. Switch Positions

In Figure 2, DIP switch sections 6, 7, and 8 allow the computer to read Out A, Out B or Lock Detect from the PLL device. Each of the inputs can only be read on one board at a time. But each item could be read on a different board. In a three–board cascade, Out A could be read from the first board, Out B from the second, and Lock Detect from the third. There is no way to determine in software the board address of a particular input. The control program doesn't make use of these inputs. Pin assignment on the printer port connector is:

Label	Pin Number
Out A	12
Out B	13
Lock Detect	15

PRINTER PORT CONFIGURATION

Printer port outputs on an IBM PC or clone use TTL–LS logic levels. Inputs are one TTL–LS load. Signal lines can be used for any purpose. The standard names, direction of data flow, true and inverted data are shown in Figure 3.

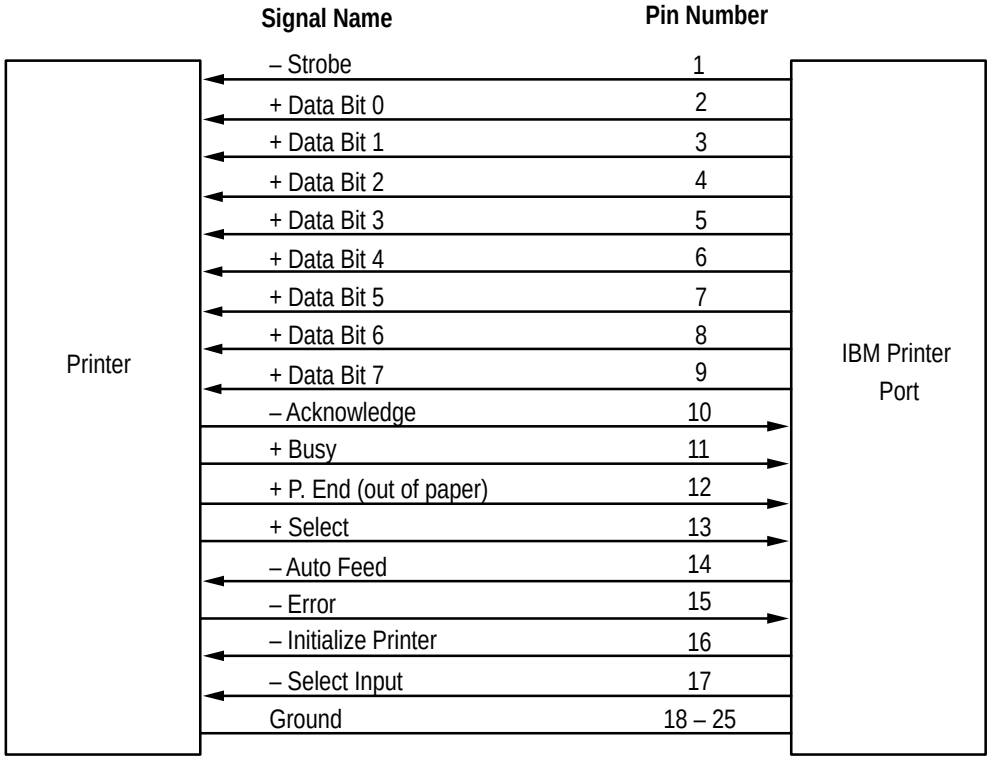

Figure 3. Printer Port Data Lines

Pin numbers for the port connector are shown in Figure 4.

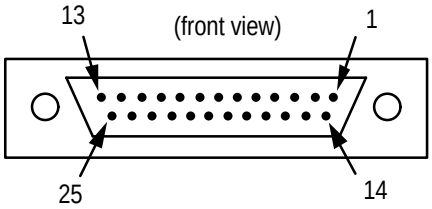

Figure 4. DB–25 Male Connector

SECTION 2 – SOFTWARE SUMMARY

The MC145xxx EVK control program (PLLDEMO) is used to program all PLL evaluation kits. It will simultaneoulsy control up to three different boards independently from one printer port. All features of the PLL device may be accessed. Default frequencies can be modified to allow us of different channel spacings and VCOs.

User input errors are detected and appropriate messages are displayed.

To show the format of PLLDEMO, one of the eighteen program screens is shown below:

Screen #2 'Select from the available options'

```
                    Welcome to MC145xxx EVK Demonstration Program, rev 3.0
                              Select from the available options

Available Boards – Current target board is: A, MC145190 EVK
 Brd [A]!: MC145190 EVK    Brd [–]!: N/A            Brd [–]!: N/A
–------------------------------------------------------------------------------
MC145xxx Frequency Commands – Current Output Frequency is 746 MHz
 [L]! Set to low freq      741 MHz      [W] Change default low freq.
 [M]! Set to med. freq     746 MHz      [Y] Change default med. freq.
 [H]! Set to high freq.    751 MHz      [Z] Change default high freq.
 [U]! Step frequency up by step size    [O] Set PLL output frequency
 [D]! Step frequency down by step size  [F] Set REFin freq. & channel spacing
MC145xxx Additional Commands
 [E]  Set function of output A          [N] Change C register and Prescale
 [R]  Set crystal/reference mode – Current mode is Ref. mode, REFout low


–------------------------------------------------------------------------------
Initialization/System Setup Commands:
 [P]  Set output port address – Current address is $278
 [G]  Change board definitions
 [I]  Initialize board(s), Write all registers

                [X]! Terminate demonstration program. [?]! View help screen.
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