4-Bit Transparent Latch/4-to-16 Line Decoder

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical "1" at the selected output, whereas the MC14515B (output active low option) presents a logical "0" at the selected output. The latches are R–S type flip–flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4–bit latch/4 to 16 line decoder are constructed with N–channel and P–channel enhancement mode devices in a single monolithic structure. The latches are R–S type flip–flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

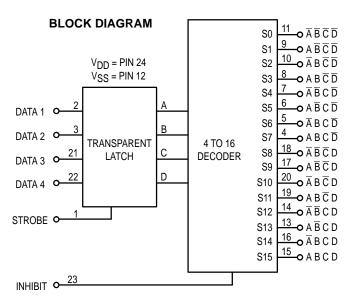
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to VSS)

| Symbol | Parameter | Value | Unit |
|--|--|------------------------------|------|
| V_{DD} | DC Supply Voltage | - 0.5 to + 18.0 | V |
| V _{in} , V _{out} | Input or Output Voltage (DC or Transient) | 0.5 to V _{DD} + 0.5 | V |
| I _{in} , I _{out} | Input or Output Current (DC or Transient), per Pin | ± 10 | mA |
| PD | Power Dissipation, per Package† | 500 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |
| T _L Lead Temperature (8–Second Soldering) | | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating:

Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



MC14514B MC14515B



L SUFFIX CERAMIC CASE 623



P SUFFIX PLASTIC CASE 709



DW SUFFIX SOIC CASE 751E

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

 $T_{\Delta} = -55^{\circ}$ to 125°C for all packages.

DECODE TRUTH TABLE (Strobe = 1)*

| | Data Inputs | | | | Selected Output |
|---------|-------------|---|---|---|--|
| Inhibit | D | С | В | Α | MC14514 = Logic "1" MC14515 = Logic "0" |
| 0 | 0 | 0 | 0 | 0 | S0 |
| 0 | 0 | 0 | 0 | 1 | S1 |
| 0 | 0 | 0 | 1 | 0 | S2 |
| 0 | 0 | 0 | 1 | 1 | S3 |
| 0 | 0 | 1 | 0 | 0 | S4 |
| 0 | 0 | 1 | 0 | 1 | S 5 |
| 0 | 0 | 1 | 1 | 0 | S6 |
| 0 | 0 | 1 | 1 | 1 | S7 |
| 0 | 1 | 0 | 0 | 0 | S8 |
| 0 | 1 | 0 | 0 | 1 | S9 |
| 0 | 1 | 0 | 1 | 0 | S10 |
| 0 | 1 | 0 | 1 | 1 | S11 |
| 0 | 1 | 1 | 0 | 0 | S12 |
| 0 | 1 | 1 | 0 | 1 | S13 |
| 0 | 1 | 1 | 1 | 0 | S14 |
| 0 | 1 | 1 | 1 | 1 | S15 |
| 1 | Х | Х | Х | Х | All Outputs = 0, MC14514 All Outputs = 1, MC14515 |

X = Don't Care

*Strobe = 0, Data is latched

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | | | V _{DD} | - 5 | 5°C | | 25°C | | 125 | i∘C | |
|---|-----------|-----------------|------------------------|------------------------------------|----------------------|----------------------------------|---|----------------------|------------------------------------|----------------------|------|
| | | Symbol | Vdc | Min | Max | Min | Тур # | Max | Min | Max | Unit |
| Output Voltage V _{in} = V _{DD} or 0 | "0" Level | VOL | 5.0 10 15 | _ _ _ | 0.05 0.05 0.05 | _ _ _ | 0 0 0 | 0.05 0.05 0.05 | _ _ _ | 0.05 0.05 0.05 | Vdc |
| $V_{in} = 0$ or V_{DD} | "1" Level | VOH | 5.0 10 15 | 4.95 9.95 14.95 | _ _ _ | 4.95 9.95 14.95 | 5.0 10 15 | _ _ _ | 4.95 9.95 14.95 | _ _ _ | Vdc |
| Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | "0" Level | V _{IL} | 5.0 10 15 | _ _ _ | 1.5 3.0 4.0 | _ _ _ | 2.25 4.50 6.75 | 1.5 3.0 4.0 | _ _ _ | 1.5 3.0 4.0 | Vdc |
| $(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$ | "1" Level | VIH | 5.0 10 15 | 3.5 7.0 11 | _ _ _ | 3.5 7.0 11 | 2.75 5.50 8.25 | _ _ _ | 3.5 7.0 11 | _ _ _ | Vdc |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) | Source | ІОН | 5.0 5.0 10 15 | - 1.2 - 0.25 - 0.62 - 1.8 | - - - | - 1.0 - 0.2 - 0.5 - 1.5 | - 1.7 - 0.36 - 0.9 - 3.5 | _ _ _ _ | - 0.7 - 0.14 - 0.35 - 1.1 | _ _ _ _ | mAdc |
| $(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$ | Sink | lOL | 5.0 10 15 | 0.64 1.6 4.2 | _ _ _ | 0.51 1.3 3.4 | 0.88 2.25 8.8 | _ _ _ | 0.36 0.9 2.4 | _ _ _ | mAdc |
| Input Current | | l _{in} | 15 | _ | ± 0.1 | _ | ±0.00001 | ± 0.1 | _ | ± 1.0 | μAdc |
| Input Capacitance (V _{in} = 0) | | C _{in} | _ | _ | _ | _ | 5.0 | 7.5 | _ | _ | pF |
| Quiescent Current (Per Package) | | IDD | 5.0 10 15 | | 5.0 10 20 | _ | 0.005 0.010 0.015 | 5.0 10 20 | _ _ _ | 150 300 600 | μAdc |
| Total Supply Current**† (Dynamic plus Quiesce Per Package) (C _L = 50 pF on all outp buffers switching) | • | l _{TL} | 5.0 10 15 | | | $I_{T} = (2)$ | .35 μΑ/kHz) † .70 μΑ/kHz) † .05 μΑ/kHz) † | f + I _{DD} | | | μAdc |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: IT is in μ A (per package), CL in pF, V = (VDD - VSS) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, $precautions\ must\ be\ taken\ to\ avoid\ applications\ of\ any\ voltage\ higher\ than\ maximum\ rated\ voltages\ to\ this\ high-impedance$ circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must

be left open.

^{**} The formulas given are for the typical characteristics only at 25°C.

[†]To calculate total supply current at loads other than 50 pF:

| | | | | All Types | | |
|---|--|-----------------|------------------|-----------------------|--------------------|------|
| Characteristic | Symbol | V _{DD} | Min | Typ # | Max | Unit |
| Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$ | tтLH | 5.0 10 15 | _ _ _ | 180 90 65 | 360 180 130 | ns |
| Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | tтн∟ | 5.0 10 15 | _ _ _ | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time; Data, Strobe to S tpLH, tpHL = (1.7 ns/pF) C _L + 465 ns tpLH, tpHL = (0.86 ns/pF) C _L + 192 ns tpLH, tpHL = (0.5 ns/pF) C _L + 125 ns | t _{PLH} , t _{PHL} | 5.0 10 15 | _ _ _ | 550 225 150 | 1100 450 300 | ns |
| Inhibit Propagation Delay Times $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) \text{ C}_{L} + 315 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) \text{ C}_{L} + 117 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) \text{ C}_{L} + 75 \text{ ns}$ | t _{PLH} , t _{PHL} | 5.0 10 15 | _ _ _ | 400 150 100 | 800 300 200 | ns |
| Setup Time Data to Strobe | ^t su | 5.0 10 15 | 250 100 75 | 125 50 38 | _ _ _ | ns |
| Hold Time Strobe to Data | ^t h | 5.0 10 15 | - 20 0 10 | - 100 - 40 - 30 | _ _ _ | ns |
| Strobe Pulse Width | tWH | 5.0 10 15 | 350 100 75 | 175 50 38 | _ _ _ | ns |

^{*}The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

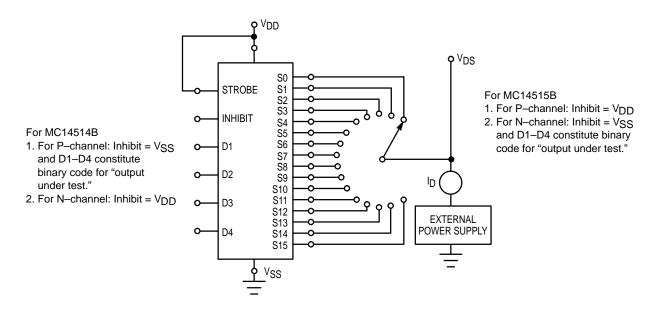


Figure 1. Drain Characteristics Test Circuit

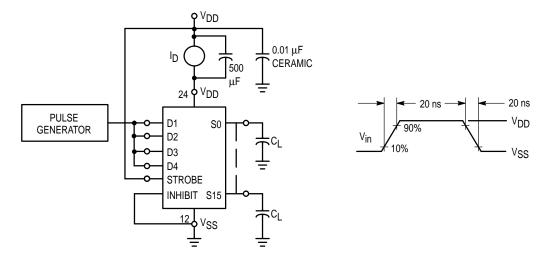


Figure 2. Dynamic Power Dissipation Test Circuit and Waveform

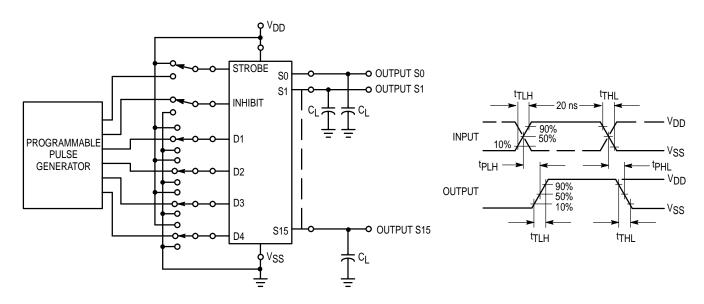
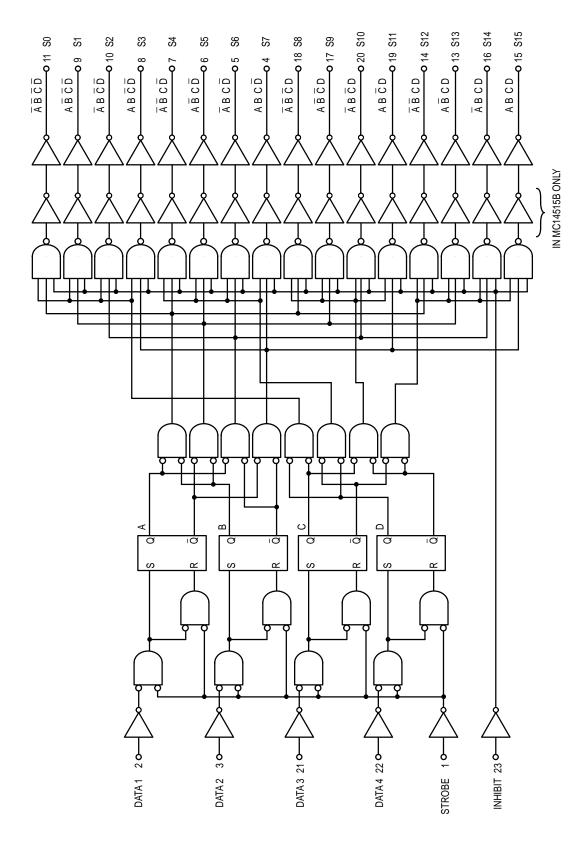


Figure 3. Switching Time Test Circuit and Waveforms

| PIN | ASSIGN | ME | NT |
|-------|--------|----|-----------------|
| ST [| 1 ● | 24 | v _{DD} |
| D1 [| 2 | 23 | INH |
| D2 [| 3 | 22 | D4 |
| S7 [| 4 | 21 | D3 |
| S6 [| 5 | 20 | S10 |
| S5 [| 6 | 19 | S11 |
| S4 [| 7 | 18 |] S8 |
| S3 [| 8 | 17 |] S9 |
| S1 [| 9 | 16 | S14 |
| S2 [| 10 | 15 | S15 |
| S0 [| 11 | 14 | S12 |
| Vss [| 12 | 13 | S13 |



COMPLEX DATA ROUTING

Two MC14512 eight—channel data selectors are used here with the MC14514B four—bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3—state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re—routed or intermixed according to patterns determined by data select and distribution inputs.

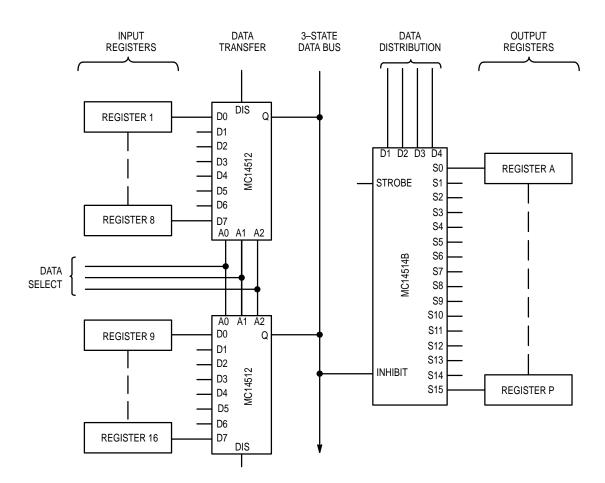
Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3–state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight

times faster then the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3–state bus is redistributed by the MC14514B four–bit latch/decoder. Using the four–bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

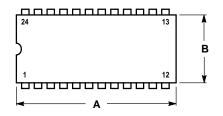
DATA ROUTING SYSTEM

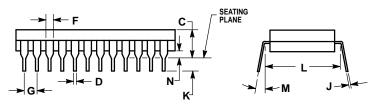


OUTLINE DIMENSIONS

L SUFFIX

CERAMIC DIP PACKAGE CASE 623-05 ISSUE M





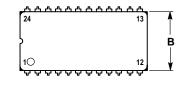
- NOTES:

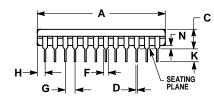
 1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

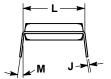
| | MILLIN | IETERS | INC | HES |
|-----|-----------|--------|-------|-------|
| DIM | MIN | MAX | MIN | MAX |
| Α | 31.24 | 32.77 | 1.230 | 1.290 |
| В | 12.70 | 15.49 | 0.500 | 0.610 |
| С | 4.06 | 5.59 | 0.160 | 0.220 |
| D | 0.41 | 0.51 | 0.016 | 0.020 |
| F | 1.27 | 1.52 | 0.050 | 0.060 |
| G | 2.54 | BSC | 0.100 | BSC |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| ٦ | 15.24 BSC | | 0.600 | BSC |
| М | 0 ° | 15° | 0 ° | 15° |
| N | 0.51 | 1.27 | 0.020 | 0.050 |

P SUFFIX

PLASTIC DIP PACKAGE CASE 709-02 **ISSUE C**





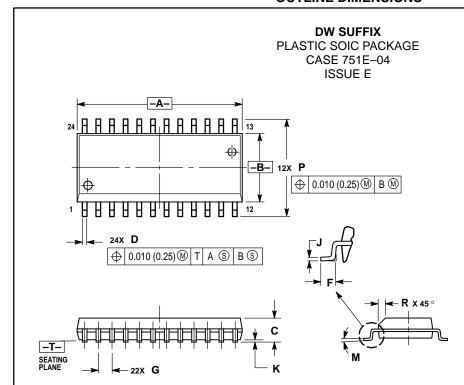


- OTES:

 1. POSITIONAL TOLERANCE OF LEADS (D),
 SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM
 MATERIAL CONDITION, IN RELATION TO
 SEATING PLANE AND EACH OTHER.
 2. DIMENSION L TO CENTER OF LEADS WHEN
 FORMED PARALLEL.
- 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| | MILLIN | IETERS | INC | HES | |
|-----|--------|--------|-----------|-------|--|
| DIM | MIN | MAX | MIN | MAX | |
| Α | 31.37 | 32.13 | 1.235 | 1.265 | |
| В | 13.72 | 14.22 | 0.540 | 0.560 | |
| С | 3.94 | 5.08 | 0.155 | 0.200 | |
| D | 0.36 | 0.56 | 0.014 | 0.022 | |
| F | 1.02 | 1.52 | 0.040 | 0.060 | |
| G | 2.54 | BSC | 0.100 BSC | | |
| H | 1.65 | 2.03 | 0.065 | 0.080 | |
| J | 0.20 | 0.38 | 0.008 | 0.015 | |
| K | 2.92 | 3.43 | 0.115 | 0.135 | |
| L | 15.24 | BSC | 0.600 | BSC | |
| M | 0 ° | 15° | 0 ° | 15° | |
| N | 0.51 | 1.02 | 0.020 | 0.040 | |

OUTLINE DIMENSIONS



NOTES

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION: ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN
 EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIN | IETERS | INC | HES |
|-----|--------|--------|-------|-------|
| DIM | MIN | MAX | MIN | MAX |
| Α | 15.25 | 15.54 | 0.601 | 0.612 |
| В | 7.40 | 7.60 | 0.292 | 0.299 |
| С | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.41 | 0.90 | 0.016 | 0.035 |
| G | 1.27 | BSC | 0.050 | BSC |
| J | 0.23 | 0.32 | 0.009 | 0.013 |
| K | 0.13 | 0.29 | 0.005 | 0.011 |
| М | 0° | 8° | 0° | 8° |
| Р | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

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JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



