MC141562

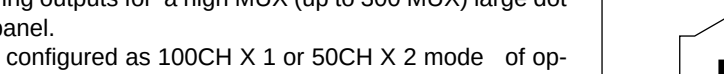
LCD Common (Row) Driver
CMOS

The MC141562 is a high volt, high MUX passive LCD common driver. It is a low power silicon-gate CMOS LCD driver chip which consists of 100-channel common driving outputs for a high MUX (up to 300 MUX) large dot matrix passive LCD panel.

This chip can be configured as 100CH X 1 or 50CH X 2 mode of operation. The 28 V high voltage output driving cells can be controlled by low voltage (3.0 volts) logic input.

The MC141562 will provide the best performance in combination with the MC141563 (segment driver).

- Operating Supply Voltage Range -
  Control Logic, Shift Register (VDD): 2.7V to 5.5V
  Common Drivers (VLCD): 10 V to 28 V
- Operating Temperature Range: -20 to 70˚C
- 100 LCD Common Driving Outputs.
- Driving Duty Cycle (MUX) : 1/100 to 1/300.
- Bi-directional Shift Register with 100CH X 1 or 50CH X 2 Mode of Operation.
- Interchangeable Carry-In / Carry-Out Terminals.
- Left / Right Shift Mode Selection.
- Cascadable.
- Maximum Shift Clock Frequency = 1.0 MHz
- Available in TAB (Tape Automated Bonding), 115 pins



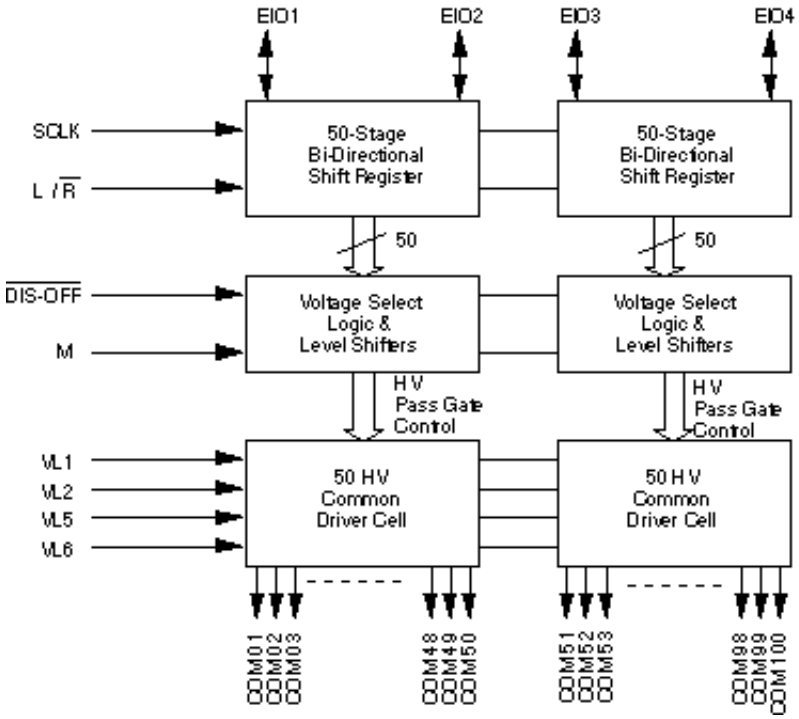
MC141562T

TAB

ORDERING INFORMATION

MC141562T	TAB

BLOCK DIAGRAM



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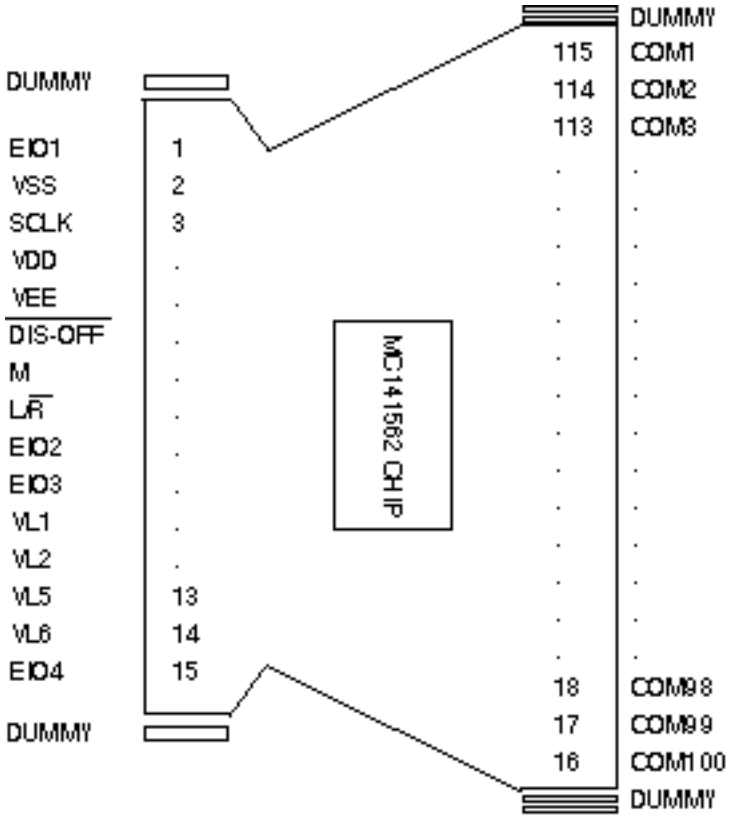


Figure 1. TAB Package Contact Assignment (Copper View)

MAXIMUM RATINGS*(Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +6.0	V
V_{EE}		-0.3 to -24.0	V
V_{LCD}	DC Supply Voltage (V_{DD} - V_{EE})	V_{DD} to +30	V
V_{Din} V_{Ain}	Input Voltage All Digital Input V_{LCD} Level Input	 V_{SS}-0.3 to V_{DD}+0.3 V_{EE}-0.3 to V_{DD}+0.3	 V V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature Range	-20 to 70	˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A = 25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Operating Voltage					V
V_{DD}	Supply Voltage (reference to V_{SS})		2.7	-	5.5	V
V_{LCD}	LCD Supply Voltage (V_{DD} - V_{EE})		10.0	-	28.0	
	Supply Current (V_{DD} Pin)	V_{DD}=5.5V, V_{EE}=-23V				
I_{DP}	Display Mode	SCLK = 200KHz, M=2KHz	-	40	100	µA
I_{SB}	Standby Mode		-	0.3	2	µA
	Supply Current (V_{DD} Pin)	V_{DD}=2.7V, V_{EE}=-23V				
I_{DP}	Display Mode	SCLK = 200KHz, M=2KHz	-	20	-	µA
I_{SB}	Standby Mode		-	0.3	-	µA
I_{EE}	Supply Current at V_{EE}	No Load	-	30	150	µA
	Common Output Voltage	Iload = 150µA				
V_{OL}	VL5,6=V_{EE}		-	-	V_{EE}+0.3	V
V_{OH}	VL1,2=V_{DD}		V_{DD}-0.3	-	-	V
	COM1-COM100					
V_{OH}	Output High Voltage	V_{DD}=5.0V, Iload=1mA	V_{DD}-1.0	-	-	V
V_{OL}	Output Low Voltage		-	-	V_{SS}+1.0	V
	EIO1, EIO2, EIO3, EIO4					
V_{IH}	Input High Voltage		0.7xV_{DD}	-	V_{DD}	V
V_{IL}	Input Low Voltage		V_{SS}	-	0.2xV_{DD}	V
	SCLK, L/$\overline{R}$, EIO1, EIO2, EIO3, EIO4, M, $\overline{DIS\text{-}OFF}$					
I_{in}	Input Current		-	0.5	1	µA
	SCLK, L/$\overline{R}$, EIO1, EIO2, EIO3, EIO4, M, $\overline{DIS\text{-}OFF}$					
C_{in}	Capacitance		-	5	10	pF
	SCLK, L/$\overline{R}$, EIO1, EIO2, EIO3, EIO4, M, $\overline{DIS\text{-}OFF}$					
I_{OHX}, I_{OLX}	Common Output Current	V_{OH}= V_{DD} - 0.3V, V_{OL}=V_{EE} +0.3V	150	-	-	µA
	COM1-COM100					
I_{OHC}, I_{OLC}	Carry Output Current	V_{OH}= V_{DD} - 1.0V, V_{OL}=V_{SS} +1.0V	1.0	-	-	mA
	EIO1, EIO2, EIO3, EIO4					
R_{ON}	Common Output Impedance	V_{DD} - V_{EE} =28V, I_{OHX}, I_{OLX}= 150µA	-	1	2	K Ohm
	Common Output Impedance Variance		-	10	30	%

AC ELECTRICAL CHARACTERISTICS -WRITE CYCLE (V_{DD} =5.0V, V_{SS} = 0V, V_{EE} = -23V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{TLH} t_{THL}	Digital Input Rise and Fall Time SCLK, M, EIO1,2,3,4, $\overline{\text{DIS-OFF}}$	- -	25 25	50 50	ns ns
$t_{SCØ}$	Shift Clock (SCLK) Cycle	1000	-	-	ns
t_{SCH}	Shift Clock (SCLK) Pulse Width HIGH	150	-	-	ns
t_{SCL}	Shift Clock (SCLK) Pulse Width LOW	150	-	-	ns
t_{SUE}	Enable Input (EIO) to Shift Clock (SCLK) Set up Time	100	-	-	ns
t_{he}	Enable Input (EIO) to Shift Clock (SCLK) Hold Time	100	-	-	ns
t_{PEO}	Shift Clock (SCLK) to Enable Output (EIO) Delay Time CL = 25pF	-	-	100	ns

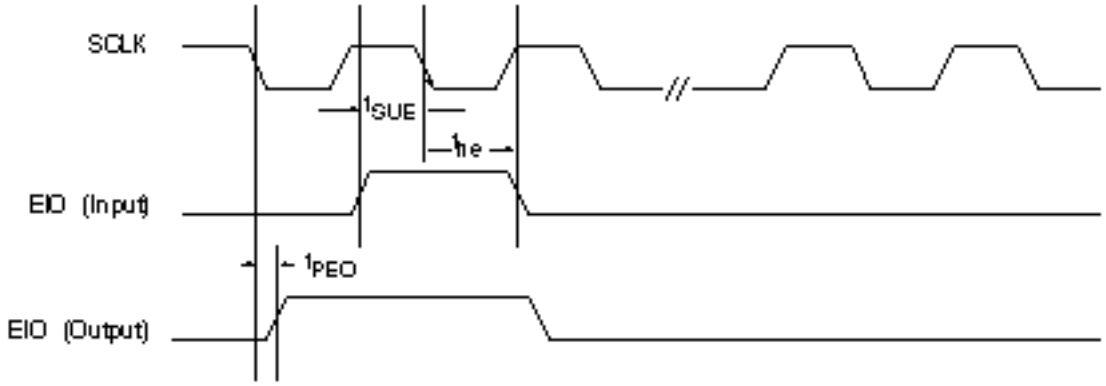


Figure 2. SCLK, EIO Input and Output Propagation Delay Timing Diagram

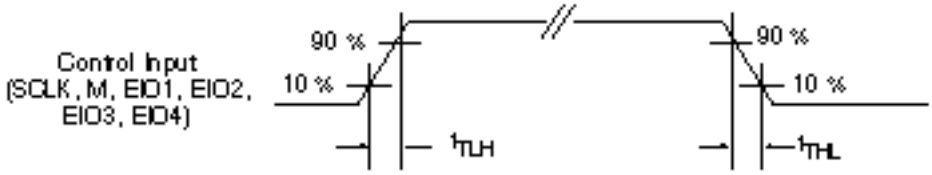


Figure 3. Control Input Rise and Fall Timing Diagram

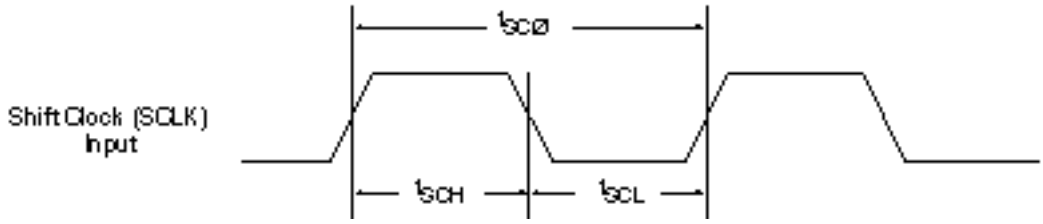


Figure 4. Shift Clock Pulse Width High and Pulse Width Low Timing Diagram

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

The main dc power is supplied to the part by these two connections. V_{DD} is the most-positive supply level and V_{SS} is ground.

VEE

This supply connection provides the negative power supply voltage for the common drivers.

VL1, VL2, VL5, VL6

These input pins are connected to the external voltage divider (See Figure 5).
Voltage supply level for the LCD :
VL1, VL6 : On-level of the LC
VL2, VL5 : Off-level of the LC

Carry Shift Clock (SCLK)

Carry input is strobed into the shift register by the falling edge of the SCLK.

Left / Right Shift Select (L / $\overline{R}$)

This input pin determines the direction of the shift register operation (See Table 1).
L / $\overline{R}$ = "0", the carry will shift right (COM. 1 to COM. 100).
L / $\overline{R}$ = "1", the carry will shift left (COM. 100 to COM. 1).

Carry-In / Carry-Out (EIO1, EIO2, EIO3, EIO4)

These four input / output pins perform the Carry-In and Carry-Out function depending on the shift register direction of operation. EIO1 and EIO2 are used as the I/O pins of the COM1 to COM50 block, while EIO3 and EIO4 are used as I/O pins for the COM51 to COM100 block. In right shift mode (L / $\overline{R}$ = "0"), the EIO1/EIO3 is the Carry-In input while the EIO2/EIO4 will be the Carry-Out output for cascading. In left shift mode (L / $\overline{R}$ = "1"), the pin functions and operation are reversed. In case of 100 CH application, EIO2 and EIO3 should be connected together.

Frame Signal Input (M)

This input signal is the Frame Sync. Signal which provides an frame alternating output format of the output (See Figure 6).

M	1	0	1	0
EIO (Input)	1	0	0	1
Output	VL1	VL2	VL5	VL6

Display-Off Enable ($\overline{\text{DIS-OFF}}$)

This input pin is active low. If set "LOW", all output pins (Common 1 to Common 100) are forced to VL1.

Common Output (Common 1 to Common 100)

These 100 output lines provide the high volt common signal to the LCD panel. They are all at VL1 while display is turned off.

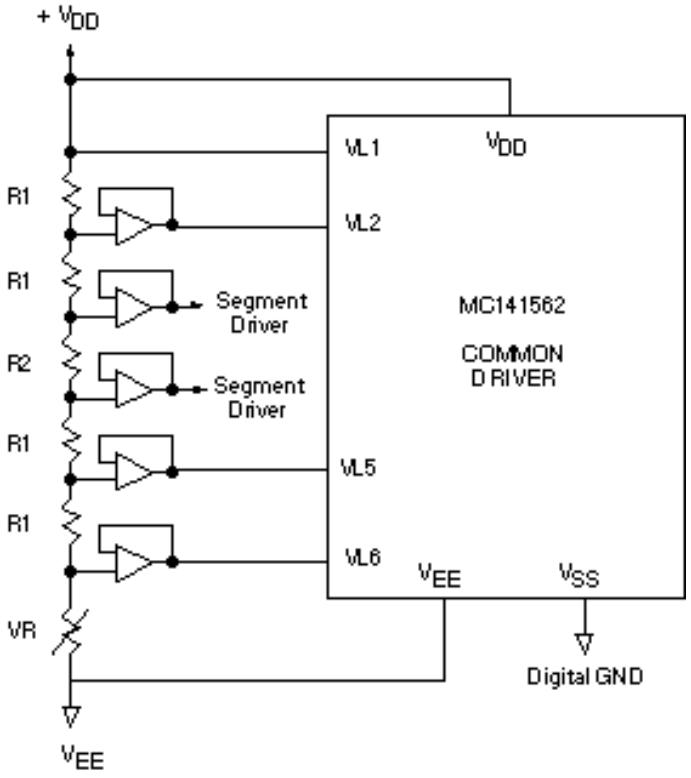


Figure 5. External Voltage Divider

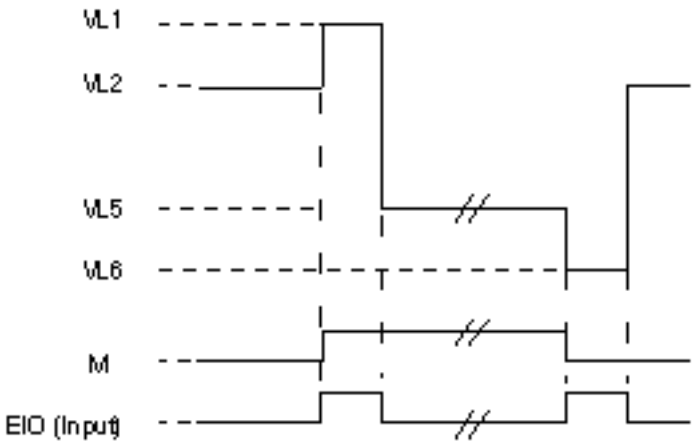


Figure 6. EIO Input, M Signal and Common Output Format

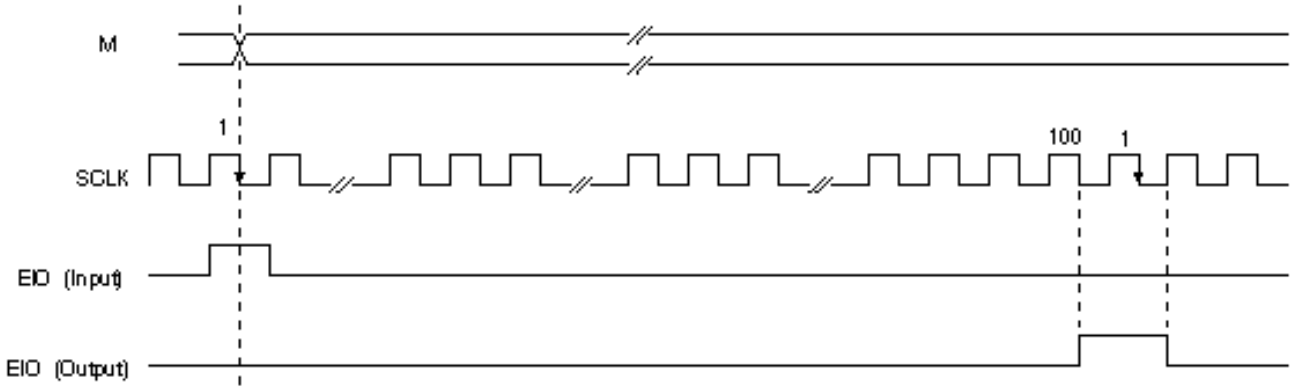


Figure 7. SCLK, M Signal and EIO Input and Output Timing Diagram

	EIO				
L / $\overline{R}$	1	2	3	4	Common Output
H	output			input	COM 100, 99 - - - - - - - - ▶ COM 2, 1
	output	input	output	input	COM 100, 99 - - - - - - - - ▶ COM 52, 51 COM 50, 49 - - - - - - - - ▶ COM 2, 1
L	input			output	COM 1, 2 - - - - - - - - ▶ COM 99, 100
	input	output	input	output	COM 1, 2 - - - - - - - - ▶ COM 49, 50 COM 51, 52 - - - - - - - - ▶ COM 99, 100

Table 1. Left / Right Shift Control, EIO and Common Output Relation

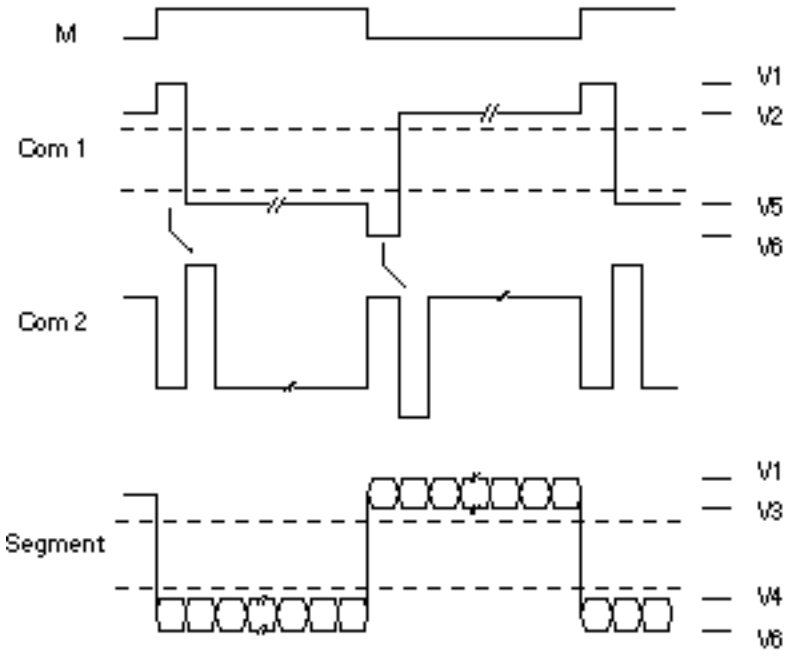
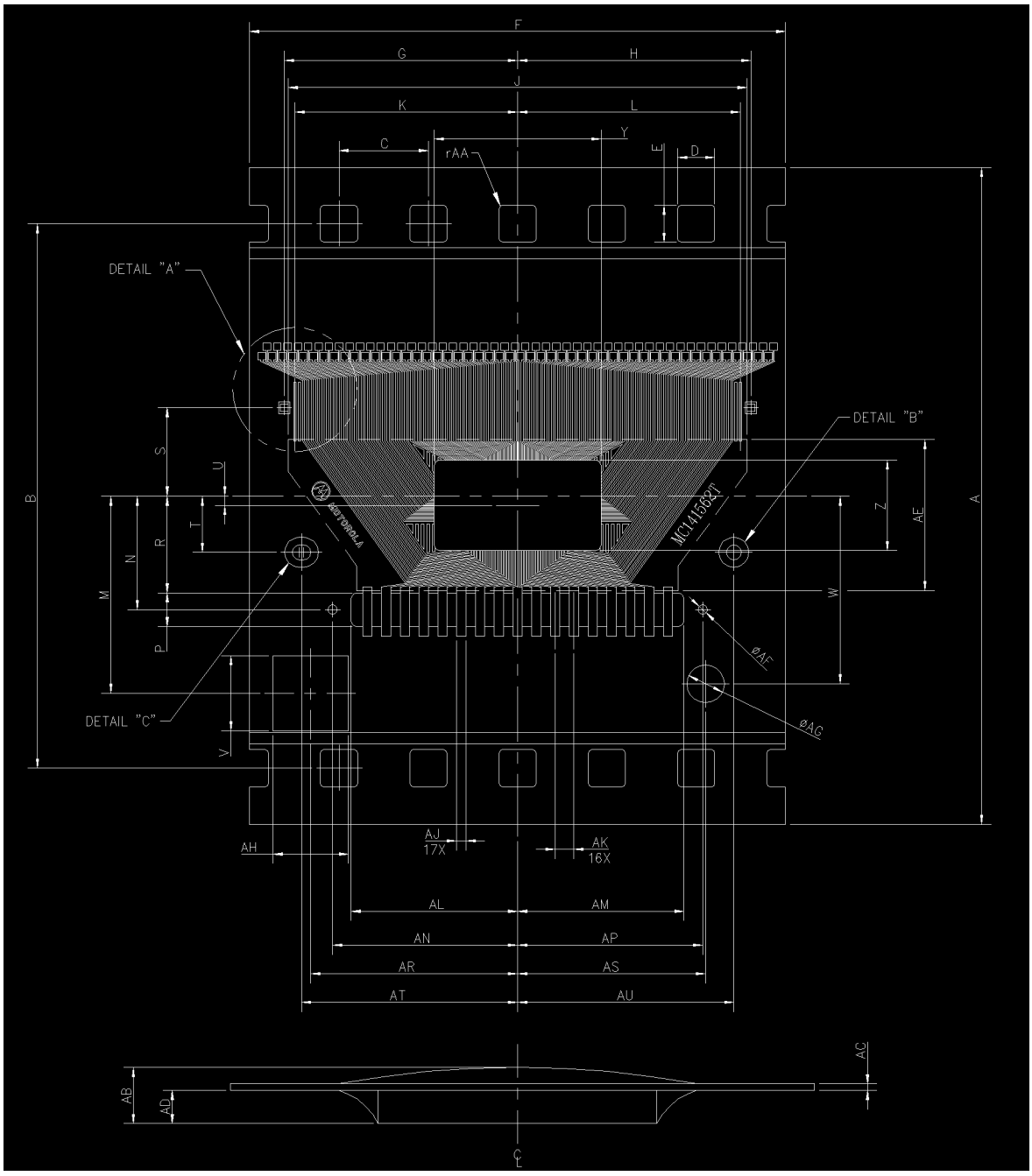


Figure 8. M Signal, Common and Segment Output Format

PACKAGE DIMENSIONS

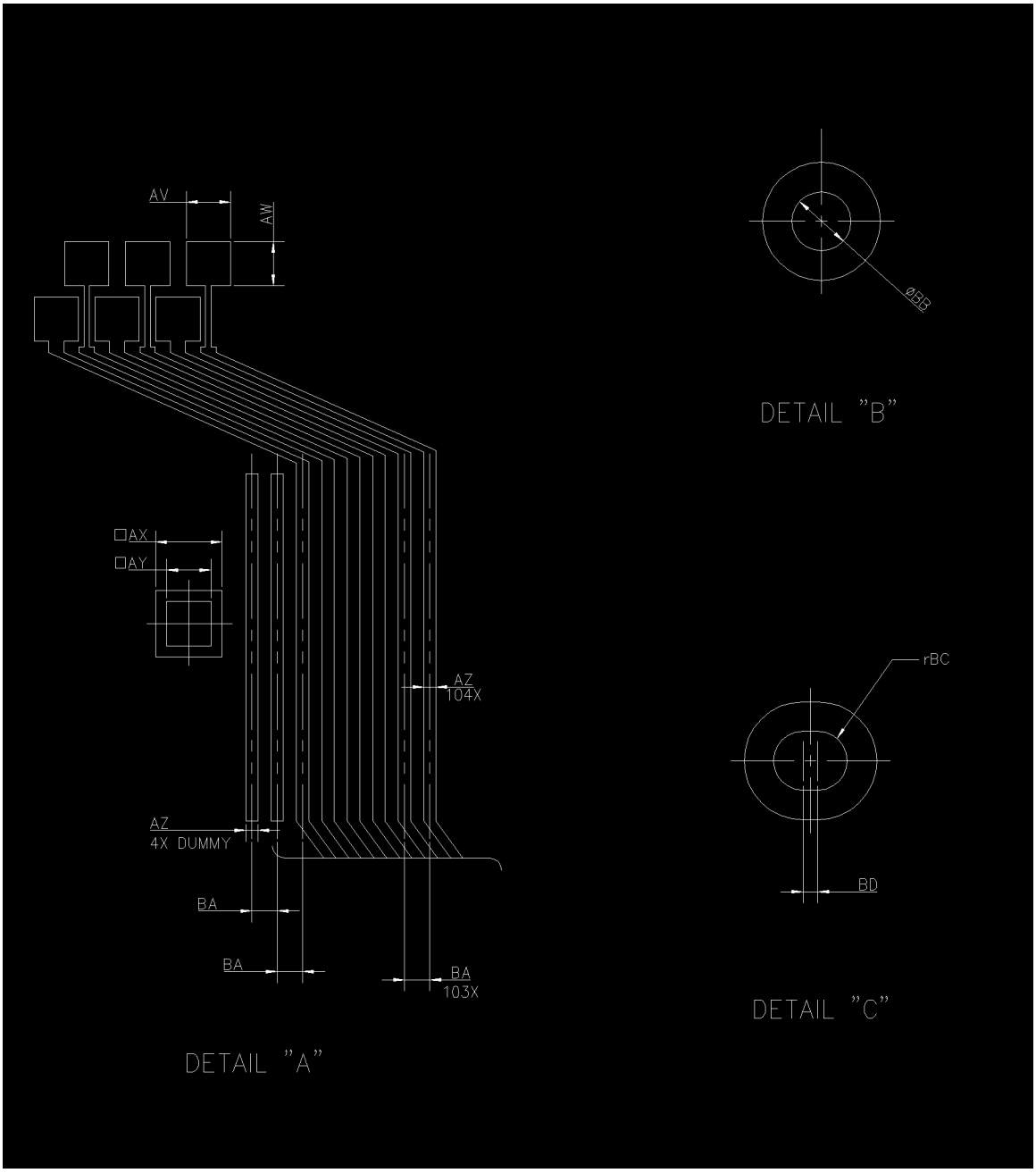
MC141562T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



MAGNIFIED VIEW

Reference : 98ASL00130A	Issue “0” released on 04/15/94

MC141562T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



Reference : 98ASL00130A	Issue “0” released on 04/15/94

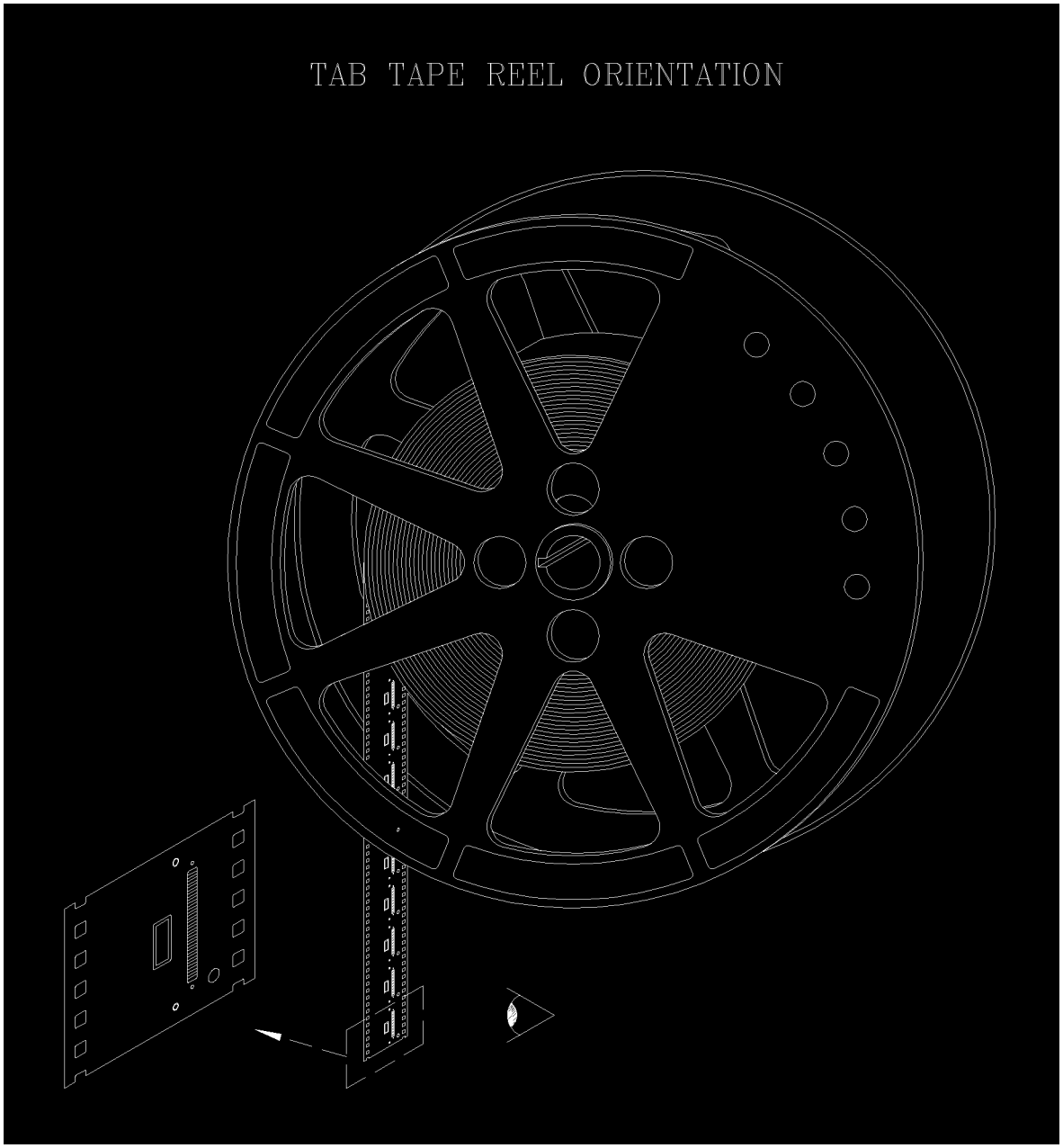
MC141562T TAB PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	**Min**	**Max**	**Min**	**Max**	**Dim**	**Min**	**Max**	**Min**	**Max**
A	34.775	35.175	1.3691	1.3848	AD	0.579	0.629	0.0228	0.0248
B	28.927	29.027	1.1389	1.1428	AE	7.765	8.365	0.3057	0.3293
C	4.720	4.780	0.1858	0.1882	AF	0.450	0.550	0.0177	0.0217
D	1.951	2.011	0.0768	0.0792	AG	1.950	2.050	0.0768	0.0807
E	1.951	2.011	0.0768	0.0792	AH	3.950	4.050	0.1555	0.1594
F	28.000	29.000	1.1024	1.1417	AJ	0.480	0.520	0.0189	0.0205
G	12.365	12.465	0.4868	0.4907	AK	0.990	1.010	0.0390	0.0398
H	12.365	12.465	0.4868	0.4907	AL	8.800	8.900	0.3465	0.3504
J	24.100	24.700	0.9488	0.9724	AM	8.800	8.900	0.3465	0.3504
K	11.821	11.869	0.4654	0.4673	AN	9.800	9.900	0.3858	0.3898
L	11.821	11.869	0.4654	0.4673	AP	9.800	9.900	0.3858	0.3898
M	10.000	11.000	0.3937	0.4331	AR	10.500	11.500	0.4134	0.4528
N	6.005	6.105	0.2364	0.2404	AS	9.500	10.500	0.3740	0.4134
P	1.750	1.850	0.0689	0.0728	AT	11.450	11.550	0.4508	0.4547
R	5.105	5.205	0.2010	0.2049	AU	11.450	11.550	0.4508	0.4547
S	4.643	4.743	0.1828	0.1867	AV	0.350	0.450	0.0138	0.0177
T	2.950	3.050	0.1161	0.1201	AW	0.350	0.450	0.0138	0.0177
U	0.000	1.000	0.0000	0.0394	AX	0.580	0.620	0.0228	0.0244
V	3.950	4.050	0.1555	0.1594	AY	0.380	0.420	0.0150	0.0165
W	9.500	10.500	0.3740	0.4134	AZ	0.090	0.130	0.0035	0.0051
Y	-	8.880	-	0.3496	BA	0.220	0.240	0.0087	0.0094
Z	-	4.820	-	0.1898	BB	0.750	0.850	0.0295	0.0335
AA	-	0.200	-	0.0079	BC	0.350	0.450	0.0138	0.0177
AB	0.686	0.838	0.0270	0.0330	BD	0.150	0.250	0.0059	0.0098
AC	0.068	0.083	0.0027	0.0032					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper Thickness: 1oz.
4. Tin plating thickness: 0.4µm
5. 6 sprocket hole device

Reference : 98ASL00130A	Issue “0” released on 04/15/94

MC141562T



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