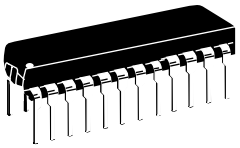
MC141546P2

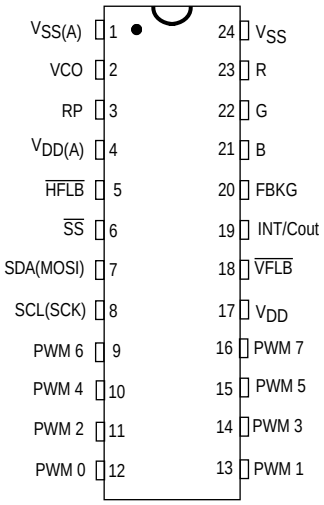
Advanced Monitor On-Screen Display II - 24
CMOS



P SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION
MC141546P2 Plastic Dip

PIN ASSIGNMENT



This is a high performance HCMOS device designed to interface with a microcontroller unit to allow colored symbols or characters to be displayed on a color monitor. Its on-chip PLL allows both multisystem operation and self generation of system timing. It also minimizes the MCU's burden through its built-in display and control bytes RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. There are two different resolutions that users can choose. By changing the number of dots per horizontal line to 384 (CGA) or 768 (VGA), smaller characters with higher resolution can be easily achieved.

Special functions such as character bordering or shadowing, multi-level windows, intensity control for windows, double height and double width, and programmable vertical length of character are also incorporated. Furthermore, neither massive information update nor extremely high data transmission rate are expected for normal on- screen display operation and serial protocols are implemented in lieu of any parallel formats to achieve the minimum pin count.

There are 8 PWM DAC channels for external digital to analog control. Each PWM DAC channel is composed of an 8 bit register which contains a 5 bit PWM in MSB portion and a 3 bit binary rate multiplier (BRM) in LSB portion.

Moreover, the font matrix is improved from 10 by 16 to high resolution font matrix, 12 by 18, in this version. In order to maintain the constant menu height in the different display modes, one special register, controlling the row to row spacing, is implemented to avoid the nonuniform extension of BRM algorithm in character height adjustment.

- 8 Channels 8-bit Synchronous PWM DAC with Push-Pull Output
- Two Resolutions: 384 (CGA) or 768 (VGA) Dots per Line
- 12 x 18 Dot Matrix Character
- Maximum Horizontal Frequency is 120 KHz (92.2MHz Dot Clock at 768 mode)
- Four Fully Programmable Background Windows with Intensity Control
- Row to Row Spacing Register to Manipulate the Constant Menu Height
- Programmable Height of Character to Meet Multi-Sync Requirement
- Smooth Menu Movement by Real Time Programming of H/V Delay Registers
- Fully Programmable Character Array of 15 Rows by 30 Columns
- Internal PLL Generates a Wide-Ranged System Clock
- Programmable Vertical and Horizontal Positioning for Display Center
- 128 Characters and Graphic Symbols ROM (Mask ROM is Optional)
- Character by Character Color Selection
- A Maximum of Four Selectable Colors per Row
- Double Character Height and Double Character Width
- Character Bordering or Shadowing
- M_BUS (IIC) Interface with Address $7A (SPI Bus is Mask Option)

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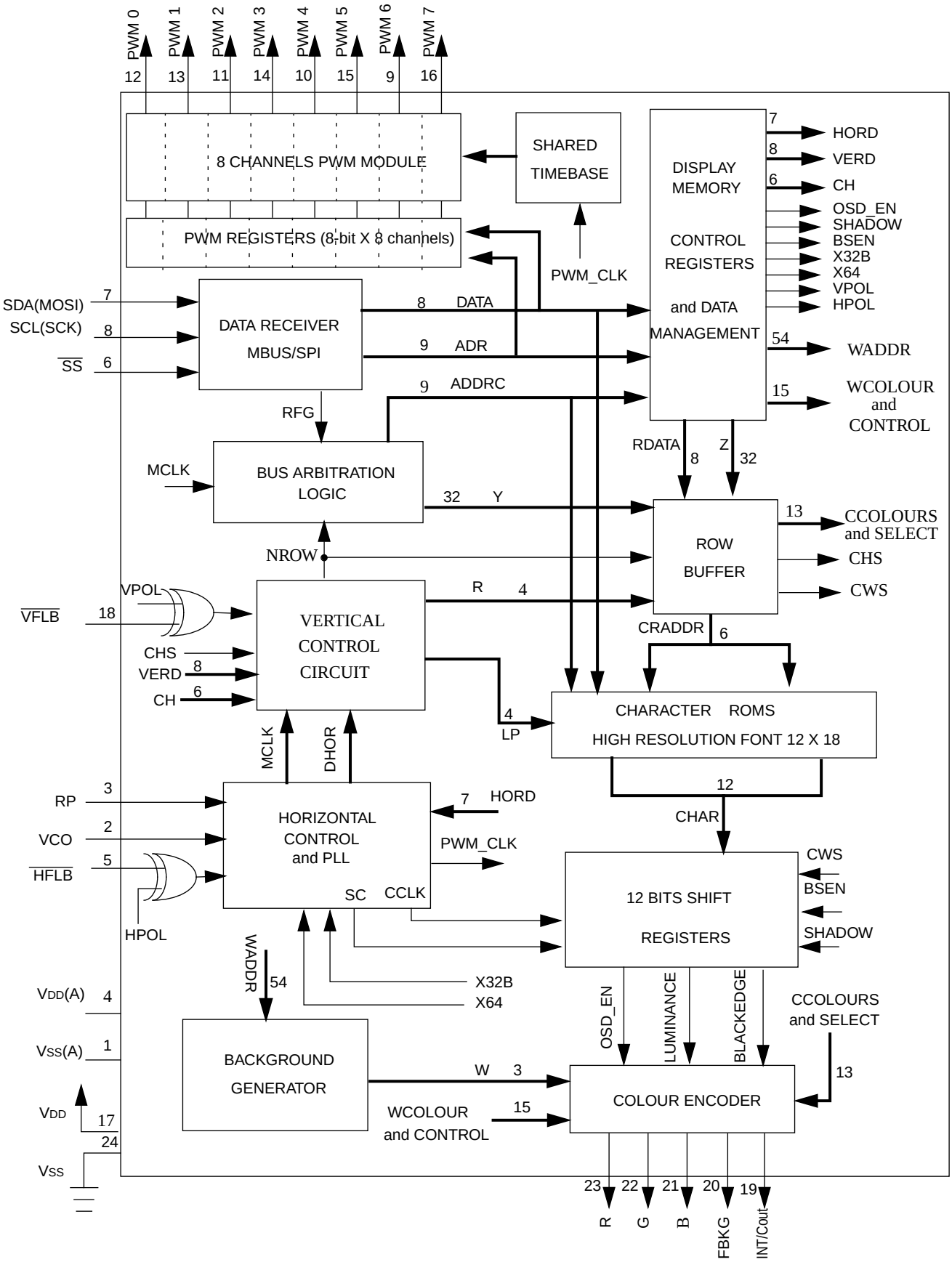
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}/V_{DD(A)}$ = 5.0 V, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25C, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and INT/Cout) C_{load} = 30 pF				
t_r	Rise Time	—	—	6	ns
t_f	Fall Time	—	—	6	ns
	Output Signal (PWM0 - PWM7) C_{load} = 30 pF				
t_r	Rise Time	—	—	20	ns
t_f	Fall Time	—	—	20	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	15K	—	120K	Hz

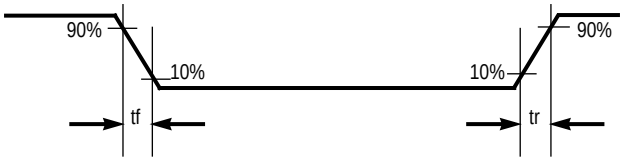


Figure 1. Switching Characteristics

DC CHARACTERISTICS $V_{DD}/V_{DD(A)}$ = 5.0 V ± 10%, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in SPI Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{II}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{II}	Input Current (Not Including RP, VCO, R, G, B, FBKG and INT)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output)	—	—	+ 20	mA
LVI	Low Voltage Inhibit for PWM DAC Output	2.7	3.2	3.6	V

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)

Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configured as a uni-directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

PWM 6 (Pin 9)
Channel 6 of the PWM.

PWM 4 (Pin 10)
Channel 4 of the PWM.

PWM 2 (Pin 11)
Channel 2 of the PWM.

PWM 0 (Pin 12)
Channel 0 of the PWM.

PWM 1 (Pin 13)
Channel 1 of the PWM.

PWM 3 (Pin 14)
Channel 3 of the PWM.

PWM 5 (Pin 15)
Channel 5 of the PWM.

PWM 7 (Pin 16)
Channel 7 of the PWM.

V_{DD} (Pin 17)

This is the power pin for the digital logic of the chip.

$\overline{VFLB}$ (Pin 18)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

INT/ Cout (Pin 19)

This is a multiplexed pin. When the Cout bit is cleared after power on or by the MCU, this pin is INT and this output pin is used to indicate the color intensity. If the associated window intensity control bits are set, this pin will output a logic high while displaying the specified windows. Otherwise, it will keep in low state. Only the windows have the color intensity selection and all displayed characters or symbols are all high intensity. It means that INT pin must be driven high while displaying the characters or symbols.

Please refer to the timing figure for detail timing chart. Thus, 16-color selection is achievable by combining this intensity pin with R/G/B outputs for windows' color control. On the other hand, this color intensity information could be reflected on the R/G/B pins by asserting tri-state instead of logic high if 3_S bit is set to 1. Refer to the "REGISTERS" for more information.

If the Cout bit is set to 1 via M_BUS or SPI, this pin is changed to a mode-dependent clock output with 50/50 duty cycle and synchronous with the input horizontal synchronization signal at Pin 5. The frequency is dependent on the mode in which the AMOSD II is currently running. The exact frequencies in the different resolution modes are described below.

Resolution	Frequency	Duty Cycle
384 dots/line	32 x H_f	50/50
768 dots/line	64 x H_f	50/50

NOTE: H_f is the frequency of the input H sync. on Pin 5.

Typically, this clock is fed into an external pulse width modulation module as its clock source. Because of the synchronization between Cout clock and H sync, a better performance on the external PWM controlled functions can be achieved.

FBKG (Pin 20)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 21, 22, 23)

AMOSD II color outputs in TTL level to the host monitor. These three outputs are in high impedance if 3_S bit is set and the color intensity is low. Otherwise, they are active high push-pull outputs. See "REGISTERS" for more information. These pins are in high impedance state after power on.

V_{SS} (Pin 24)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141546P2 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the AMOSD II is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the AMOSD II functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 $\overline{HFLB}$), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

BUS Operation

The operating clock for M_Bus or SPI bus derives from system dot clock. Internal PLL is using to generate the dot clock base on the HFLB input frequency where the dot clock is equal to 384/768xHFLB in 384/768 modes respectively. In order to have stable operation of M_Bus or SPI bus in the OSD and meet below specifications, HFLB(15k-120k) must be presented and the PLL locks to HFLB properly. Refer to Application Diagram for PLL bias circuit.

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100 kbps.The default chip address is $7A. Please refer to the IIC-Bus specification for detail timing requirement.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in

one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the AMOSD II circuitry of MC141546P2, so that the received information can then be displayed.

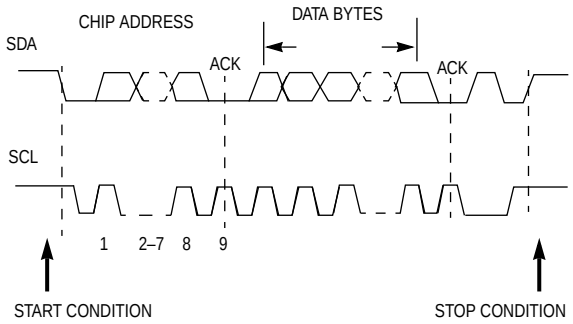


Figure 2. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{SS}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{SS}$ pin low by the master device to enable MC141546P2 to accept data. The $\overline{SS}$ input line must be a logic low prior to occurrence of SCK and remain low until and after the last (eighth) SCK cycle. After all data has been sent, the $\overline{SS}$ pin is then pulled high by master to terminate the transmission. Data bit is sent from master to OSD's internal latch during rising edge of SCK and then transmit to internal register during falling edge. Therefore, last falling edge of CLK is needed for proper transmission of last byte data. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

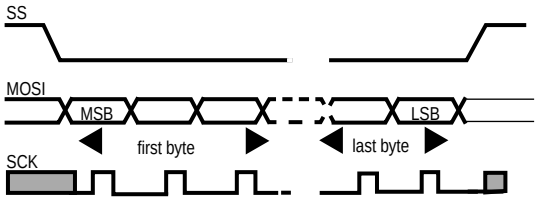


Figure 3. SPI Protocol

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the master. There are three transmission formats from (a) to (c) as stated below. The data train in each sequence consists of row address (R), column address (C), and display information (I), as shown in Figure 4. In format (a), display information data must be preceded with the corresponding row address and column address. This format is particularly suitable for updating small amounts of data between different rows. However, if the current information byte has the same row address as the one before, format (b) is recommended. For a full screen pattern change which requires a massive information update, or during power up situation, most of the row and column addresses on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. This sends the RAM starting row and column addresses once only, and then treats all subsequent data as display information. The row and column addresses will be automatically incremented internally for each display information data from the starting location.

The data transmission formats are:

(a) R – > C– > I –> R – > C – > I – > . . . . . .

(b) R – > C – > I – > C – > I – > C – > I. . . . . .

(c) R – > C – > I – > I – > I – > . . . . . .

To differentiate the row and column addresses when transferring data from master, the MSB (Most Significant Bit) is set as in Figure 5: '1' to represent row, while '0' for column address. Furthermore, to distinguish the column address between format (a), (b) and (c), the sixth bit of the column address is set to '1' which represents format (c), and a '0' for format (a) or (b). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

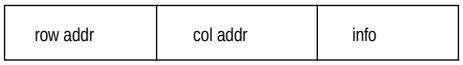


Figure 4. Data Packet

ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	X	X	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 5. Row & Column Address Bit Patterns

MEMORY MANAGEMENT

Internal RAM are addressed with row and column (coln) number in sequence. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character ROM address corresponding to display location on monitor screen. Every data row associate with two control registers, which locate at coln 30 and 31 of their respective rows, to control the characters display format of that row. In addition, three window control registers for each of three windows together with six frame control registers occupy the first 15 columns of row 15 space. The PWM registers are located from column 20 to 31.

User should handle the internal RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on

screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

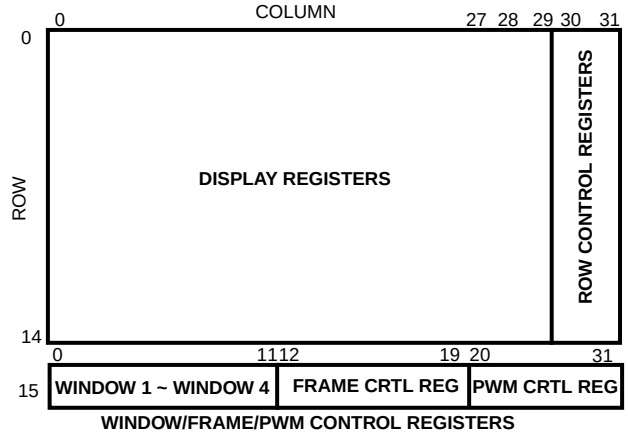
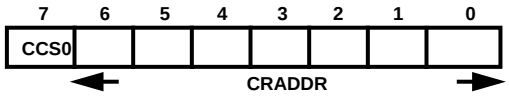


Figure 6. Memory Map

REGISTERS

Display Register

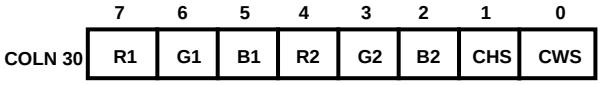


Bit 7 CCS0 - This bit defines a specific character color out of the two preset colors. Color 1 is selected if this bit is cleared, and color 2 otherwise.

Bit 6-0 CRADDR - This seven bits address the 128 characters or symbols resided in the character ROM.

Row Control Registers

Coln 30

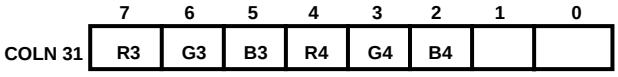


Bit 7-2 Color 1 is determined by R1, G1, B1 and color 2 by R2, G2, B2. Refer to Table 1 for color selection.

Bit 1 CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

Coln 31



Bit 7-2 Color 3 and 4 are defined by R3, G3, B3, and R4, G4, B4 respectively.

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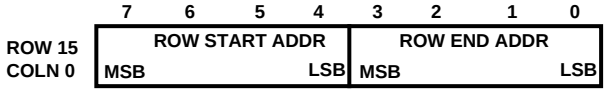
Table 1. The Character/Window Color Selection

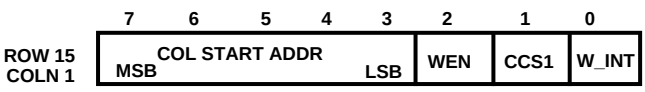
	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Window 1 Registers

Row 15 Coln 0



Row 15 Coln 1

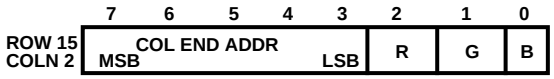


Bit 2 WEN - It enables the background window 1 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 1 with two extra color selections, making a total of four selection for that row.

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 1. If this bit is 0, INT pin will go low while displaying window 1. The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

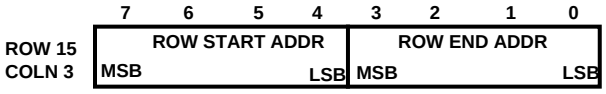
Row 15 Coln 2



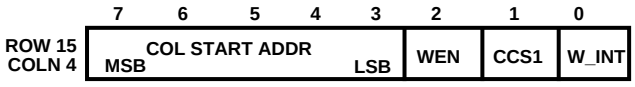
Bit 2-0 R, G and B - Controls the color of window 1. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3



Row 15 Coln 4

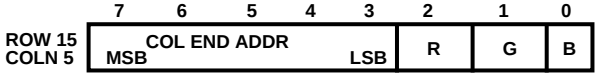


Bit 2 WEN - It enables the background window 2 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 2 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 2. If this bit is 0, INT pin will go low while displaying window 2. The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

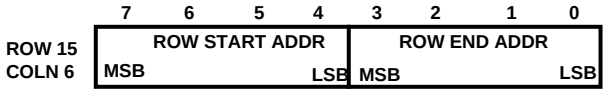
Row 15 Coln 5



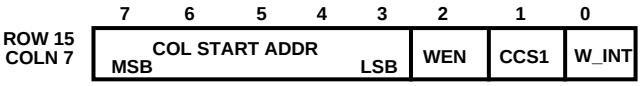
Bit 2-0 R, G and B - Controls the color of window 2. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6



Row 15 Coln 7

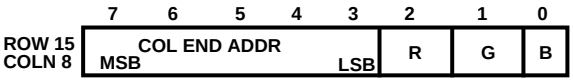


Bit 2 WEN - It enables the background window 3 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 3 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 3. If this bit is 0, INT pin will go low while displaying window 3.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

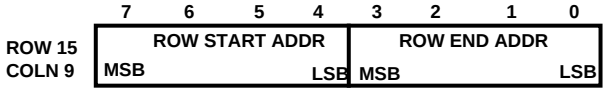
Row 15 Coln 8



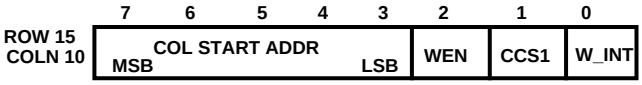
Bit 2-0 R, G and B - Controls the color of window 3. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9



Row 15 Coln 10

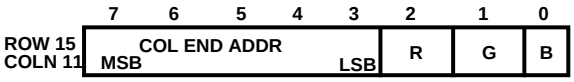


Bit 2 WEN - It enables the background window 4 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 4 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 4. If this bit is 0, INT pin will go low while displaying window 4.The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

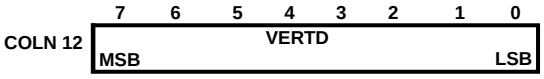
Row 15 Coln 11



Bit 2-0 R, G and B - Controls the color of window 4. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

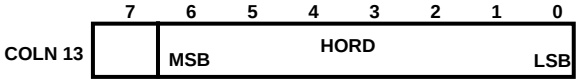
Frame Control Registers

Frame Control Register Row 15 Coln 12



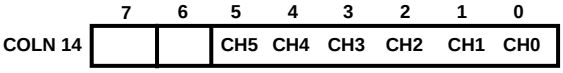
Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Frame Control Register Row 15 Coln 13



Bit 6-0 HORD - Horizontal starting position for character display. 7 bits give a total of 128 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value of it is 15.

Frame Control Register Coln 14



Bit 5-0 CH5-CH0 - This six bits will determine the displayed character height. AMOSD II adopts 12 by 18 font matrix and the middle 16 lines, line 2 to line 17, are expanded by BRM algorithm. The top line and bottom line will be duplicated dependent on the value of CH. No any line is duplicated for top and bottom if CH is less than 32. One extra duplicated line will be inserted for top and bottom if CH is larger or equal to 32 and less than 48. Two extra duplicated lines will be inserted for top and bottom if CH is larger or equal to 48. Setting a value below 16 will not have a predictable result. Display character line number is equal to C1 x (18 + C2) where C1 = 1, 2 or 3 defined by CH5-CH4 and C2 = 0-15 defined by CH3-CH0 (BRM).

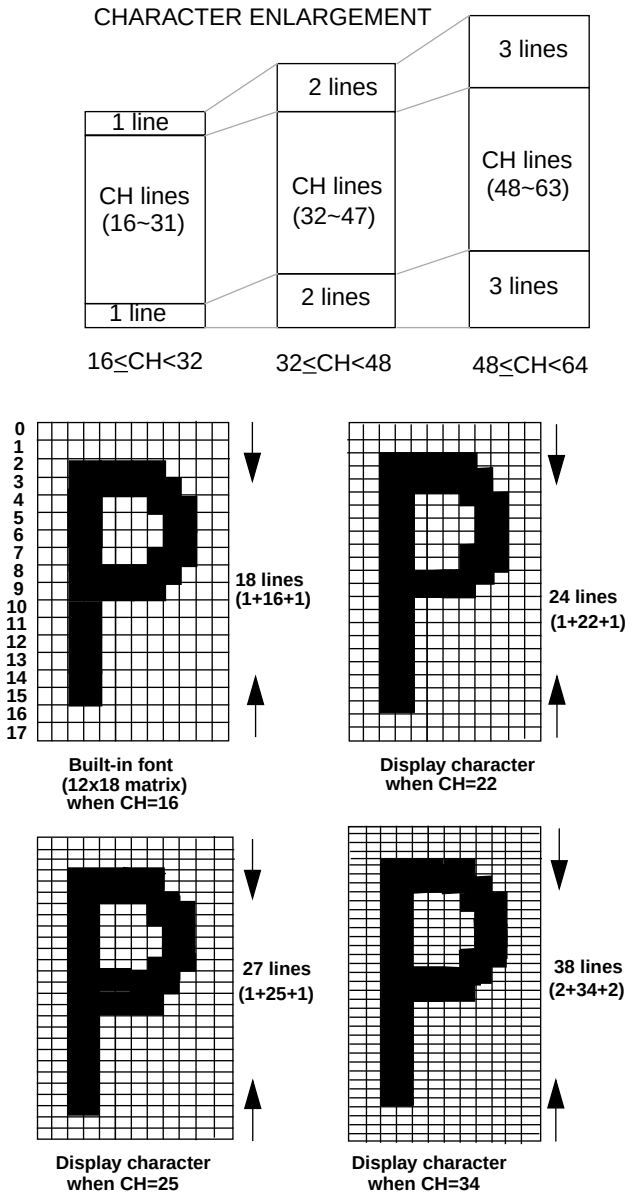


Figure 7. Variable Character Height

Figure 7 illustrates the enlargement algorithm for top and bottom lines and how this chip expand the built-in character font to the desired height.

In this approach, the actual character height in unit of the scan line can be calculated from the following simple equation:

H = CH + N

Where H is the expanded character height in unit of lines

CH is the number defined by CH5 ~ CH0

N is a variable dependent on the value of CH

N = 2 when 16≤CH<32

N = 4 when 32≤CH<48

N = 6 when 48≤CH<64

Frame Control Register Row 15 Coln 15

	7	6	5	4	3	2	1	0
ROW 15 COLN 15	OSD_EN	BSEN	SHADOW		X32B	3_S		FBKGC

Bit 7 OSD_EN - OSD circuit is activated when this bit is set.

Bit 6 BSEN - It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW - Character with black-edge shadowing is selected if this bit is set, otherwise bordering prevails.

Bit 3 X32B - It determines the number of dots per horizontal line. There are 384 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 768 dots per horizontal sync line when bit X32B is set to 1. Please refer to the Table 2 for details.

Table 2. Resolution Setting

X32B	0	1
Dots / Line	384	768
Resolution	CGA	SVGA

Bit 2 3_S - By setting this bit to 1, R/G/B could output high impedance state if the intensity attribute of windows is set to 0. It means the corresponding R/G/B output will go high impedance instead of driving-high while displaying the low intensity windows which can be implemented by simple external circuit. After power on, this bit is reset and the R/G/B are push-pull outputs initially.

Bit 0 FBKGC - It determines the configuration of FBKG output pin. When it is clear. FBKG pin outputs high during displaying characters or windows. Otherwise, FBKG pin outputs high only during displaying characters.

Frame Control Register Row 15 Coln 16

	7	6	5	4	3	2	1	0
COLN 16				RSPACE				
				MSB				LSB

Bit 4-0 RSPACE - These 5 bits define the row to row spacing in unit of horizontal scan line. It means extra N lines, defined by this 5-bit value, will be appended for each display row. Because of the nonuniform expansion of BRM used by character height control, this register is usually used to maintain the constant OSD menu height for different display modes instead of adjusting the character height. The default value of it is 0. It means there is no any extra line inserted between row and row after power on.

Frame Control Register Row 15 Coln 17

	7	6	5	4	3	2	1	0
ROW 15 COLN 17					HF	TRIC	HPOL	VPOL

Bit 2 TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 3 HF - High Frequency Bit. If the incoming H sync signal is higher than 60 KHz, set this bit to 1 for better performance. This bit controls gain of internal VCO so that PLL can work for whole range from 15KHz to 120KHz.

Bit 1 HPOL - This bit selects the polarity of the incoming horizontal sync signal ($\overline{\text{HFLB}}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0 VPOL - This bit selects the polarity of the incoming vertical sync signal ($\overline{\text{VFLB}}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

Row 15 Col 18 to Col 19

	7	6	5	4	3	2	1	0
ROW 15 COLN 18								
ROW 15 COLN 19	Cout							

Bit 7 Cout – When this bit is set to 1,INT/Cout pin will be switched to a clock output which is synchronous to the H sync and used as an external PWM (pulse width modulation) clock source. Refer to the pin description of INT/Cout for more information. After power on, the default value is 0.

PWM Control Registers Row 15 Col 20 to Col 31

	7	6	5	4	3	2	1	0
ROW 15 COLN 20-31	MSB			PWM_n				LSB

Bit 7-0 PWM_n - This eight-bit value decides the output duty cycle and waveforms of PWM. There are maximum 12 channels of PWM. And the corresponding registers are located from column 20 to column 31 respectively on row 15.

The higher five bits (MSB) are used for the conventional PWM and the lower 3 bits (LSB) for the BRM. Please refer to the following figures for more information about BRM algorithm and PWM output waveform.

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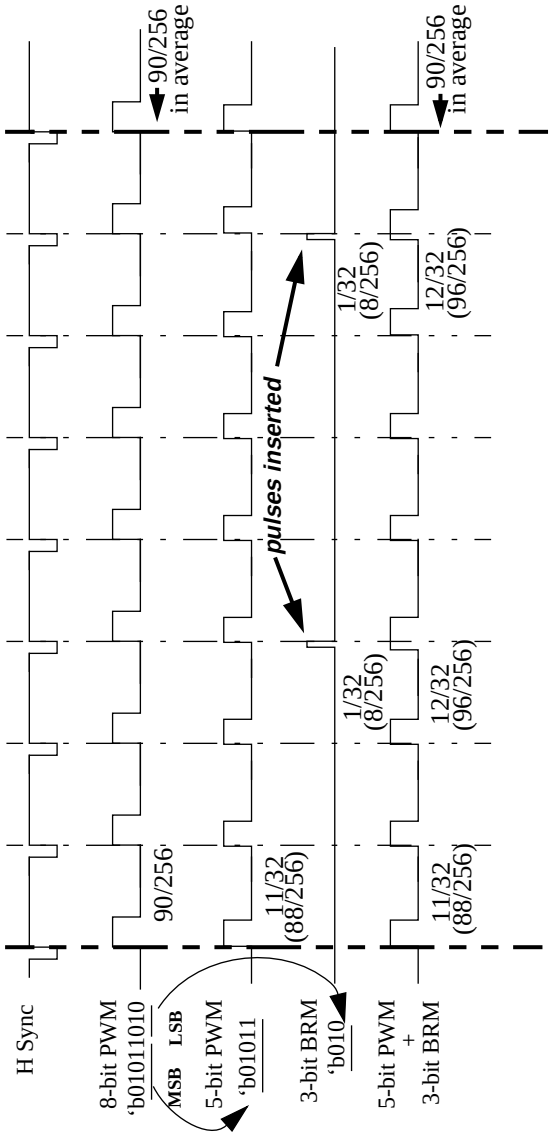

Figure 8. Pure 8-bit PWM v.s. 5-bit PWM + 3-bit BRM

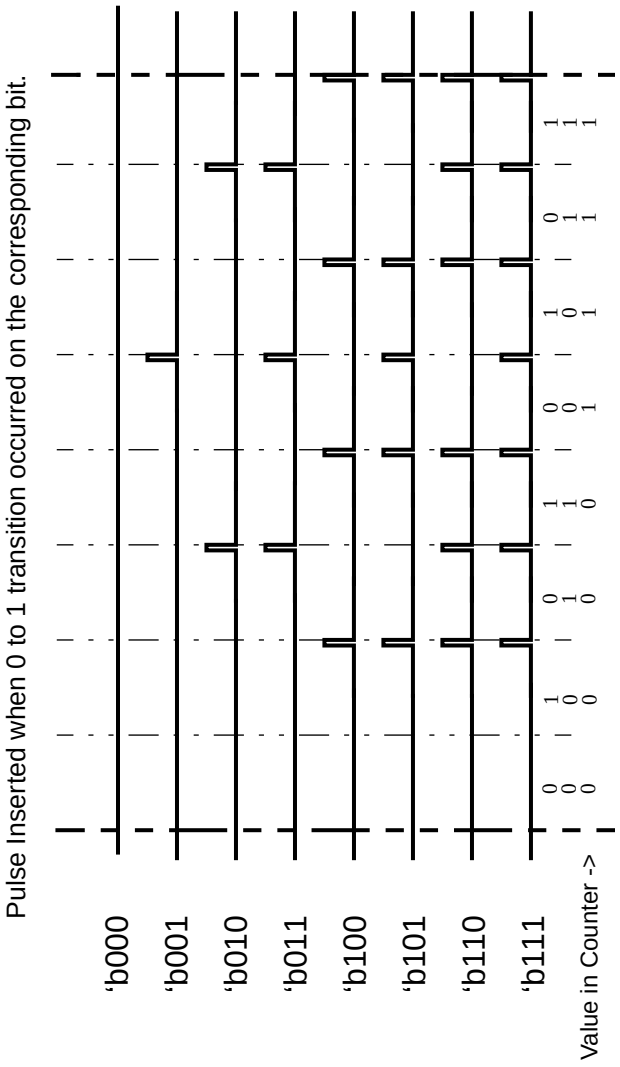

Figure 9. BRM Pulse Insertion Algorithm

Frame Format and Timing

Figure 10 illustrates the relative positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 10 for horizontal and vertical delays: fixed delays from the leading edge of $\overline{\text{HFLB}}$ and $\overline{\text{VFLB}}$ signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Please refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of external charge-up resistor, which is the 1M Ohm resistor in series with 5.6KOhm to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 384 if the bit X32B is clear and H Freq. x 768 if bit X32B is set to 1. For example, dot frequency is 12.288MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1, the dot frequency will be 24.576MHz (double of the original one).

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configured each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of $\overline{\text{VFLB}}$ of next frame to avoid wrapping display characters of the last few rows in current frame into next frame. The number of display dots in a horizontal scan line is always fixed at 360, regardless of row character width and the setting of bit X32B.

Although there are 30 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 384 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 768 dots, 30 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 11 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters are used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only.

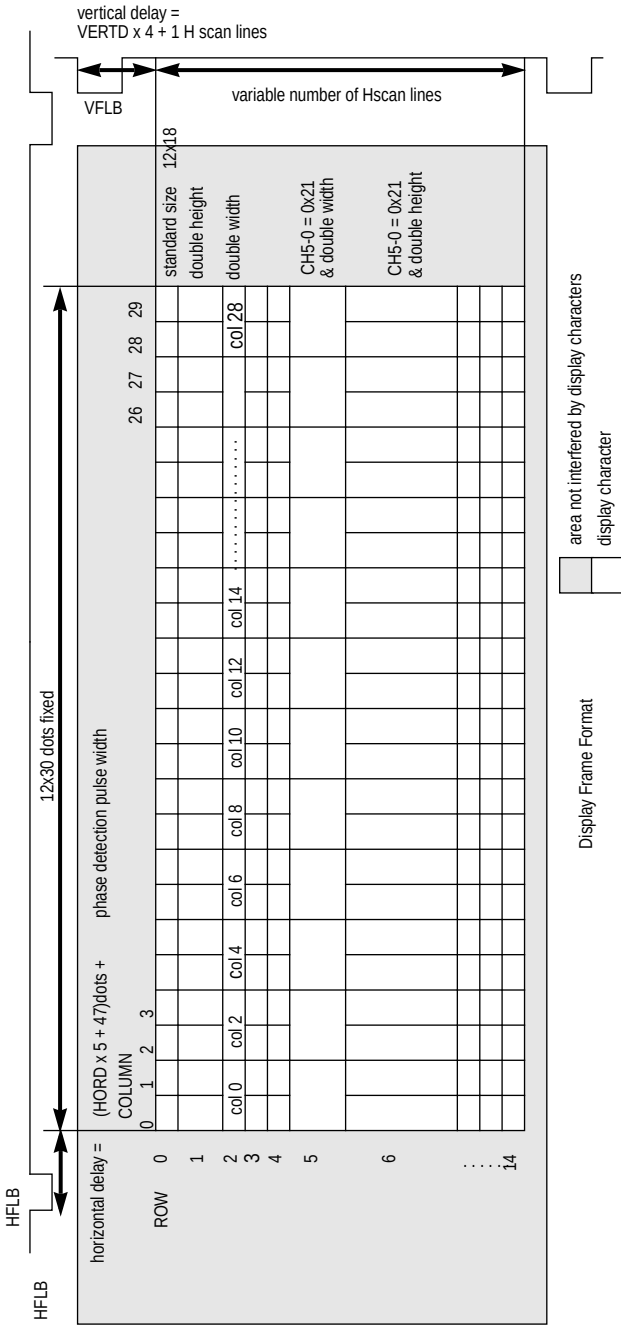

Figure 10. Timing of Output Signals

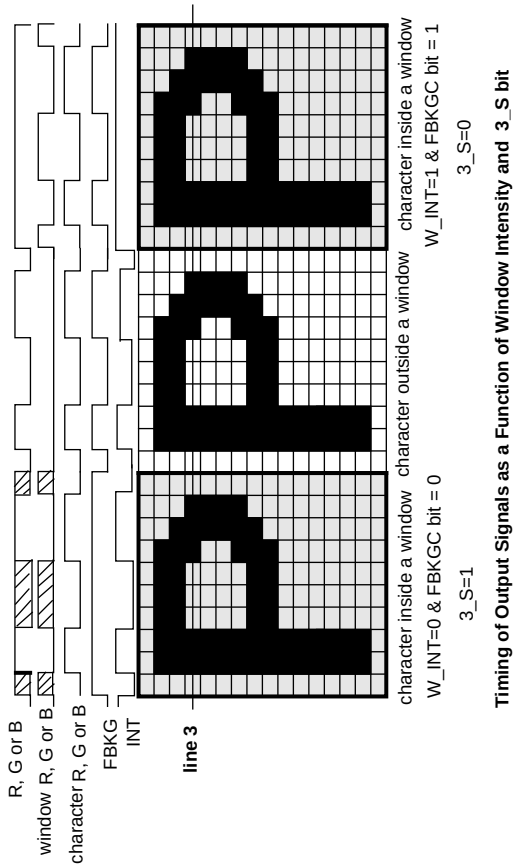

Figure 11. Display Frame Format

A software called AMOSD II FONT EDITOR in IBM PC environment was written for MC141546P2 editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141546P2.

In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 12x18 matrix, and let its spaces be equally located in the four sides of the matrix. The character $00 is pre-defined for blank character, the character $FF is pre-defined for full-filled character.

In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 12 shows how a character is being jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font.

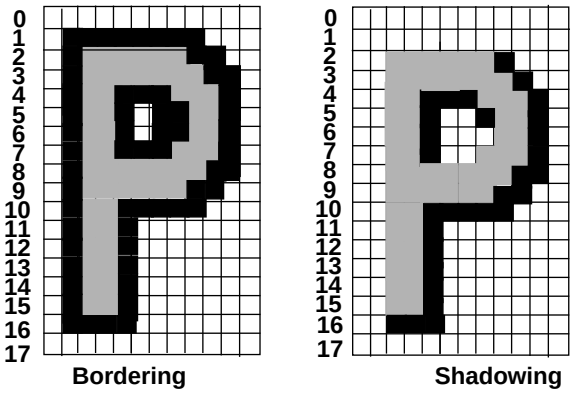

Figure 12. Character Bordering and Shadowing

FONT

Icon Combination

MC141546P2 contains 128 character ROM. The user can create an on-screen menu based on those characters and icons. Refer to Table 3 for icon combinations. Address $00 and $7F are predefined characters. They cannot be modified in any AMOSD II.

Table 3. Combination Map

ICON	ROM ADDRESS(HEX)
ARABIC NUMERALS	01-0A
ALPHABET	0B-26
EUROPEAN	27-41
SYMBOLS	42-61, 7E
GEOMETRY	C5-EE

ROM CONTENT

Figures 13 – 14 show the ROM content of MC141546P2. Mask ROM is optional for custom parts.

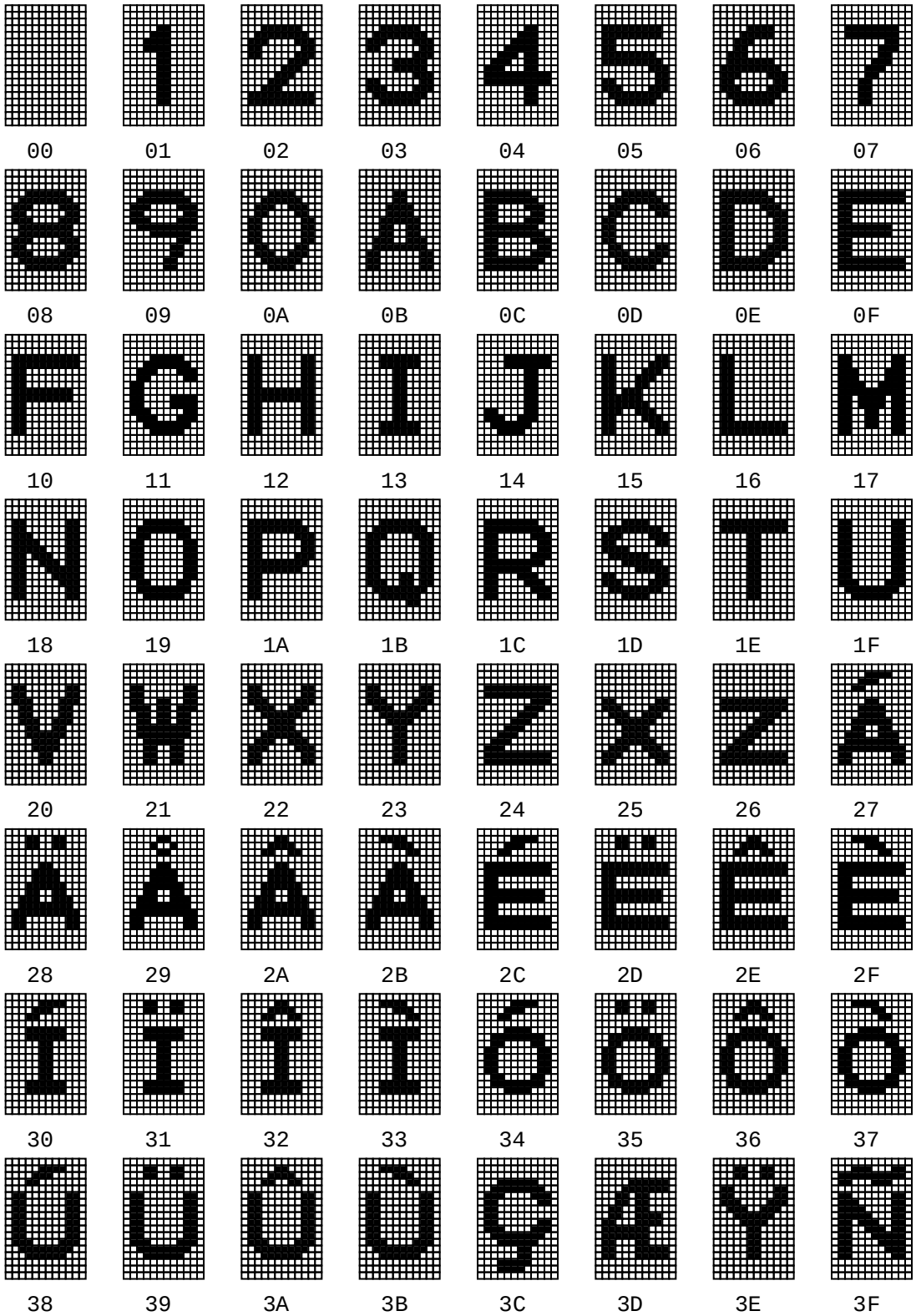

Figure 13. ROM 00 - 3F

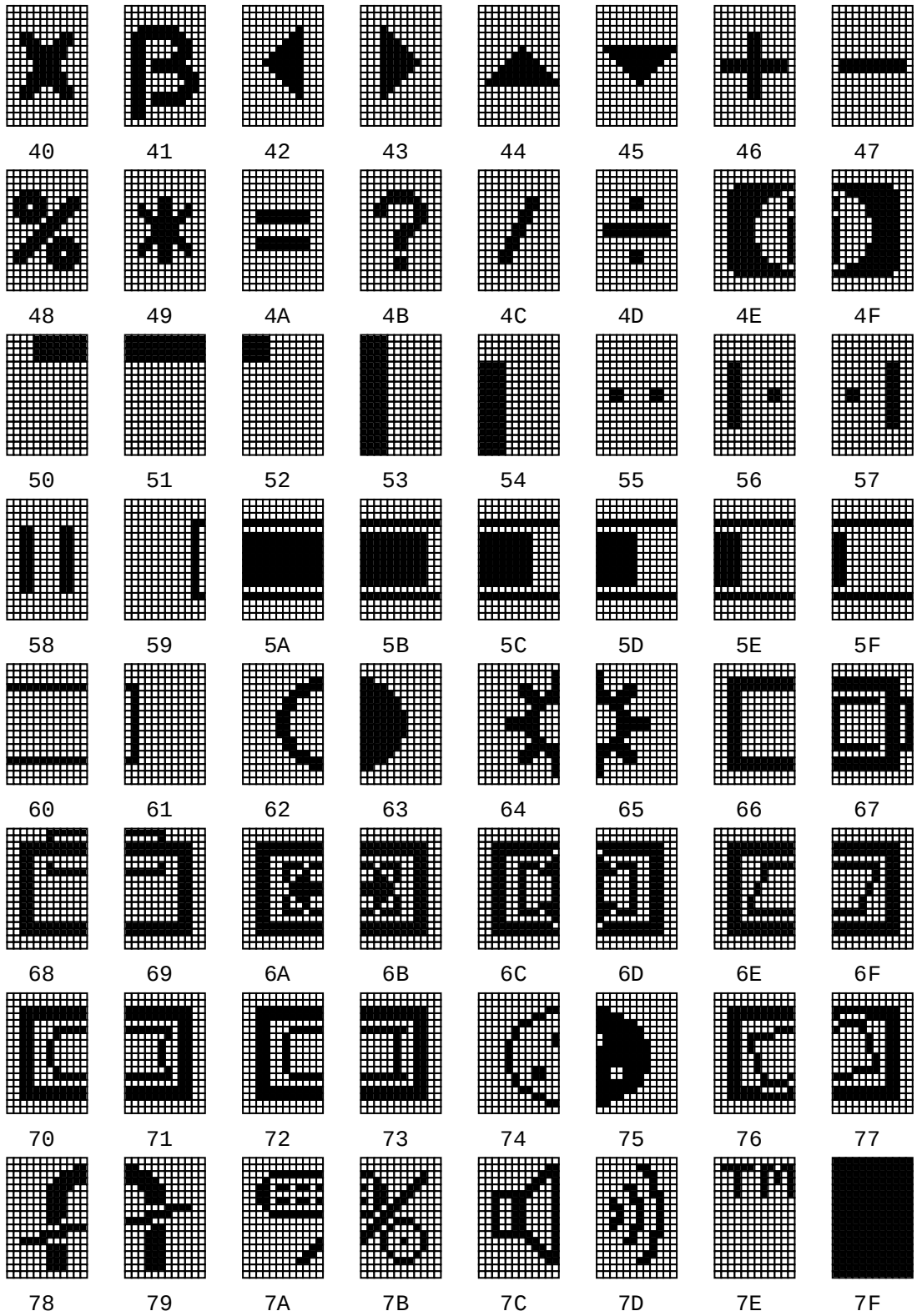

Figure 14. ROM 40 - 7F

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141546P2 has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 384/768 x HFLB (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating outside, they are connected internally). Refer to the Application Diagram for the ground connections.(NOTE: Vss(A) and Vss are connected internally.)
- DC supply path for Pin 4 ($V_{DD(A)}$) should be separated from other switching devices.
- LC filter should be connected between Pin 17 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.

Jittering and Unlocking

Most display jittering and unlocking is caused by HFLB in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. Buffer is needed for both HFLB and VFLB inputs. Refer to the value used in the Application Diagram.

Display Dancing

Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM