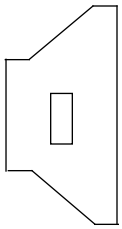
MC141524

Source (Column) Driver for TFT Type LCD Panel
CMOS



MC141524T1
TAB

ORDERING INFORMATION

MC141524T1 TAB

The MC141524 is a high voltage LCD source driver. It is a low power silicon-gate CMOS LCD driver chip which consists of 120 channels source drive to provide the drain bus signal of a TFT (Thin-Film-Transistor) LCD panel.

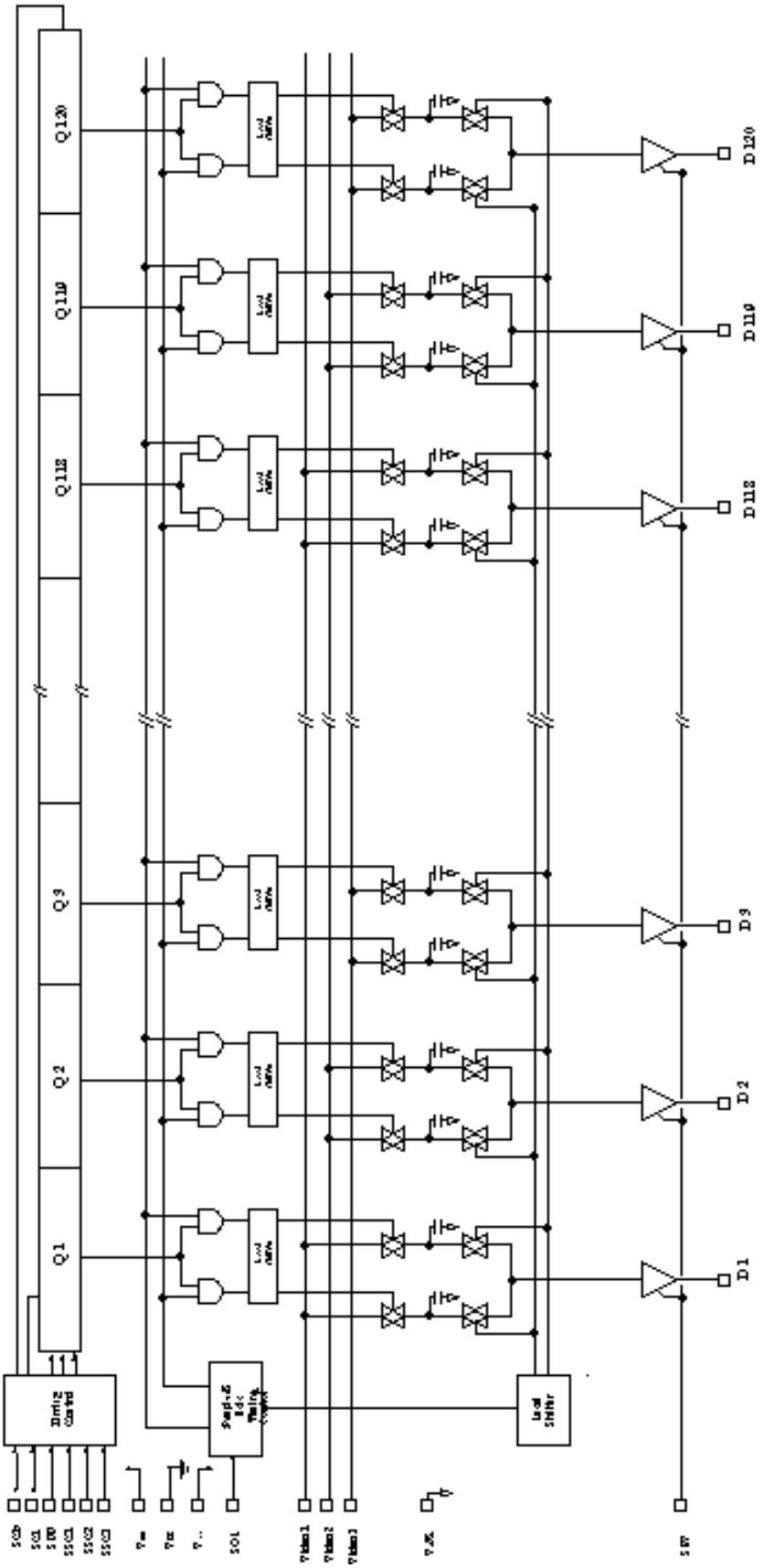
This chip accepts the three video signals R, G, B. The built-in sample and hold circuitry will sample the video signals and hold these signals before outputting to drive the TFT-LCD panel.

The MC141524 will provide the best performance in combination with the MC141522 (gate driver). The two devices can drive LCD panels from 480 x 240 pixels middle-resolution up to 720 x 480 pixels high-resolution by cascading.

- Operating Supply Voltage Range
  - Logic (V_{DD} pin): 4.5V to 5.5V
  - (V_{EE} pin): -5V to -10V
  - Output Drive (V_{DD} - V_{EE}) = 10V to 15V
- Dynamic Range: 11.0 Volts Peak to Peak
- Operating Temperature Range: -30 to 85 C
- 120 - Column Output Driver
- 2 Sample & Hold Cells Structure
- Bi-directional Shift Register with Interchanging Carry-Borrow Terminals
- Left / Right Shift Mode Selection
- Maximum Sampling Frequency = 30MHz (Three Phase (3ø)'s Operation)
- Video Bandwidith (-3dB): 5.0MHz
- Programmable Buffer Output Drive with External Resistor
- Cascadable
- Available in TAB (Tape Automated Bonding), 152 pins

REV 4
10/96

BLOCK DIAGRAM



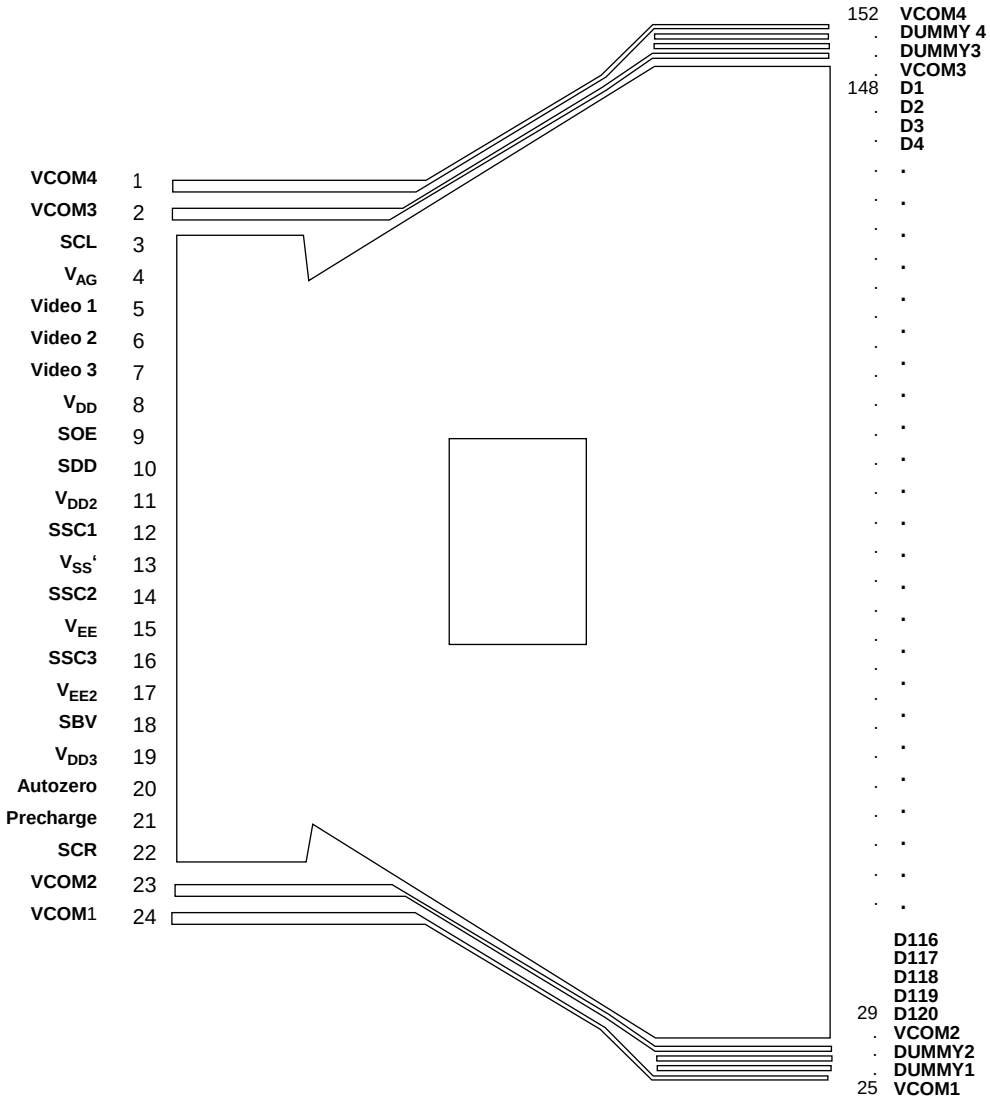


Figure 1A. TAB Package Contact Assignment (Copper View)

ABSOLUTE MAXIMUM RATING (Voltage Referenced to VSS)

RATING	SYMBOL	VALUE	UNIT
Logic Supply Voltage	V_{DD}	+6.0	V
Negative Supply Voltage	V_{EE}	-16.0	V
DC Supply Voltage	V_{DD} - V_{EE}	+22	V
Input Voltage All Digital Input	V_{di}	V_{SS} - 0.5 to V_{DD} + 0.5	V
Input Voltage Analog Video Input	V_{ai}	V_{SS} - 0.5 to V_{DD} + 0.5	V
Operating Temp. Range	T_a	-30 to 85	^oC
Storage Temp. Range	T_{stg}	-55 to +150	^oC

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Logic Supply Voltage	V_{DD}	+4.5	+5	+5.5	V
Negative Supply Voltage	V_{EE}	-5	-8	-10	V
DC Supply Voltage	V_{DD} - V_{EE}	10	--	15	V
Operating Temperature	T_a	-20	--	+75	^oC

AC ELECTRICAL CHARACTERISTICS

V_{DD}=5.0 V, V_{SS}= 0V,V_{EE}=-10 V, T_A=25 C, Voltage referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
Control Input Rise Time Fall Time (SOE, SCR, SCL, SSC1,2,3)	 t_{TLH} t_{THL}	 -- --	 10 10	 20 20	 ns ns
Shift Clock (SSC) to sampling activated Shift Register Output HIGH Shift Register Output LOW	 t_{PLHR} t_{PLHR}	 -- --	 5 5	 10 10	 ns ns
Carry In to Shift Clock (SSC1) Set Up Time	t_{SUC}	--	20	--	ns
Carry In Pulse Width (SCR/SCL)	t_{WC}	80% of $t_{sø}$	--	--	ns
Shift Clock Cycle (SSC1,2,3)	$t_{sø}$	100	--	1000	ns
Shift Clock Pulse Width HIGH Shift Clock Pulse Width LOW (SSC1,2,3)	t_{SCH} t_{SCL}	40% of $t_{sø}$ 40% of $t_{sø}$	-- --	-- --	ns ns
Shift Clock n to Shift Clock n+1 Phase Delay	t_{SCT}	30	--	--	ns
Propagation Delay Time Low to High Carry Output from SSC High to Low Carry Output from SSC C_L = 100pF	 t_{PLHC} t_{PLHC}	 -- --	 10 10	 30 30	 ns ns

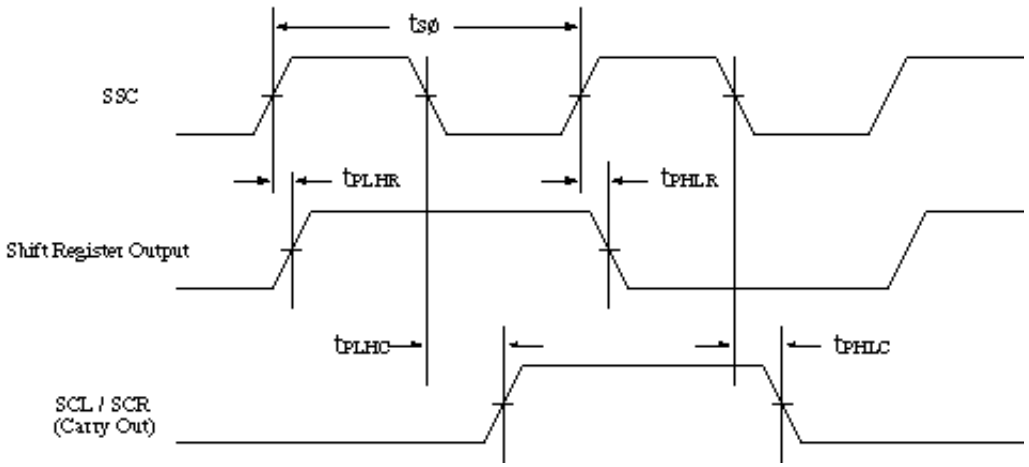


Figure 1. Shift Clock, SR Output and Carry Out Propagation Delay Timing Diagram

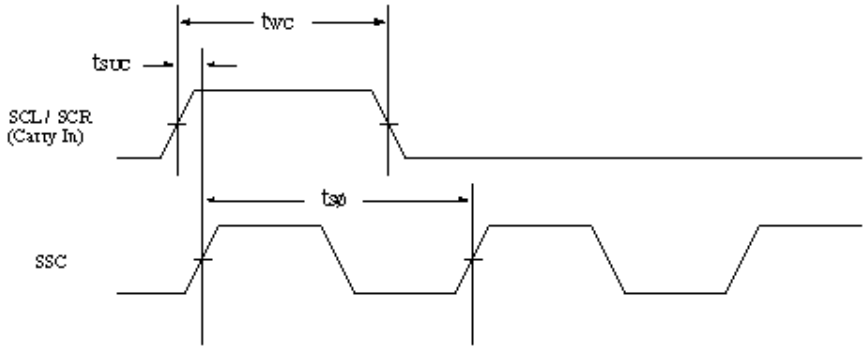


Figure 2. Shift Clock and Carry In Propagation Delay Timing Diagram

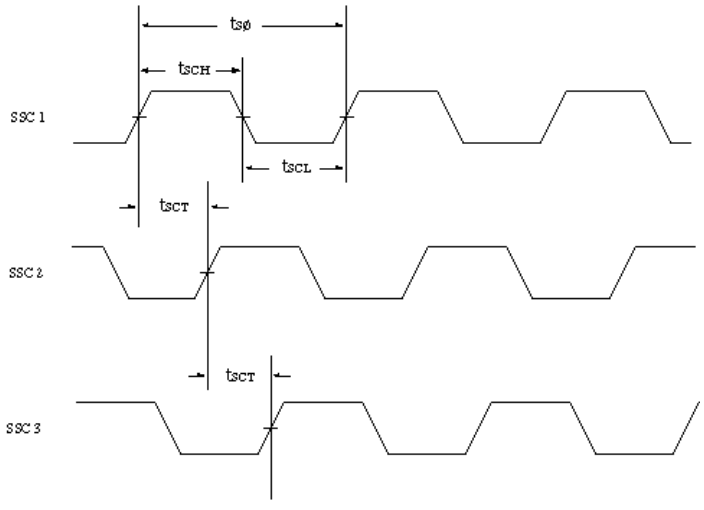


Figure 3. Three Phase Shift Clock Phase Shift Delay Timing Diagram

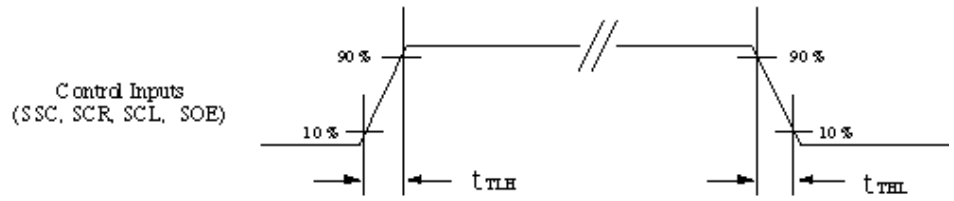


Figure 4. Control Input Rise and Fall Time

DC ELECTRICAL CHARACTERISTICS

V_{DD}=5.0 V, V_{SS}= 0V,V_{EE}=-10 V, T_A=25 C, Voltage referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
Control Input Voltage Level High	V_{IH}	3.2	--	5.5	V
Control Input Voltage Level Low	V_{IL}	0.0	--	1.2	V
SDD Input Voltage High	V_{IHS}	--	--	V_{DD}	V
SDD Input Voltage Low	V_{ILS}	V_{SS}	--	--	V
D_O Output Current					
High (V_O = V_{DD}-3.0V)	I_{OHX}	--	--	800	uA
Low (V_O = V_{EE}+2.0V)	I_{OLX}	800	--	--	uA
Bias Voltage Resistance Iag=15uA	R_{Ib}	6	7.2	12	K
Input Voltage Range	V_{SG}	V_{EE}+2.0	--	V_{DD}-2.0	V
Input Video Signal Dynamic Range		--	10	11	V_{pp}
Maximum Clock Input Frequency (CLK)	$Ø_{MAX}$	1.0	--	10.0	MHz
Current Consumption Shift Register constantly shifting one V_{DD}=5V, V_{EE}=-10V, Video1,2,3=-8V	I_C	--	10	30	mA
Sample & Hold Cell Gain	$G_{s/h}$	0.95	0.96	1.00	
Driver Output High (Video input = 3V)	V_{DOH}	2.8	--	3	V
Driver Output Low (Video input = -8V)	V_{DOL}	-8	--	-7.8	V

PIN DESCRIPTION

V_{SS}
This is the power supply GND connection pin for the logic circuitry of the chip.

V_{AG}
This is the power supply GND connection pin for the analog circuitry of the chip. Normally it is set to middle between V_{DD} and V_{EE} level.

V_{DD}
This is the positive 5 V power supply pin for both the logic and the analog circuitry of the chip.

V_{EE}
This is the power supply pin for the most negative supply voltage for the analog circuitry of the chip.

Precharge
This logic input pin provides the output reset function. When precharge is held low, all driver o/p will go to the analog group level “VGA”. When precharge is set high, all driver o/p is connected to the sample & hold cell (i.e. normal signal output).

Autozero
This is a logic input pin to reset output unity gain buffer before next signal is generated. Normally, it is connected together with precharge pin. User can ignore the Autozero and / or precharge function by tying it to high.

SBV (Source Bias Voltage)
This is the bias voltage supply pin for the unity gain output analog buffer. This bias voltage can control the buffer current driving capability.

The bias voltage is controlled by an external resistor connected between SBV and VEE. The lower resistance will produce higher current driving capability.

SSC1, SSC2, SSC3 (Source Driver Shift Clock 1,2,3)
This input clock signal is divided in Three Phase Operation (3ø) each with frequency of 10.0MHz maximum. Each phase controls the sampling timing of one video line signal. The equivalent operating frequency is 30.0MHz maximum.

Each clock signal will latch the carry signal through the Bi-directional Shift Register to determine the video signal sampling timing for the sample & hold cells.

SCL (Source Driver Carry-Left) / SCR (Carry-Right)
These two input / output pins perform the same function and depends on the SDD (Shift Direction Determination) Operation. In Shift Right mode, the SCL is the Carry input while the SCR is the Carry output for cascading. In shift Left mode, the pin functions and operations are vice versa. See Table 1.

SDD	Shift Direction		SCL	SCR
“0”	D1 to D120	Shift Right Mode	Input	Output
“1”	D120 to D1	Shift Left Mode	Output	Input

Table 1.Carry Shift Direction

SDD (Source Driver Shift Direction Determination)
This input pin determines the shift left / right operation of the Bi-directional Shift Register.

SDD = “0”, the system shift register will shift right.

SDD = “1”, the system shift register will shift left.

See Table 1.

SOE (Source Driver Output Enable)
This input pin determines the sample and hold output sequence of the unity cell (See Figure 9). It governs the sample and hold alternate timing operation between lines.

D001 to D120
These 120 output pins are sample and hold buffer outputs. These buffers output the sampled video signal and drive the source of the TFT of an active matrix LCD panel.

Bi-directional Shift Register

The 120-stage Bi-directional Shift Register controls the 120 corresponding sample and hold operation of the unity cell connected to each of the LCD driving output buffer. When the shift register bit content is “1”, the sample and hold circuit is in sampling state. The shift register is activated by shifting a “1” (Carry In) into the 1st stage of the shift register and the “1” value will latch through the register in turn performs the sample function of the unity cell.

The shift register is driven by a three phase clock. The maximum frequency of each phase clock is 10.0MHz and therefore the minimum sampling window is 100ns. The equivalent sampling rate of the source (common) driver is 30.0MHz. See figure 6, 7, 8, 9.

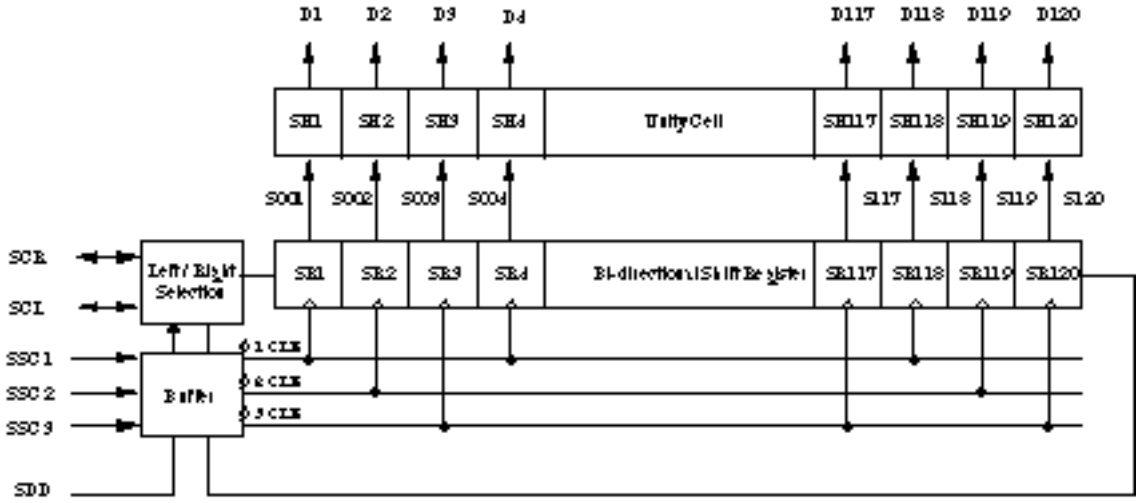


Figure 6. Bi-directional Shift Register Block Diagram

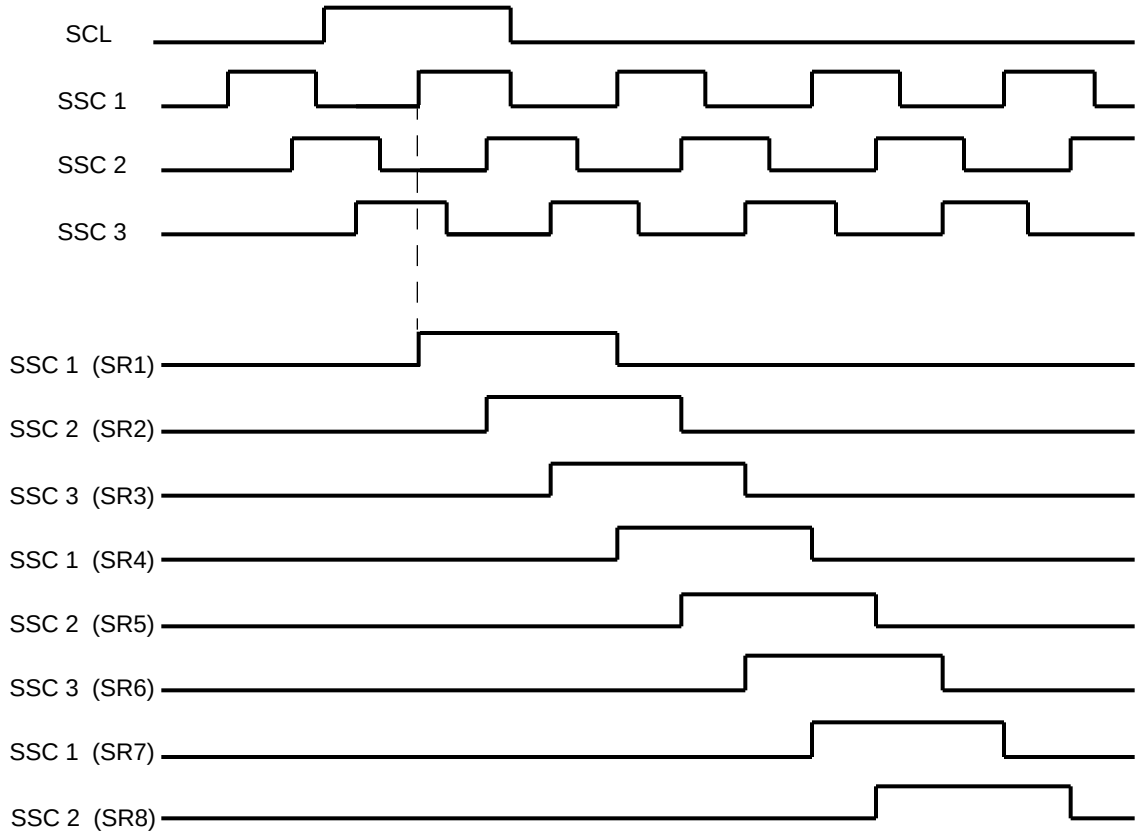


Figure 7. Shift Register Timing Diagram (Shift Right Mode)

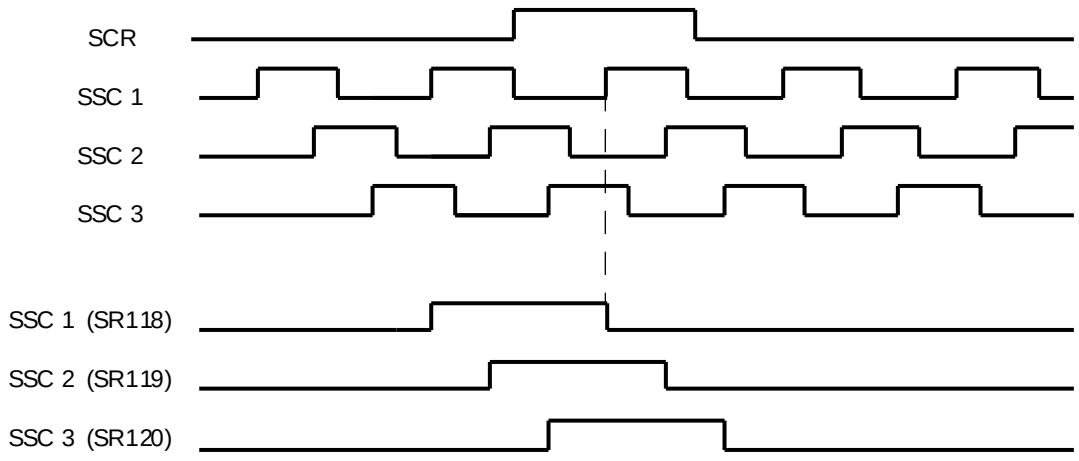


Figure 8. Carry Output Timing Diagram (Shift Right Mode)

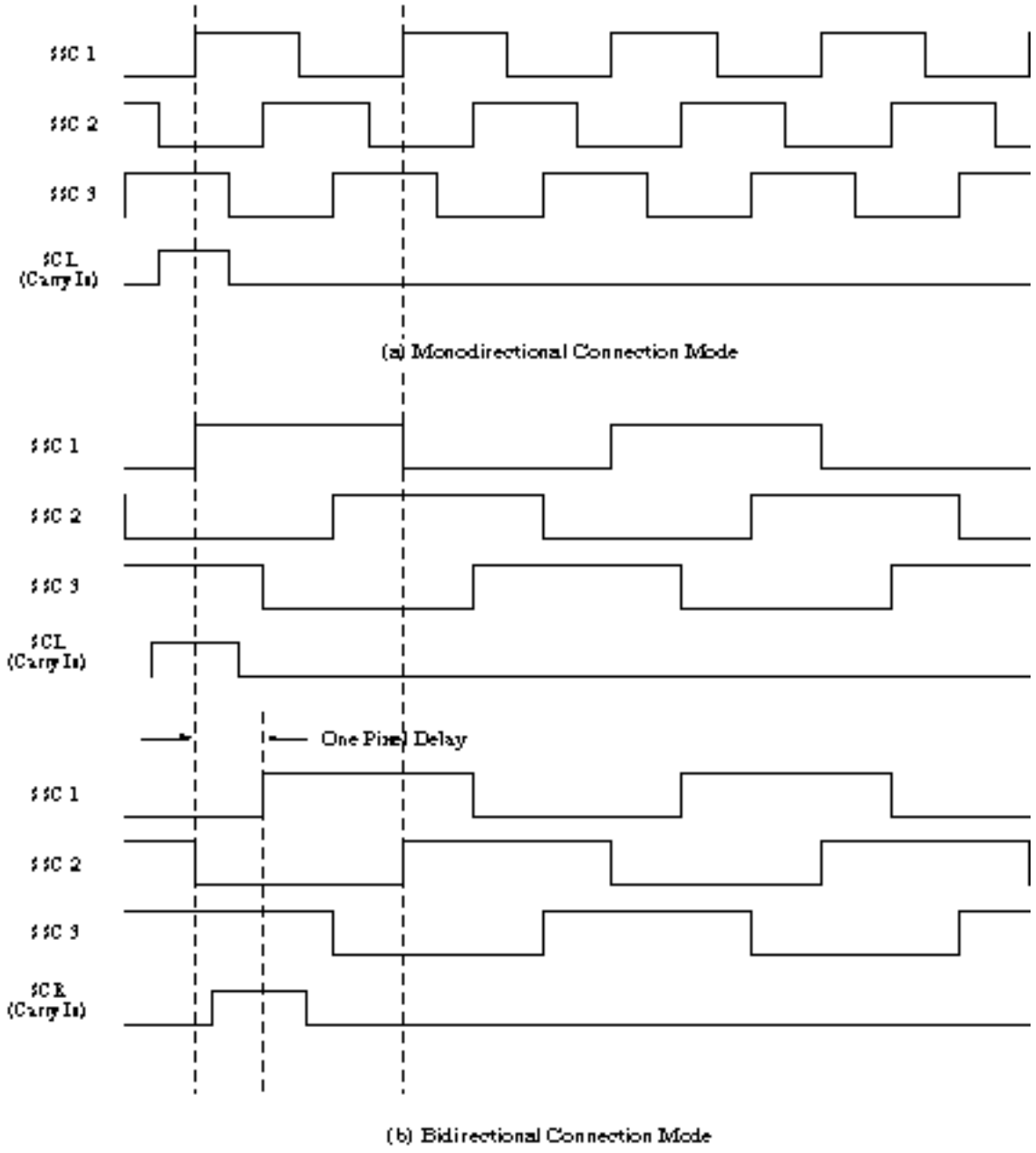


Figure 9. Three Phase Shift Clock Arrangement

SECTION 2

Unity Cell

The unity cell consists of 2 sample and hold circuitry and a unity gain buffer output. The 2 sample and hold cells are arranged in complementary fashion such that one cell is in sampling action while another cell is holding the charge that was sampled previously.

The selected sample and hold circuit samples the video signal of one horizontal scan line and read out in the next horizontal line scanning period; while the other selected sample and hold cell samples the video signal of that next scan line. See figure 10, 11, 12, 13.

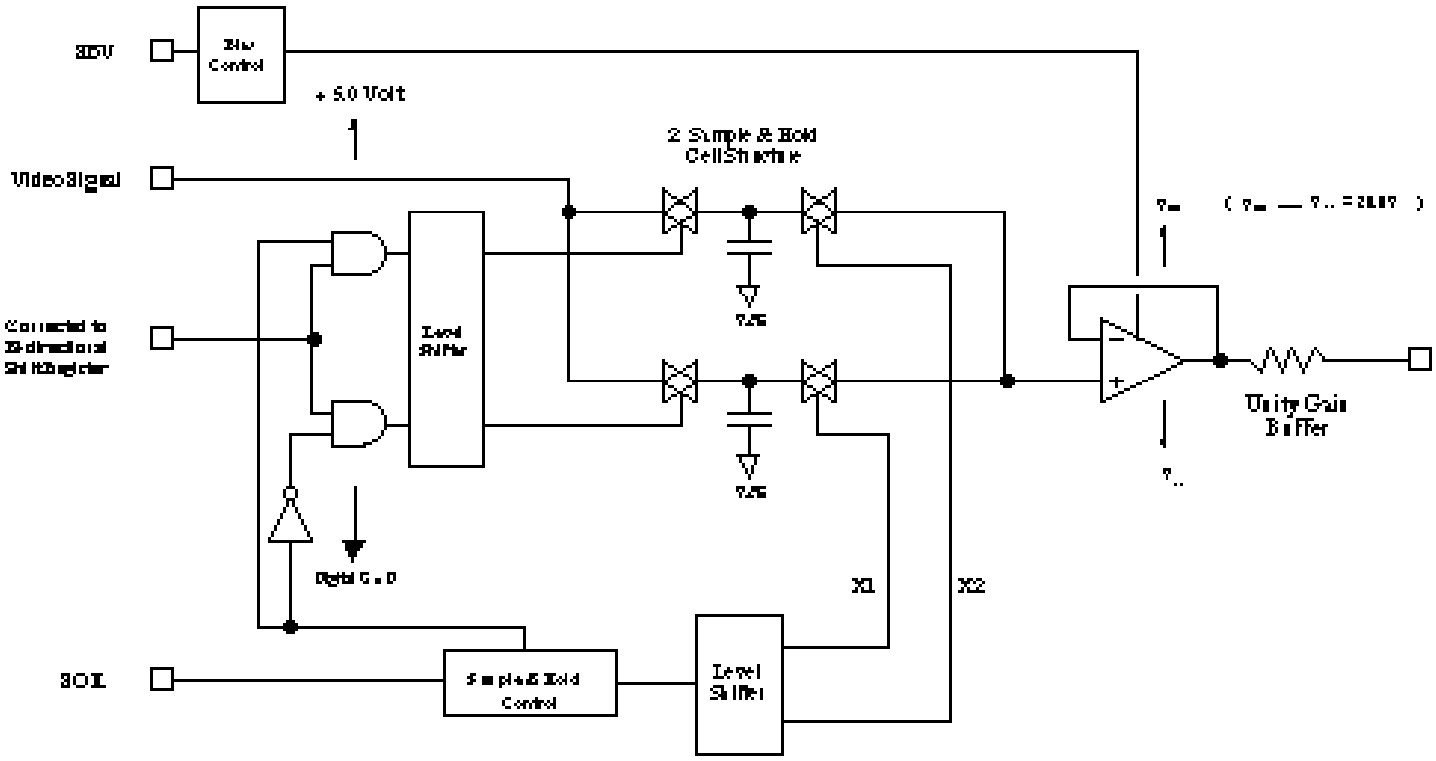


Figure 10. Sample and Hold Unity Cell Block Diagram

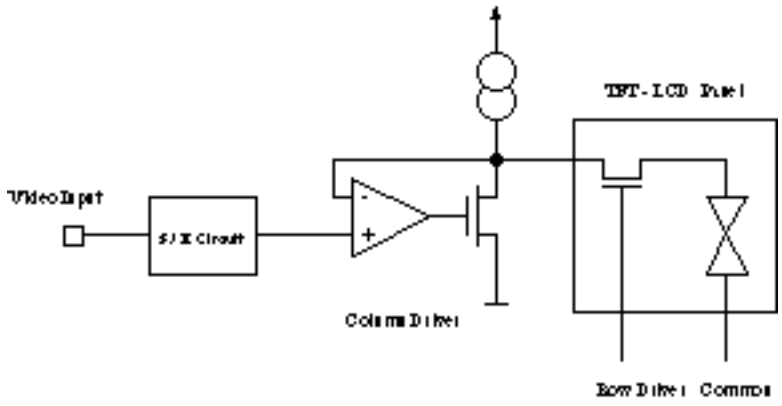


Figure 11. Sample and Hold Schematic

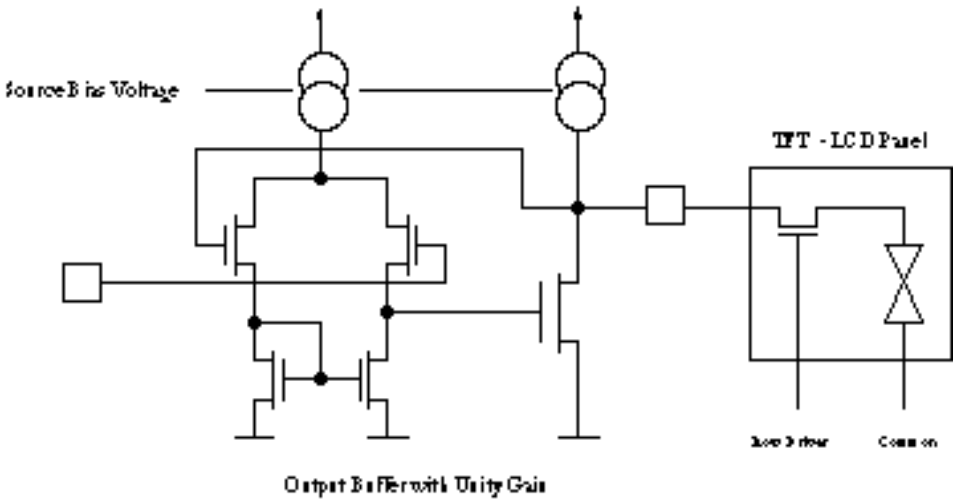


Figure 12. Unity Gain Buffer Schematic

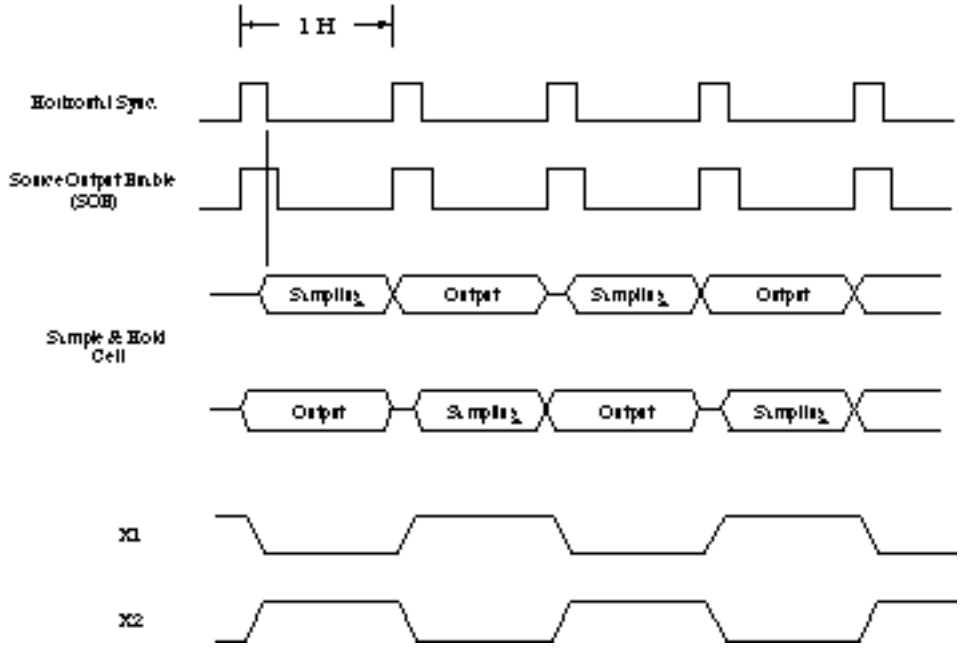


Figure 13. Sample and Hold Timing Diagram

SECTION 3

System Timing

In NTSC TV standard, the vertical synchronization signal period is 16.7ms while the horizontal synchronization signal period is 63.5us. There is about 10us horizontal retrace period in one line of video signal. The effective display period contributes 95% of the rest of valid display period. Therefore, the effective display period for single video line is about 50us. There is an half horizontal period shift between the odd field and even field, the effective display line video signal starts at the 19.0th lines scan after the vertical synchronization signal. The effective display line number for one field is 240 lines for single scan and 480 lines for double scan.

The Output Enable (SOE) control signal governs the sample and hold alternate timing operation between lines.

The driver controller has a VCO running at the required sampling rate to supply the system clock for the controller. The sampling clock is phase locked to the horizontal synchronization cooperated with the vertical synchronization signal. Odd field start and even field start signal are generated inside the controller to provide a timing signal for odd and even field start signal (Carry In). Once the start signal is generated, the column (source) driver starts sampling the video line signal while the row (gate) driver will output the latch signal one line after the start pulse to change the sampled video signal to the LCD panel through the TFT switches on the active matrix panel.

There are 240 row driver outputs for single scan and 480 row driver outputs for double scan “High resolution” panel. However, the sampling frequency of the source (column) driver will be defined by the number of horizontal pixels of the panel.

For example, if the number of horizontal pixel is 720, then the sampling frequency (fs) of the column driver will be defined by the following equation: (singe scan mode)

fs (signal scan)

= (1/effective display period)* (no. of display pixels)

= 720 / (63us*0.95)

= 14.4MHz

= 4.8MHz (using 3 phase clock)

The sampling frequency can be reduced by half if the column driver are placed in the bi-directional connection mode. See figure 6 and figure 12.

However, in the bi-directional connection mode, the controller has to provide a set of upper driver clock signal and lower driver clock signal. The phase shift between the upper and lower driver clock signal must be one pixel delay.

See Figure 14, 15.

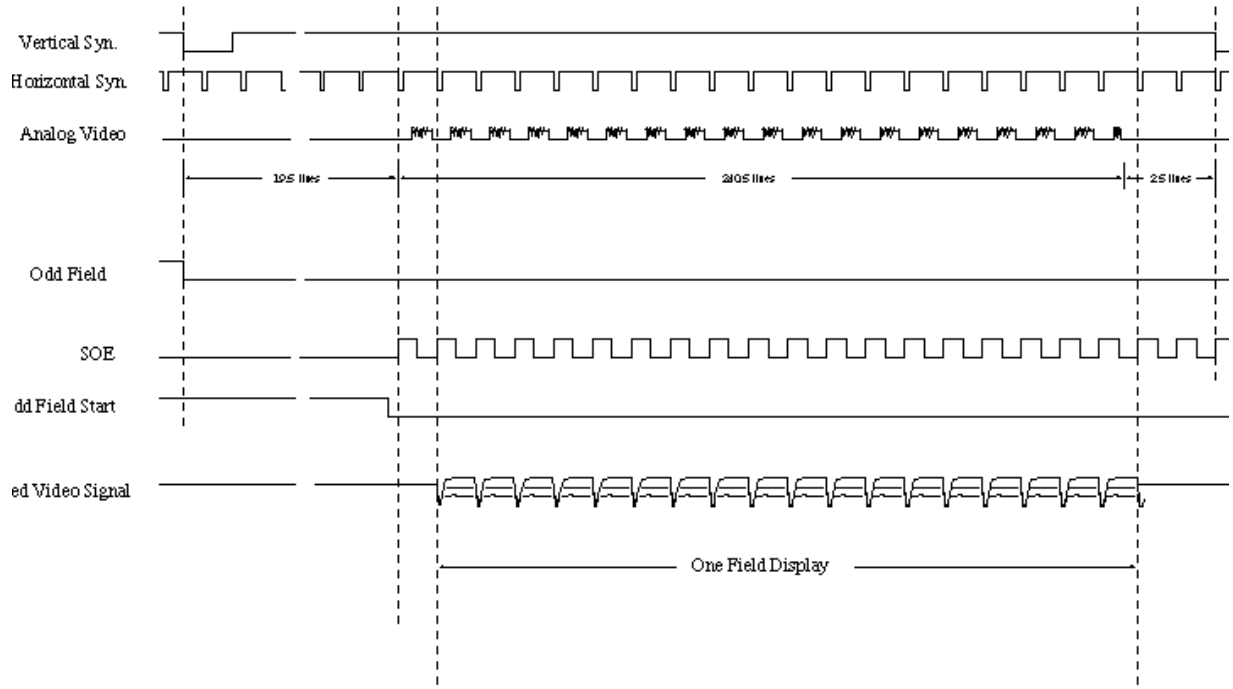


Figure 14. LCD-TV: Odd Field System Timing

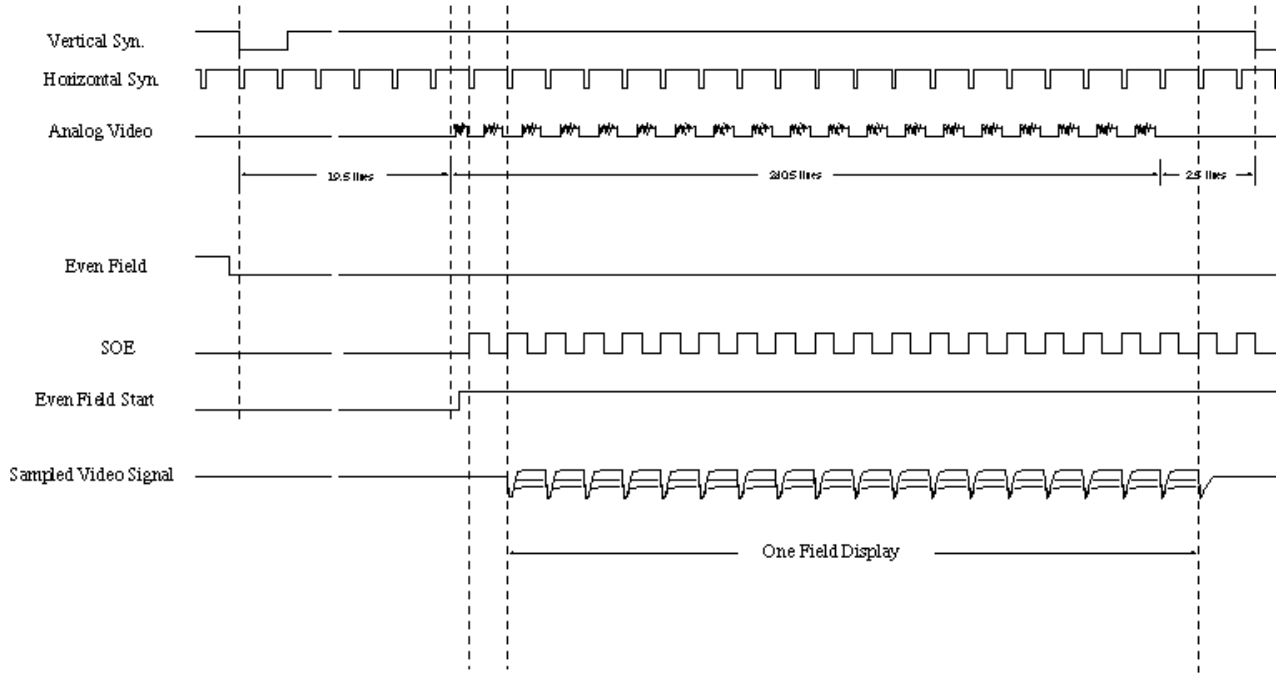


Figure 15. LCD-TV: Even Field System Timing

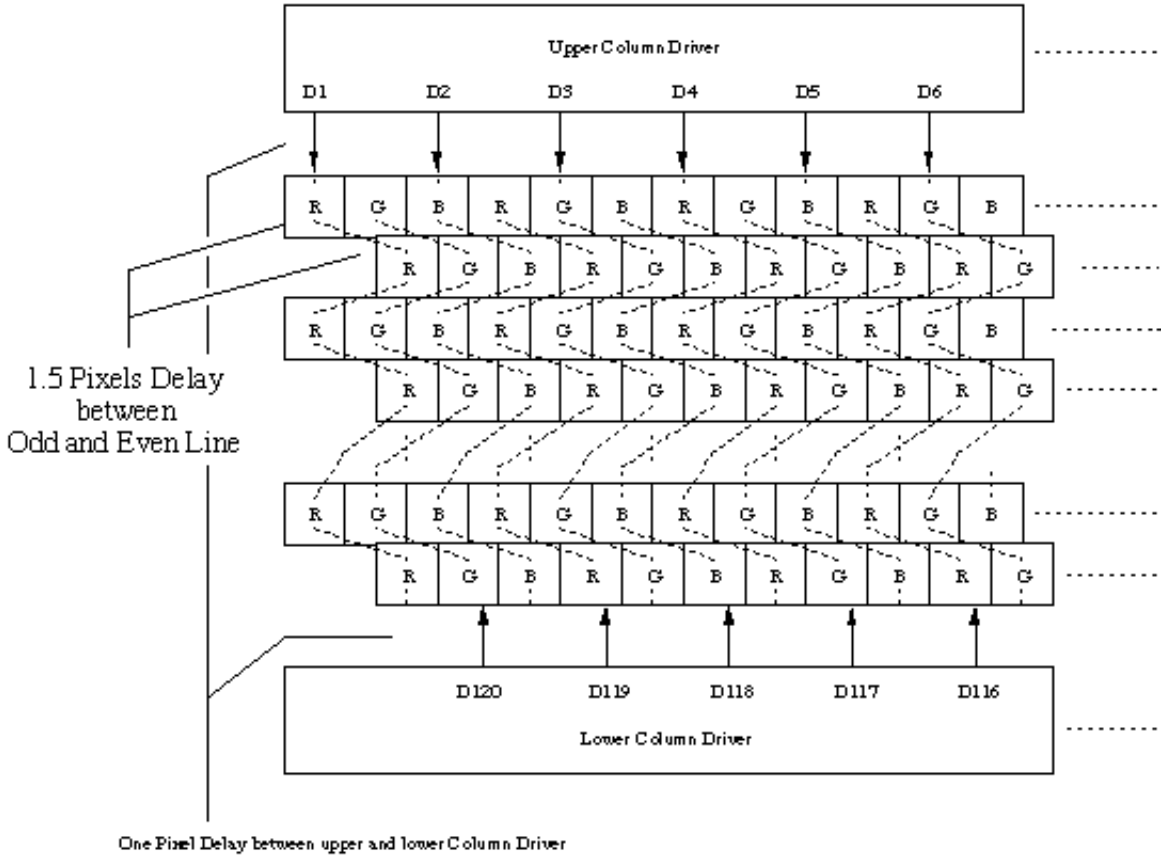


Figure 16. Sampling Pixel Delay with Upper and Lower Driver Arrangement

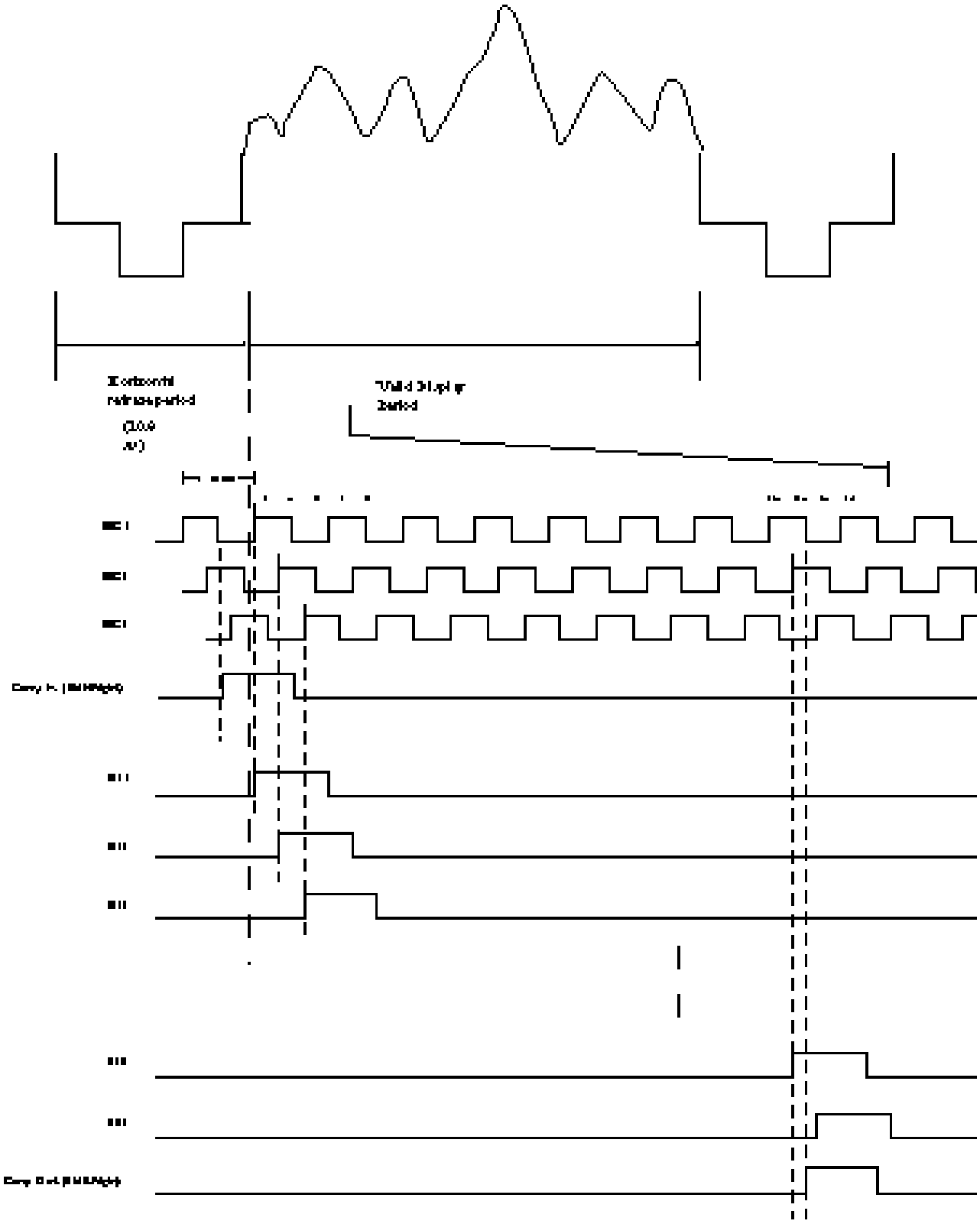


Figure 17. Source (Column) Driver Sampling of Video Line System Timing Diagram

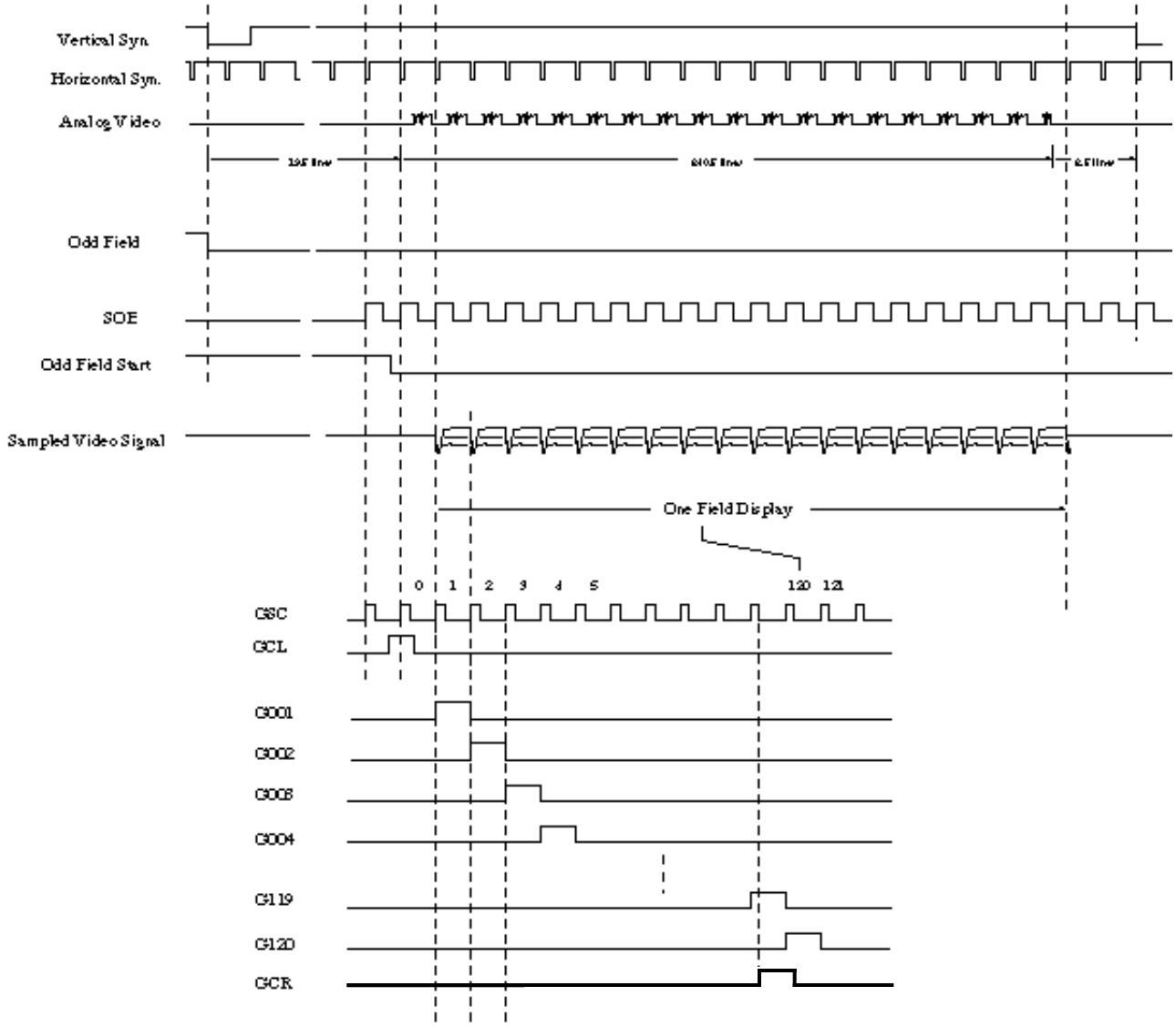
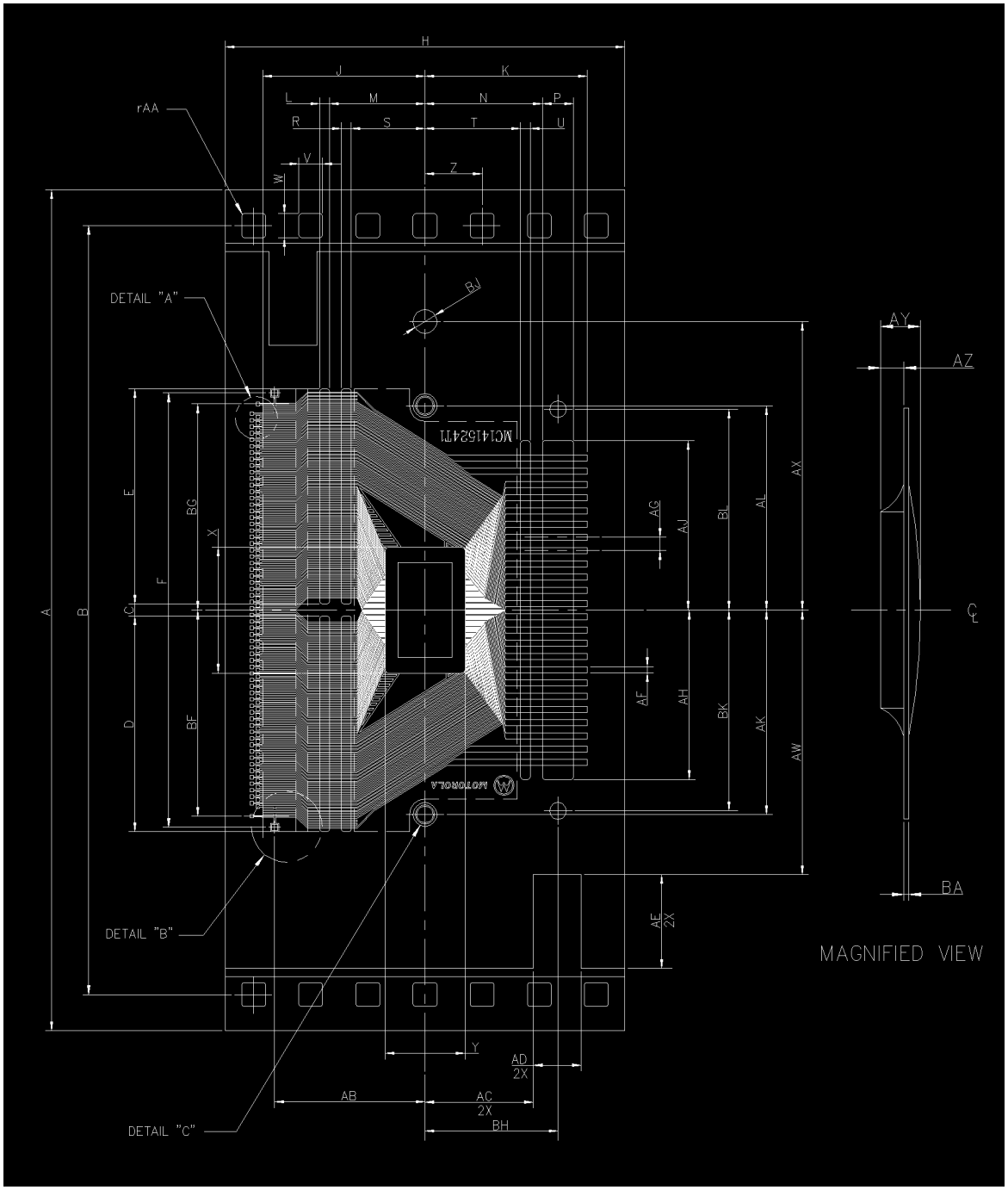


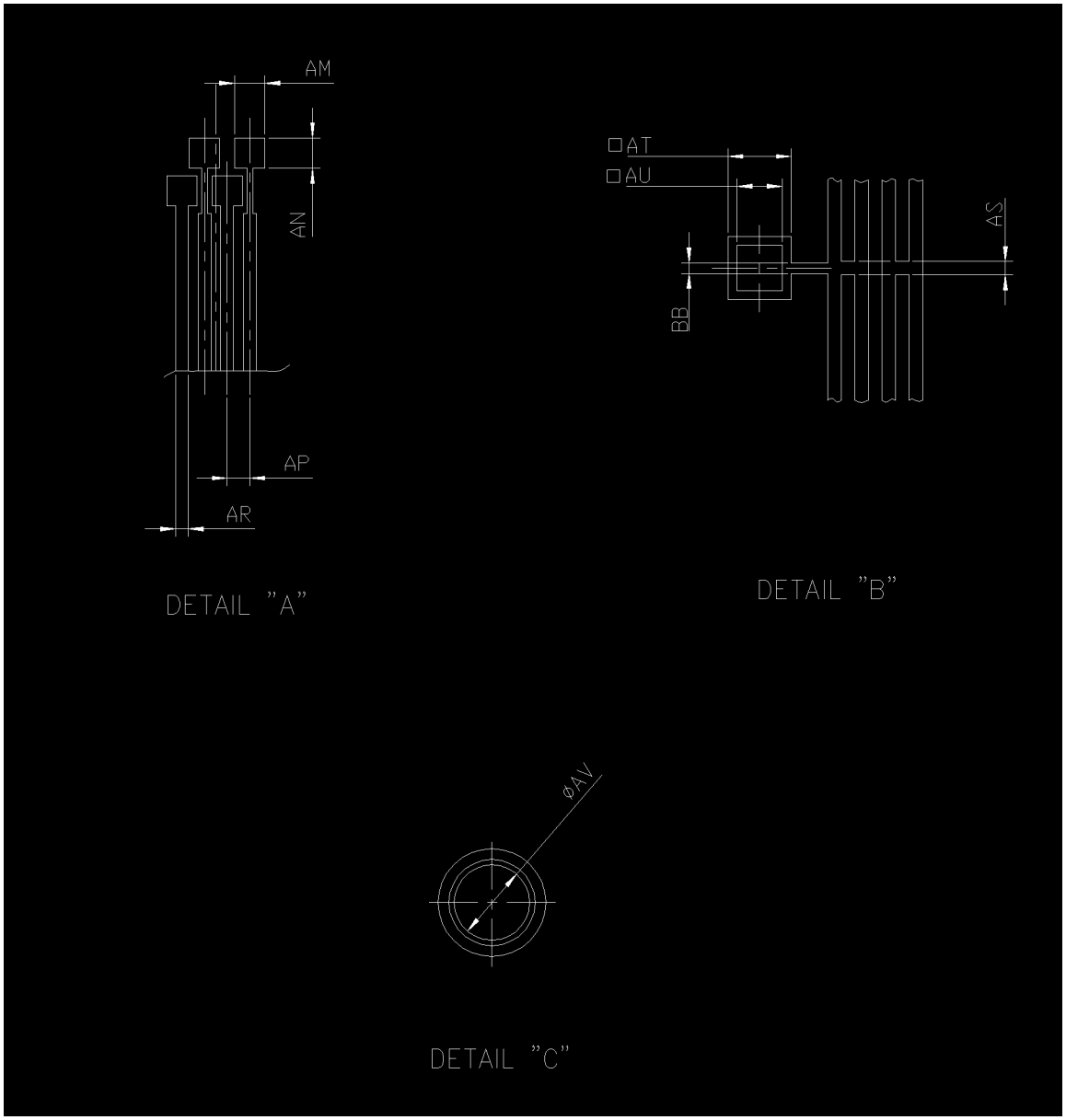
Figure 18. Source (Column) Driver and Gate (Row) Driver Timing Relation

MC141524T1
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



Reference: 98ASL00211A	Issue “0” released on 03/20/96

MC141524T1
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



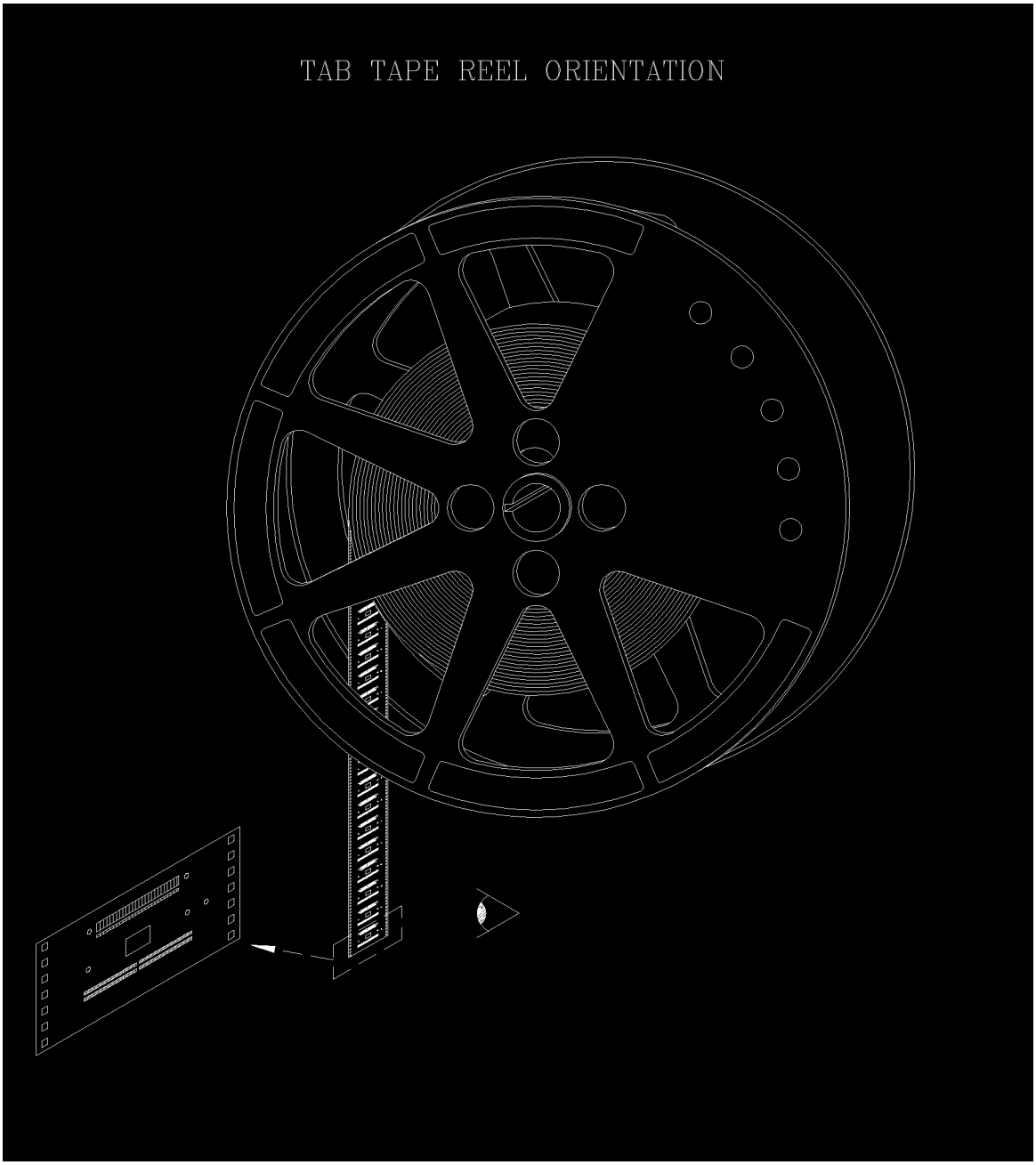
Reference: 98ASL00211A	Issue “0” released on 03/20/96

TAB PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	**Min**	**Max**	**Min**	**Max**	**Dim**	**Min**	**Max**	**Min**	**Max**
A	69.750	70.150	2.7461	2.7618	AG	1.090	1.110	0.0429	0.0437
B	63.869	64.029	2.5145	2.5208	AH	14.050	14.115	0.5531	0.5571
C	0.950	1.050	0.0374	0.0413	AJ	14.050	14.115	0.5531	0.5571
D	17.870	17.970	0.7035	0.7075	AK	16.950	17.050	0.6673	0.6713
E	17.870	17.970	0.7035	0.7075	AL	16.950	17.050	0.6673	0.6713
F	36.068	36.212	1.4200	1.4257	AM	0.250	0.350	0.0098	0.0138
H	32.750	33.750	1.2894	1.3287	AN	0.250	0.350	0.0098	0.0138
J	13.450	13.550	0.5295	0.5335	AP	0.260	0.280	0.0102	0.0110
K	13.450	13.550	0.5295	0.5335	AR	0.110	0.150	0.0043	0.0059
L	0.750	0.850	0.0295	0.0335	AS	0.130	0.170	0.0051	0.0067
M	7.900	8.000	0.3110	0.3150	AT	0.680	0.720	0.0268	0.0283
N	9.700	9.800	0.3819	0.3858	AU	0.480	0.520	0.0189	0.0205
P	2.550	2.650	0.1004	0.1043	AV	1.350	1.450	0.0531	0.0571
R	0.750	0.850	0.0295	0.0335	AW	21.500	22.500	0.8465	0.8858
S	6.100	6.200	0.2402	0.2441	AX	23.500	24.500	0.9252	0.9646
T	7.900	8.000	0.3110	0.3150	AY	0.686	0.838	0.0270	0.0330
U	0.750	0.850	0.0295	0.0335	AZ	0.5794	0.6294	0.0228	0.0248
V	1.951	2.011	0.0768	0.0792	BA	0.0675	0.0825	0.0027	0.0032
W	1.951	2.011	0.0768	0.0792	BB	0.080	0.120	0.0031	0.0047
X	-	10.490	-	0.4130	BF	17.111	17.179	0.6737	0.6764
Y	-	6.651	-	0.2619	BG	17.111	17.179	0.6737	0.6764
Z	4.720	4.780	0.1858	0.1882	BH	10.550	11.550	0.4154	0.4547
AA	-	0.200	-	0.0079	BJ	1.950	2.050	0.0768	0.0807
AB	12.450	12.550	0.4902	0.4941	BK	16.650	16.750	0.6555	0.6594
AC	8.500	9.500	0.3347	0.3740	BL	16.650	16.750	0.6555	0.6594
AD	3.500	4.500	0.1378	0.1772					
AE	7.300	8.300	0.2874	0.3268					
AF	0.480	0.520	0.0189	0.0205					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper thickness: 1oz.

Reference: 98ASL00211A Issue “0” released on 03/20/96



Reference: 98ASL00211A	Issue “0” released on 03/20/96