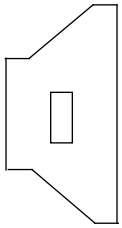
MC141522

Gate (Row) Driver for TFT Type LCD Panel
CMOS



MC141522T1
TAB

ORDERING INFORMATION

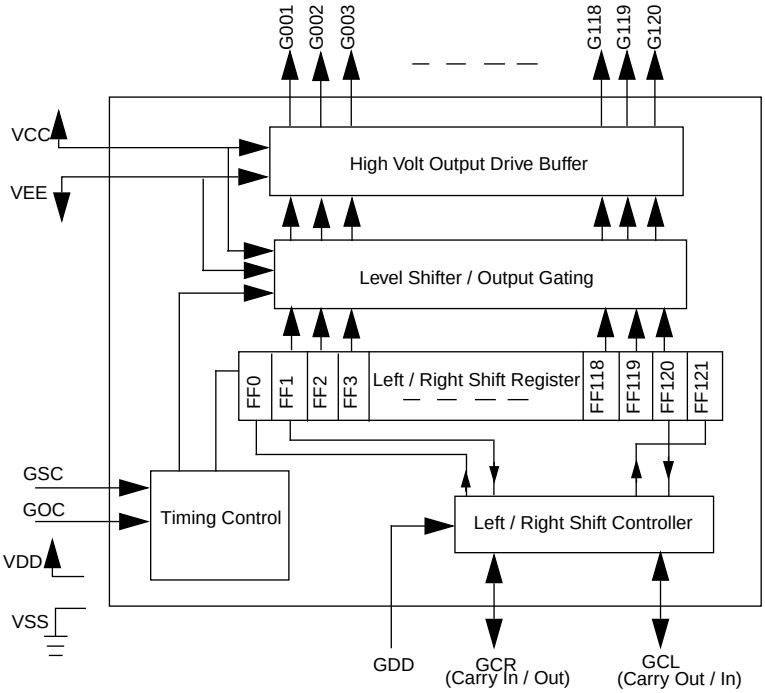
MC141522T1 TAB

The MC141522 is a high voltage LCD gate driver. It is a low power silicon-gate CMOS LCD driver chip which consists of 120 channels gate drive to provide the row gating function of a TFT (Thin-Film-Transistor) LCD panel.

This chip consists of the low voltage and high voltage part. The low voltage part includes the 122 stages of shift register, level shifter, left/right shift controller. The high voltage part consists of 120 stages level shifters and high voltage output driver buffer with 35 volts output swing capability.

The MC141522 will provide the best performance in combination with the MC141524 (source driver). The two devices can drive LCD panels from 480 x 240 pixels middle-resolution up to 720 x 480 pixels high-resolution by cascading.

- Operating Supply Voltage Range
  Logic (V_{DD} pin): 4.5V to 5.5V
  Output Drive (V_{CC} - V_{EE}) = 20.0V to 35.0V
- Operating Temperature Range: -30 to 85 C
- 120 - Row Output Driver
- Split Power Supply
- Output Pulse Width Modulation Control
- Bi-directional Shift Register
- Left / Right Shift Mode Selection
- Maximum Clock Frequency = 100KHz
- Cascadable
- Available in TAB (Tape Automated Bonding), 141 pins



BLOCK DIAGRAM

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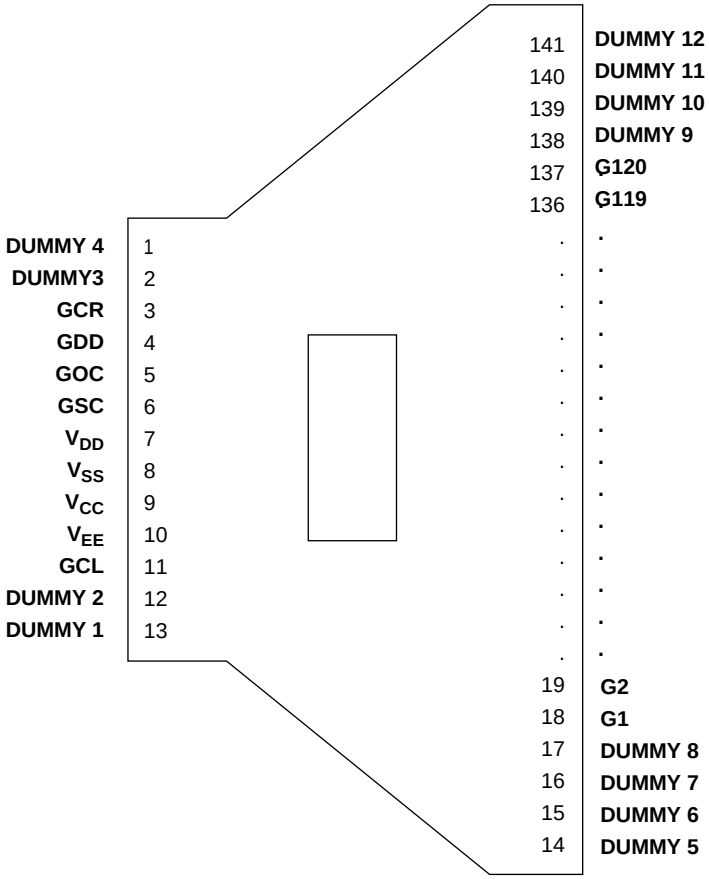


Figure 1A. TAB Package Contact Assignment (Copper View)

ABSOLUTE MAXIMUM RATING (Voltage Referenced to VSS)

Rating	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+7.0 to +17.0	V
Negative Supply Voltage	V_{EE}	-33.0 to - 23.0	V
Logic Supply Voltage	V_{DD}	-0.3 to +6.0	V
DC Supply Voltage	V_{CC} - V_{EE}	+40	V
Logic Input Voltage	V_{in}	V_{SS} - 0.5 to V_{DD} + 0.5	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	Id	10	mA
Operating Temp. Range	T_a	-30 to 85	^oC
Storage Temp. Range	T_{stg}	-55 to +150	^oC

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

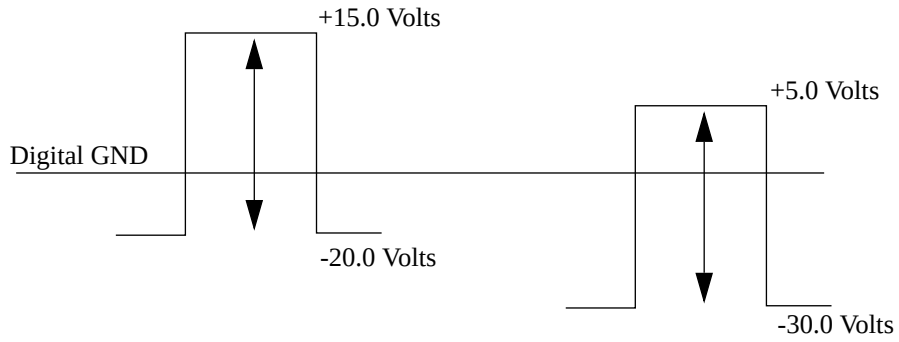
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	+5.0	+12.0	+15.0	V
Negative Supply Voltage	V_{EE}	-10.0	-12.0	-30.0	V
Logic Supply Voltage	V_{DD}	+4.5	+5.0	+5.5	V
DC Supply Voltage	V_{CC} - V_{EE}	20	25	35	V
Operating Temperature	T_a	-20	--	+75	^oC

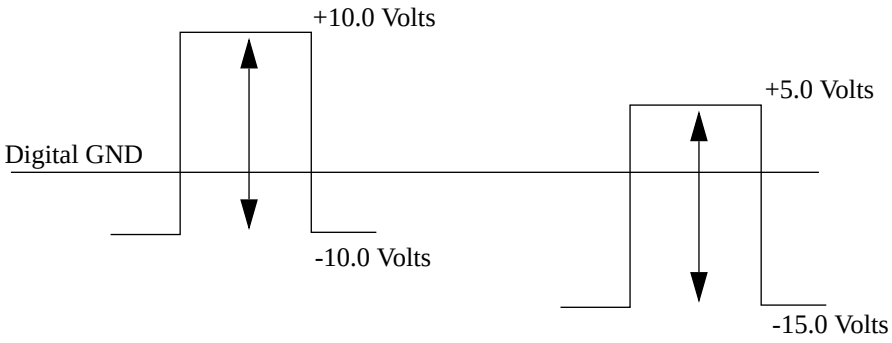
AC ELECTRICAL CHARACTERISTICS

V_{DD}=+5.0 V, V_{SS}=0 V, V_{CC}=+15.0 V, V_{EE}=-20 V, T_A=25 Ç, Voltage referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
High Voltage Driver Output					
Rise Time	tr1	--	--	1.0	us
Fall Time	tf1	--	--	1.0	us
(C_{load}=200pF)					
High Voltage Driver Output					
Rise Time	tr2	--	--	2.5	us
Fall Time	tf2	--	--	2.5	us
(Loading=5K in series with 150pF)					
Propagation Delay Time					
(Carry output from GSC)					
Low to High	tplhc	--	150	250	ns
High to Low	tphlc	--	150	250	ns
Maximum Clock Frequency (GSC)	ø Max	--	15.75	100	KHz

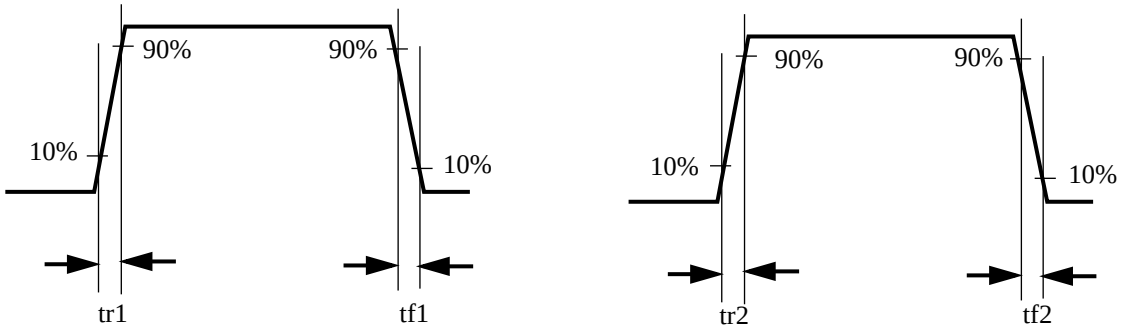


35.0 Volts Range



20.0 Volts Range

Figure 2. High Voltage Output Buffer Voltage Range



Loading Capacitance = 200pF

Loading = 5K in series with 150pF

Figure 3. High Voltage Buffer Output Rise and Fall Time

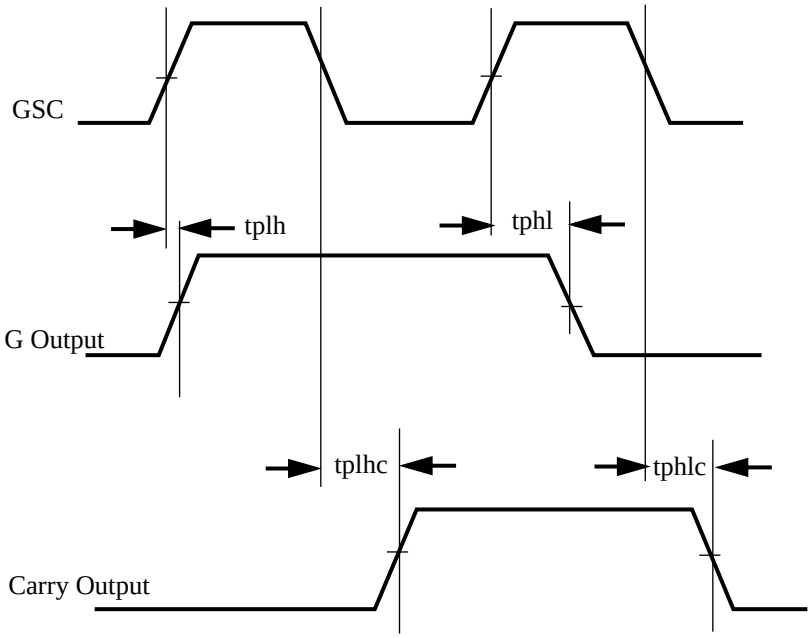


Figure 4. Shift Clock, Gate Driver Output and Carry Output Propagation Delay Timing

DC ELECTRICAL CHARACTERISTICS

V_{DD}=+5.0 V, V_{SS}=0, V_{CC}=+15.0 V, V_{EE}=-20V, T_A =25^{o}C, Voltage referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
Control Input Voltage High	V_{IH}	3.2	--	5.5	V
Control Input Voltage Low	V_{IL}	0.0	--	1.2	V
Input Leakage Current					
V_{in} = 0.5V	I_{IL}	-50	--	+50	uA
V_{in} = 3.0V	I_{IH}	-50	--	+50	uA
Driver Output Voltage (G001 - G120)					
High	V_{OH}	V_{CC}-0.8	--	--	V
Low	V_{OL}	--	--	V_{EE}+0.8	V
Supply Current					
(GSC running at 100kHZ, no loading)	I_{CC}	--	0.5	2.0	mA
	I_{DD}	--	100	200	uA
	I_{EE}	-2.0	0.5	--	mA

PIN DESCRIPTION

V_{SS}
This is the power supply GND connection pin.

V_{DD}
This is the positive 5 V power supply pin for the logic circuitry of the chip.

V_{CC}
This is the power supply pin for the most positive supply voltage.

V_{EE}
This is the power supply pin for the most negative supply voltage.

GSC (Gate Driver Shift Clock)
This input clock signal is to clock the Carry In input ripple through the 122 Stages Shift Register for controlling the Output Scan Gating Sequence.

For normal single scan, the clock frequency is the horizontal frequency of the TV signal. In double scan full resolution mode, the frequency is doubled.

GCL (Gate Driver Carry-Left) / GCR (Carry-Right)
These two input / output pins perform the same function and depends on the GDD (Shift Direction Determination) Operation. In Shift Right mode, the GCL is the Carry input while the GCR is the Carry output for cascading. In shift Left mode, the pin functions and operations are vice versa. See Table 1.

GDD	Shift Direction		GCL	GCR
“0”	G001 to G120	Shift Right Mode	Input	Output
“1”	G120 to G001	Shift Left Mode	Output	Input

Table 1.Carry Shift Direction

GDD (Gate Driver Shift Direction Determination)
This input pin provides the selection of the shift left and right mode of operation.

GDD = “0”, the system shift register will shift right.

GDD = “1”, the system shift register will shift left.

See Table 1.

GOC (Gate Driver Output Control)
This input pin provides control to the output buffer output pulse width in order to provide the effective gating timing of the TFT.

G001 to G120
These 120 output pins are high voltage buffer for driving the gate of the TFT active matrix LCD panel.

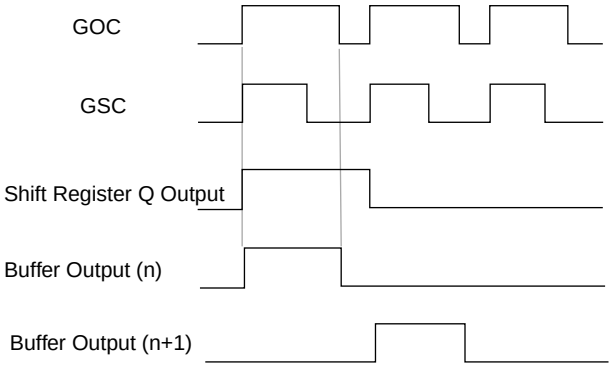


Figure 5. Gate Output Control to Control the Gating Pulse Width

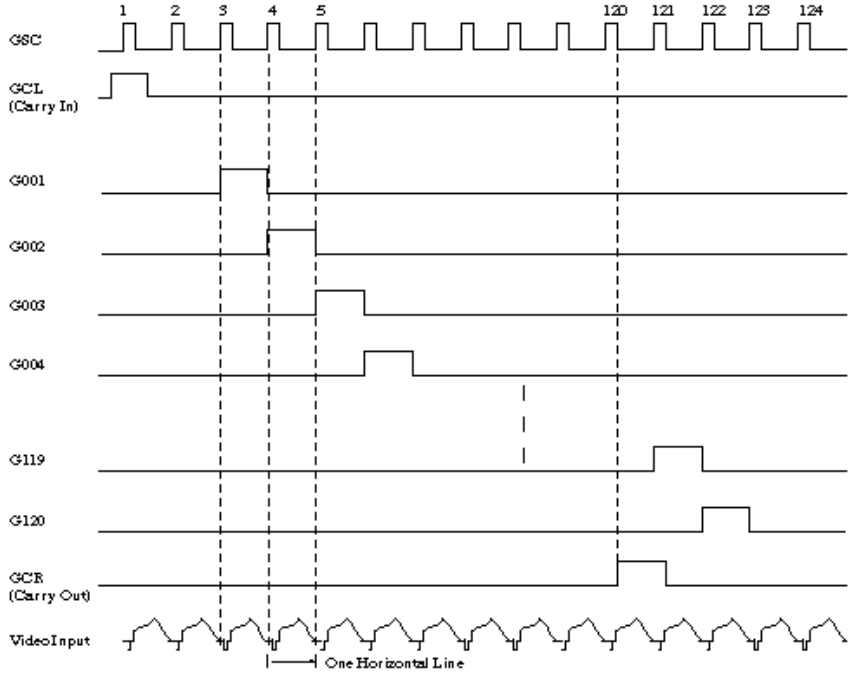


Figure 6. Row Driver Timing Diagram (Shift Right Mode)

MC141522T1

TAB PACKAGE DIMEMSION

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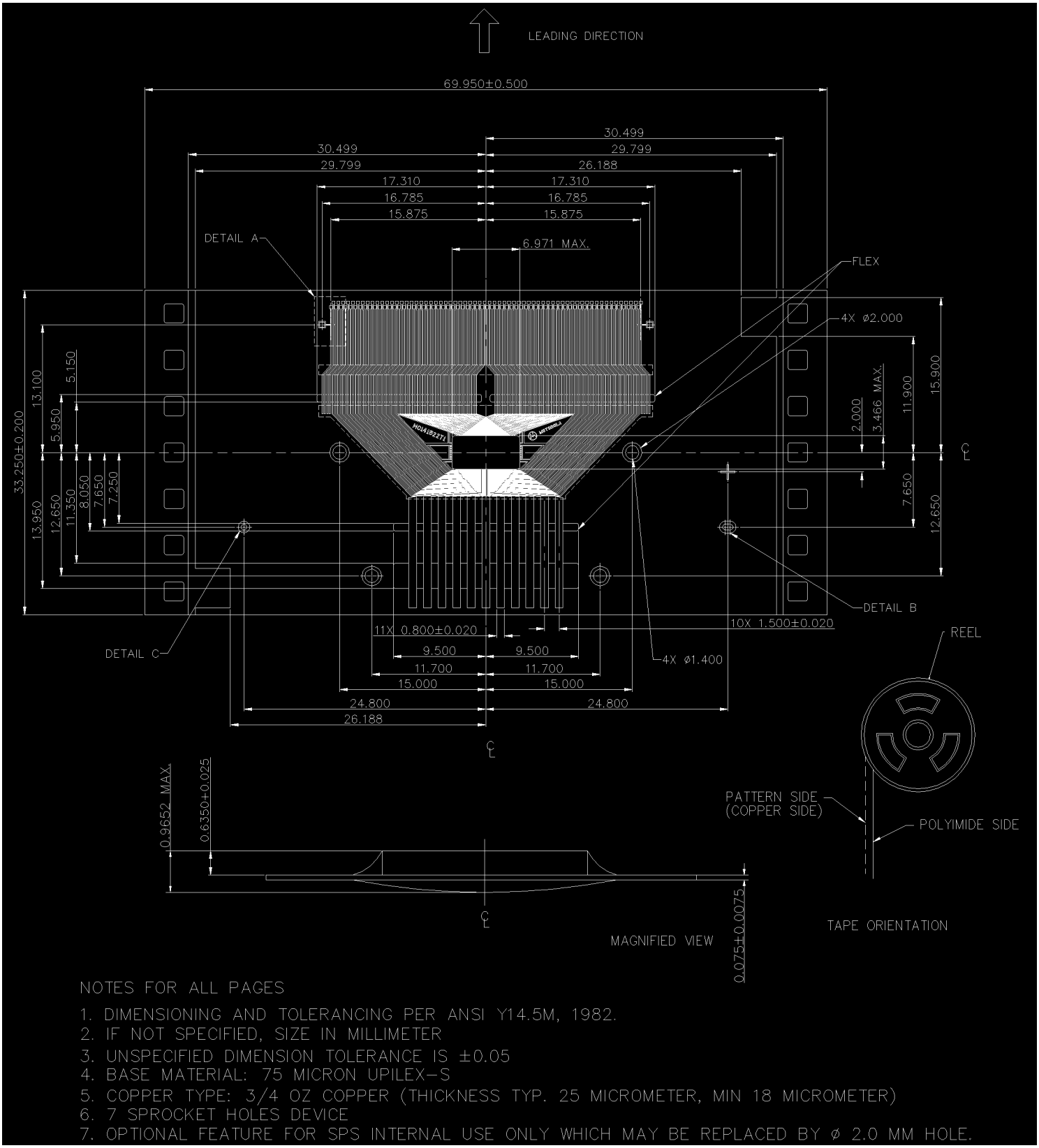

NOTES FOR ALL PAGES

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX–S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. 7 SPROCKET HOLES DEVICE
7. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ø 2.0 MM HOLE.

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TAB PACKAGE DIMEMSION
(DO NOT SCALE THIS DRAWING)