

LCD Backplane Drivers CMOS

The MC141512 and MC141515 are high voltage passive LCD backplane driver chips. The MC141512 provides 80 high voltage LCD driving signals whereas the MC141515 provides 160 high voltage LCD driving signals.

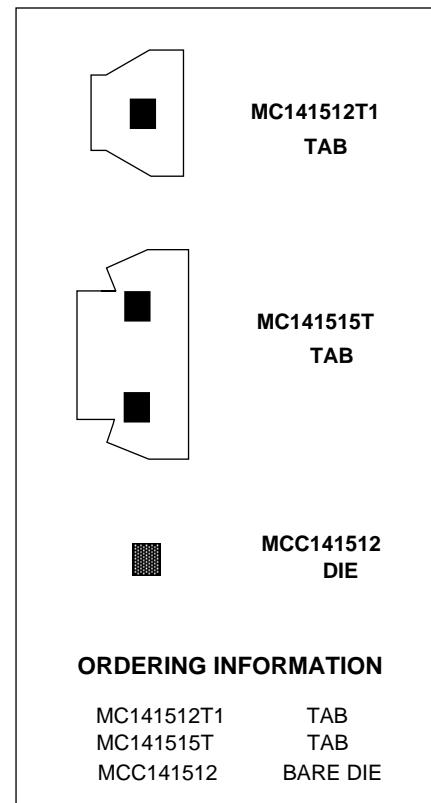
They are companion chips to the MC141514 and MC141519 LCD segment driver for medium size LCD panels. All these chips are controlled by the MC68HC05L11 microcomputer.

The MC141515T is the twin die version of the MC141512T.

See Application Note AN-HK-15.

- Operating Supply Voltage Range -
 - Control Logic (V_{DD} Pin): 2.7V to 5.5V
 - Backplane Drivers (V_{LCD} Pin): 10V to 25V
- Operating Temperature Range: -25 to 70°C
- Direct Serial Data Interface with the MC68HC05L11
- MC141512 - 80 LCD Backplane Driving Signals
- MC141515 - 160 LCD Backplane Driving Signals
- 1:5 to 1:13 Bias
- Expansion to Higher Driver Count by Cascade
- Available in Three Forms:
 - TAB (Tape Automated Bonding), 91 Contacts - MC141512T1
 - 182 Contacts - MC141515T
 - Die Form Without Gold Bumps, 91 Pads with 4.3 mil Pads Pitch

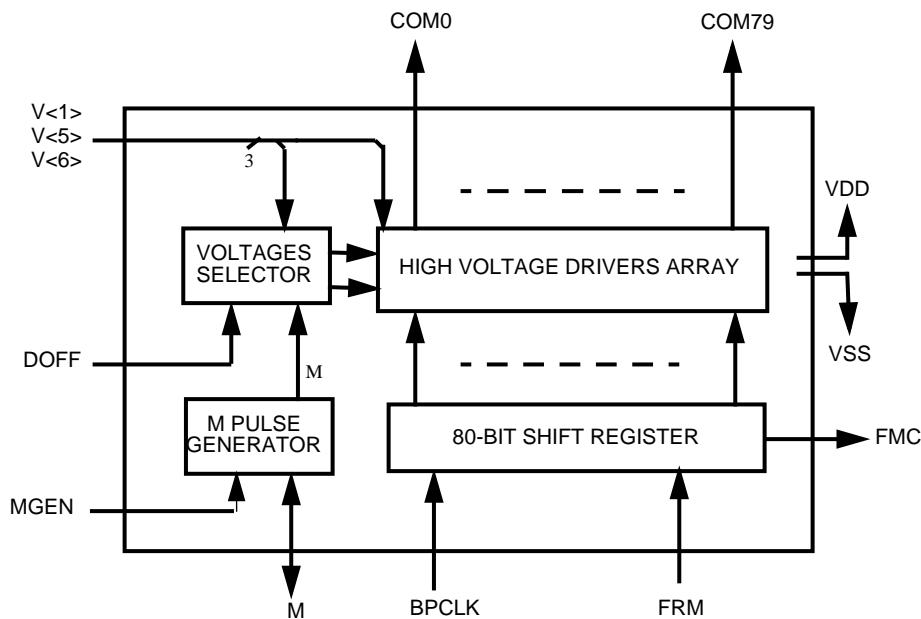
MC141512
MC141515

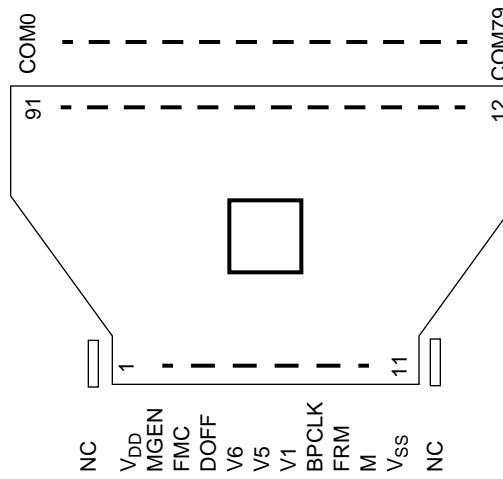


ORDERING INFORMATION

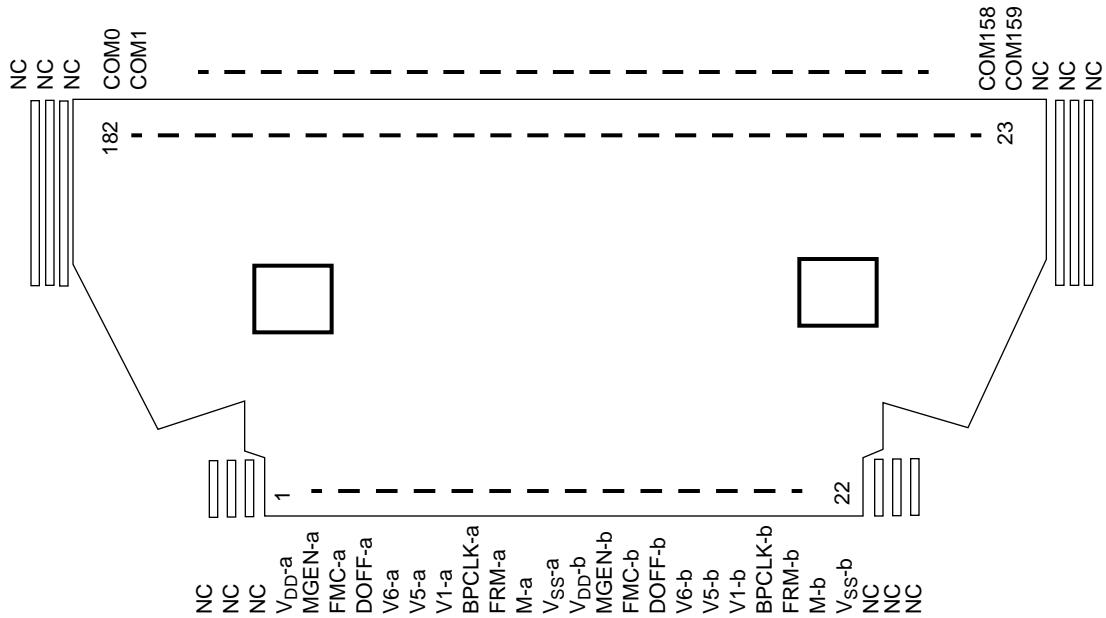
MC141512T1	TAB
MC141515T	TAB
MCC141512	BARE DIE

BLOCK DIAGRAM

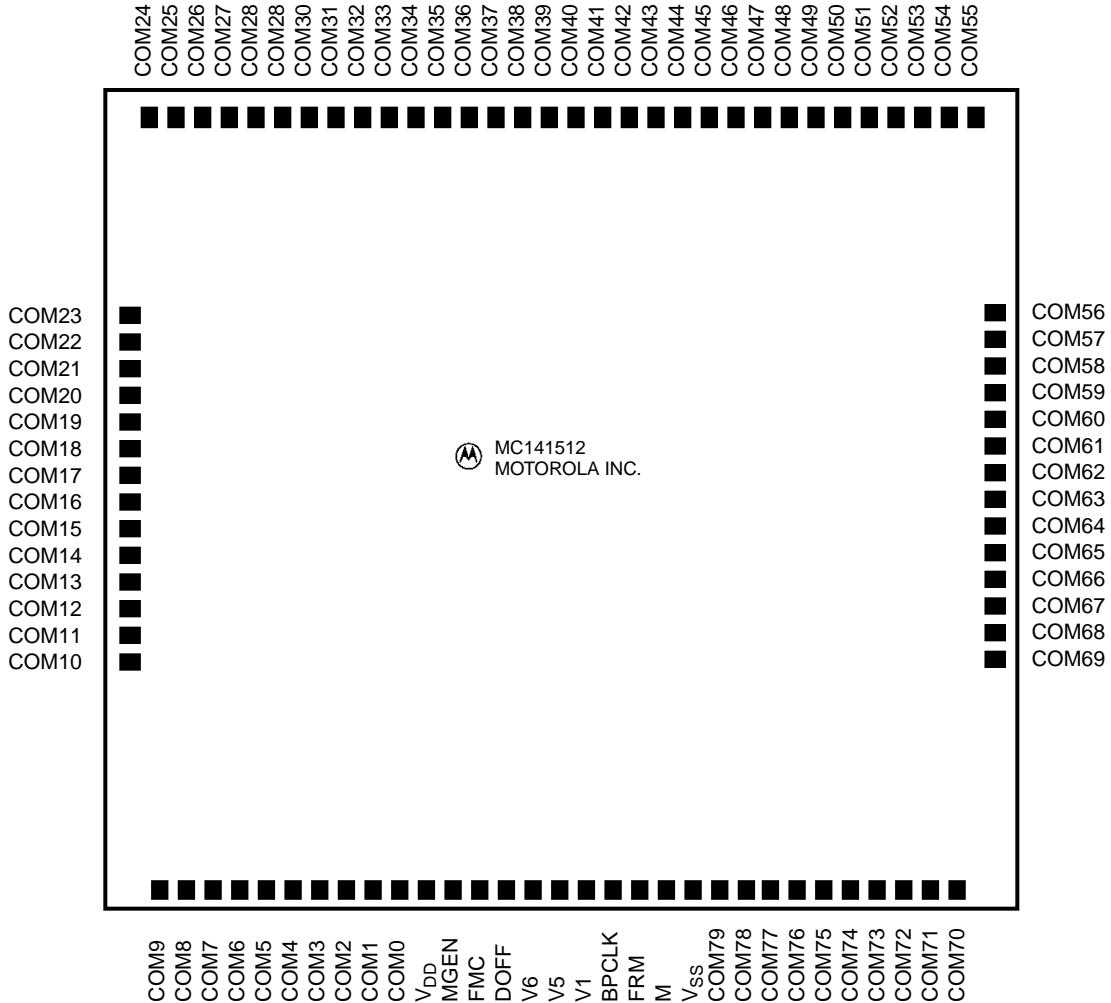




MC141512T1 TAB Package Contact Assignment (Copper View)



MC141515T TAB Package Contact Assignment (Copper View)



Chip Pad Assignment

MAXIMUM RATINGS*(Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	Supply Voltage	-0.3 to +7.0	V
V _{<1>}		-0.3 to +27.5	V
V _{in}	Input Voltage	-0.3 to V _{DD} +0.3	V
I	Current Drain Per Pin Excluding V _{DD} and V _{SS}	25	mA
T _A	Operating Temperature	-25 to +75	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

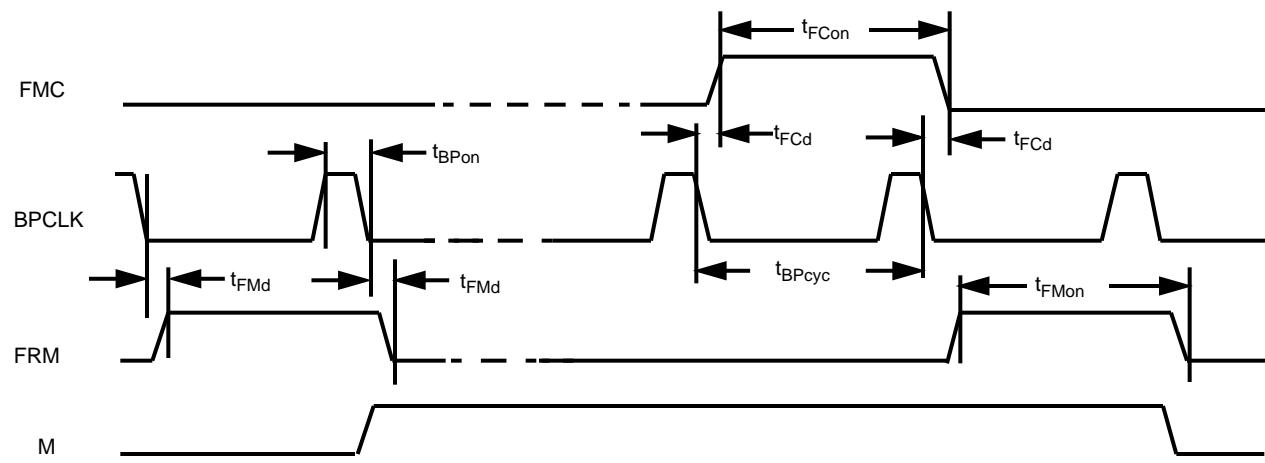
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD} = 5.0V, V_{<1>} = 25V, T_A = -25 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{DD} V _{<1>}	Supply Voltage Range LCD Supply Voltage Range	(Absolute value reference to V _{SS})	2.7 +10.0	- -	5.5 +25.0	V V
I _{DP}	Display Mode Supply Current (V _{DD} Pin)	BPCLK = 8KHz	-	1	10	uA
I _{SB}	Standby Mode Supply Current (V _{DD} Pin)	Using D _{ON} bit of the MCU	-	0.5	1	uA
I _{LDP}	Display Mode Supply Current (V _{<1>} Pin)	BPCLK = 8KHz	-	3	10	uA
I _{LSB}	Standby Mode Supply Current (V _{<1>} Pin)	BPCLK = 8KHz	-	0.5	1	uA
V _{OL} V _{OH}	Output Low Voltage Output High Voltage (M, FMC)	No Load	V _{SS} 0.8 x V _{DD}	- -	0.2 x V _{DD} V _{DD}	V V
V _{IH} V _{IL}	Input High Voltage Input Low Voltage (BPCLK, FRM, M, DOFF, FMC, MGEN)		0.7xV _{DD} V _{SS}	- -	V _{DD} 0.3xV _{DD}	V V
I _{in}	Input Current (BPCLK, FRM, M, DOFF, FMC, MGEN)		-	-	1	uA
C _{in}	Input Capacitance (BPCLK, FRM, M, DOFF, FMC)		-	-	8	pF
I _{OH} I _{OL}	Output High Current Output Low Current (M, FMC)	V _{OH} = 4.5V V _{OL} = 0.5V	+100 -	- -	- -100	uA uA

AC ELECTRICAL CHARACTERISTICS ($V_{DD} = 2.7 - 5.0V$, $V_{SS} = 0V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Max	Unit
t_{FCon}	Carry Out Frame On Time	122	-	us
t_{FCd}	Carry Out Frame Delay Time	10	100	ns
t_{BPon}	BPCLK Pulse On Time	61	-	us
t_{BPCyc}	BPCLK Cycle Period	61	-	us
t_{FMd}	Frame Delay Time	10	100	ns
t_{FMon}	Frame Pulse On Time	122	-	us



Timing Diagram

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

Power is supplied to the driver using these two pins. V_{DD} is power and V_{SS} is ground.

V<1>, V<5>, V<6>

These are the levels of voltage generated from an external voltages divider (Fig. 1).

DOFF

This is an output from MC68HC05L11 to signal the backplane driver to turn off LCD. If this signal is clear, the backplane driver will supply LCD with driving signal. If this signal is set, the backplane driver outputs will be high-impedanced and LCD display is disabled.

FRM

A periodic active high input to the backplane driver for frame timing synchronization which is connected to FRM of MC68HC05L11.

BPCLK

A periodic output from MC68HC05L11 to backplane driver for timing synchronization. The signal will affect the refreshing time of LCD display.

FMC

This is an output pin of backplane driver which is connected to the FRM of the next backplane driver in case of cascading.

M

This pin is for synchronization between the display driver. When MGEN is set, it will generate an M signal for synchronization. When MGEN is clear, it becomes an input pin and expecting a M signal from other device.

MGEN

An input which is used for program the M pin as an input or output. If MGEN is logic high, M acts as an output. If MGEN is logic low, M becomes an input.

COM 0 - 79

These are the high voltage outputs of the backplane driver which are connected to set of common lines of any LCD panel.

OPERATION OF LCD DRIVER

INTRODUCTION

The LCD backplane driver can support multiplex ratio of a LCD system up to 146 and cascading of more than one driver for expansion is possible. It can be set from 1:5 bias (for 16 mux) to 1:13 bias (for 146 mux), by the voltage divider ratio of Fig.1. The ratio of bias or the contrast ratio (a) is defined as

$$1 : \frac{4 \times R_1 + R_2}{R_1} = 1 : a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a = \frac{1}{\text{mux}} + 1$$

To set up a multiplex ratio, please refer to MC68HC05L11 technical data Section 10.6.2.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from external voltage divider. (See Fig. 1).

80-BIT SHIFT REGISTER samples the FRM at the falling edge of BPCLK and shifts the sample to the left 80 times before exports to the next backplane driver through FMC.

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as Com(1) and Com(2) are shown in Figure 2.

POWER UP SYNCHRONIZATION is activated upon the receipt the first M pulse. The M pin of the backplane driver will act as an input when MGEN is connected to Low. When MGEN is Set, this backplane driver will be the master of the synchronization system. M pin will then supply a periodic signal for all LCD drivers.

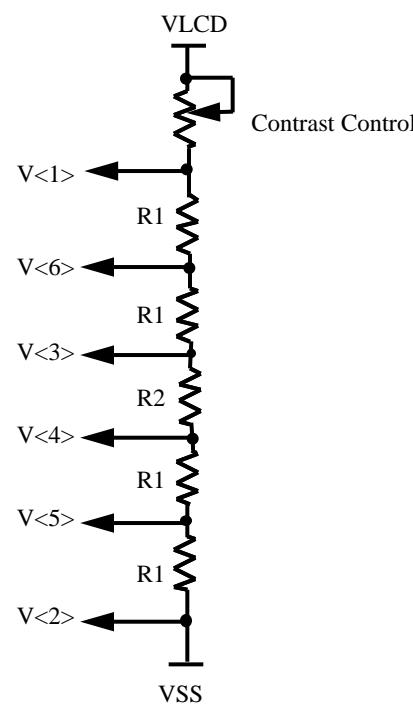


Figure 1. External Voltage Divider

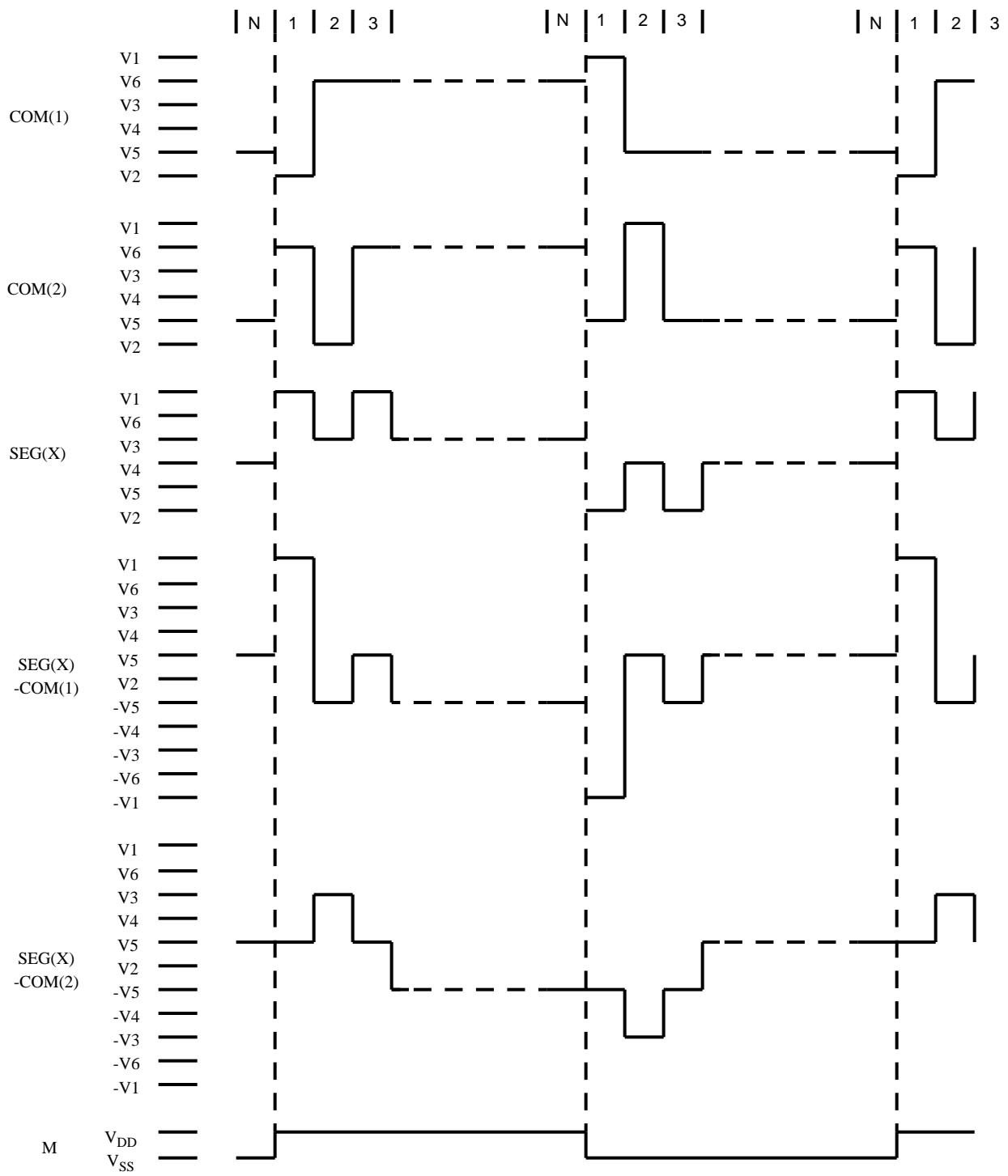
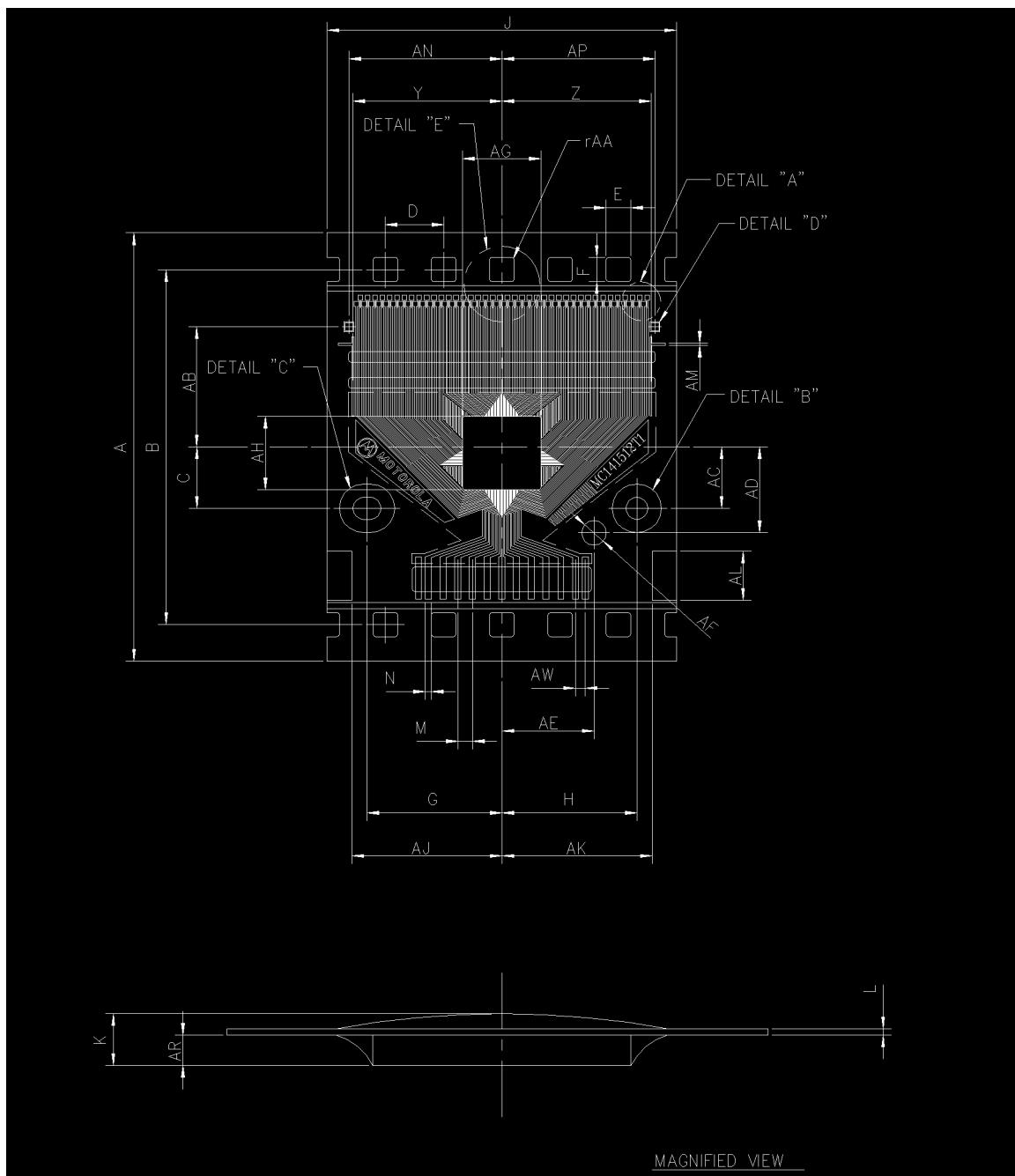


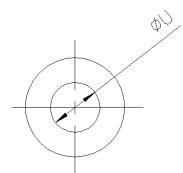
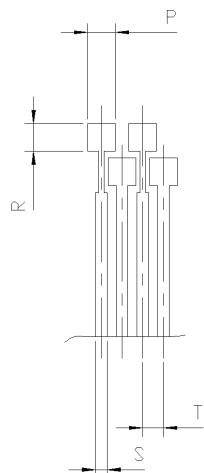
Figure 2. Driving Waveforms of 1:N Multiplex Ratio

PACKAGE DIMENSIONS

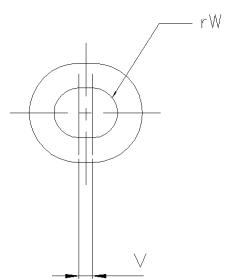
MC141512T1
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



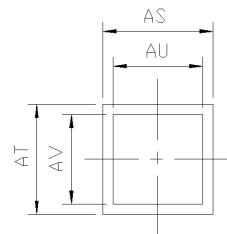
MC141512T1
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



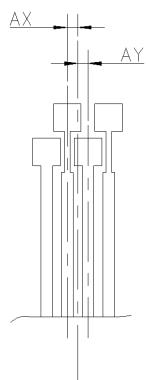
DETAIL "A"



DETAIL "C"



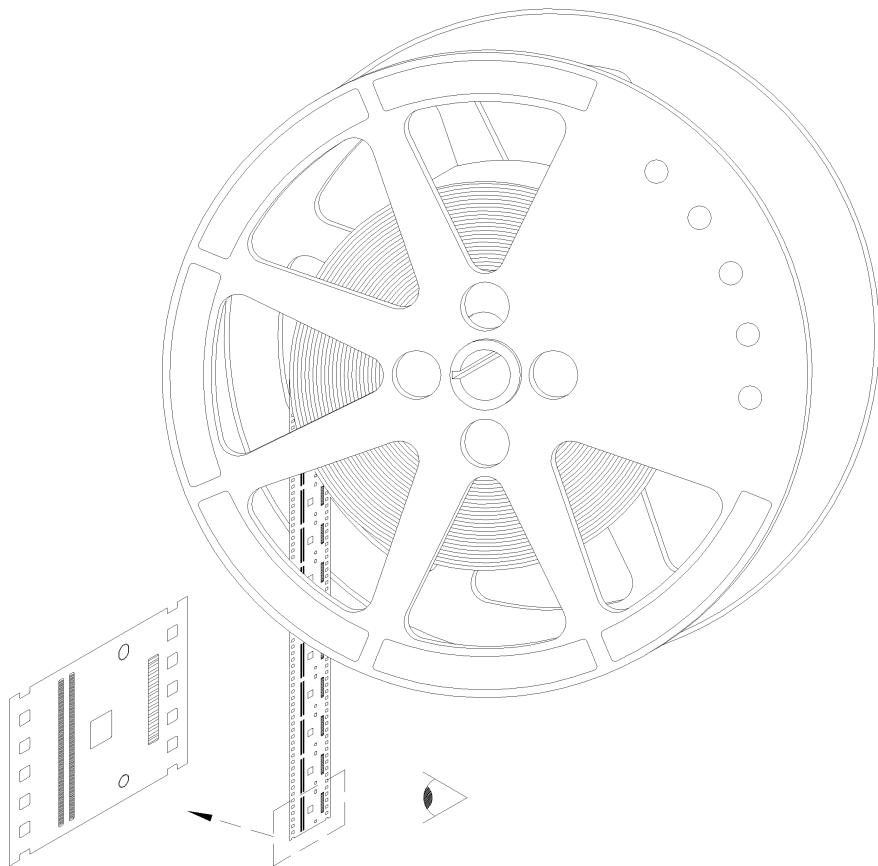
DETAIL "D"



DETAIL "E"

MC141512T1

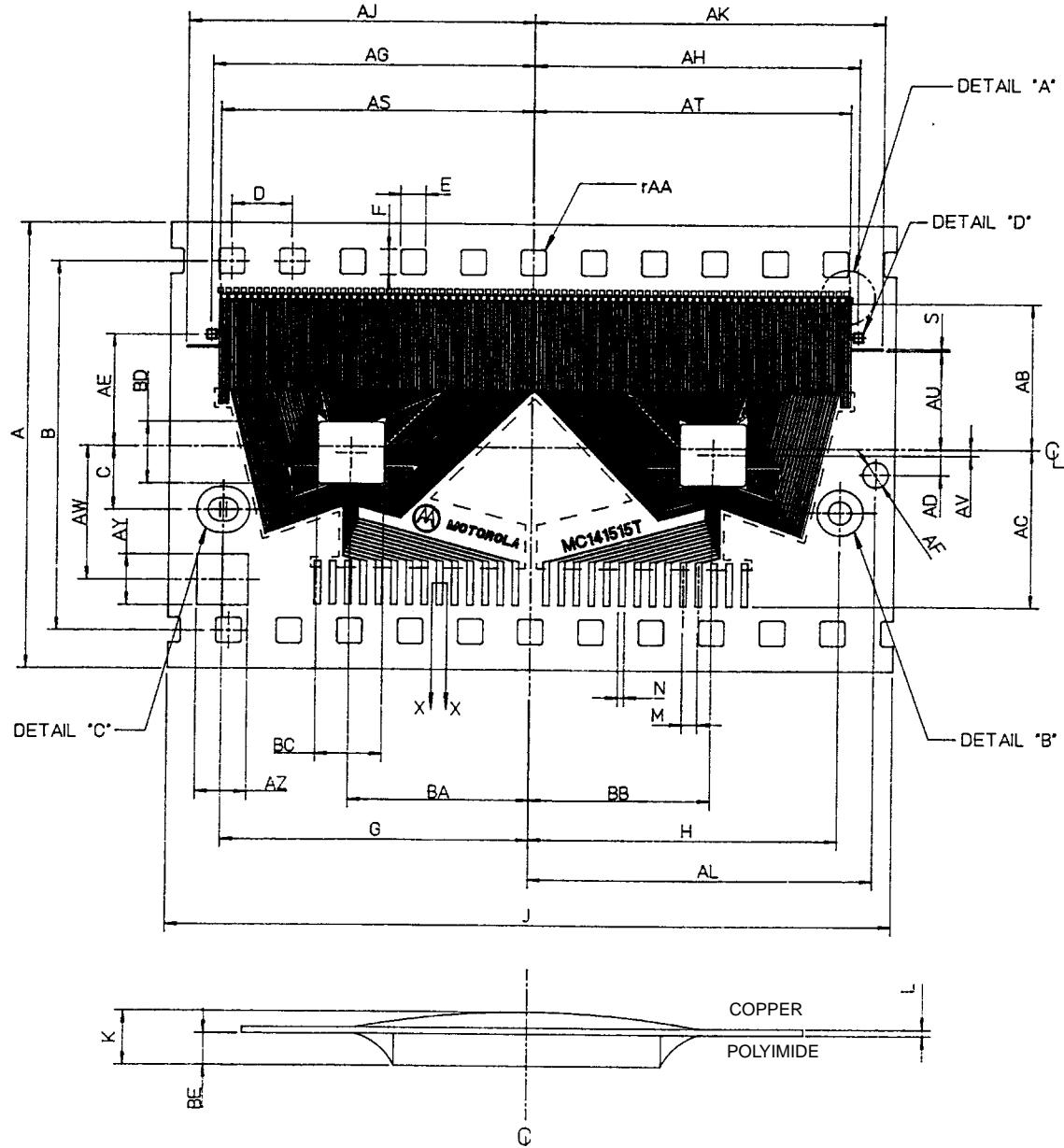
TAB TAPE REEL ORIENTATION



Reference: 98ASL00103A

Issue "A" released on 03/21/94

MC141515T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



MAGNIFIED VIEW

MC141515T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)

