

MC14106B

Hex Schmitt Trigger

The MC14106B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Increased Hysteresis Voltage Over the MC14584B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace the MC14584B or MC14069UB

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	− 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	− 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	− 65 to + 150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

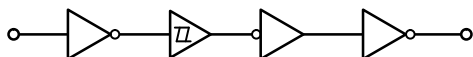
* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

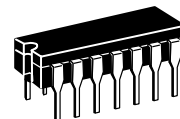
Ceramic "L" Packages: − 12 mW/°C From 100°C To 125°C

EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)

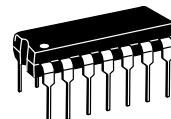


This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP

Plastic

MC14XXXBCL

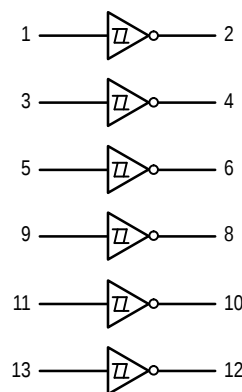
Ceramic

MC14XXXBD

SOIC

T_A = − 55° to 125°C for all packages.

LOGIC DIAGRAM



V_{DD} = PIN 14

V_{SS} = PIN 7



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ “0” Level “1” Level $V_{in} = 0$	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Hysteresis Voltage	$V_H^\dagger$	5.0 10 15	0.3 1.2 1.6	2.0 3.4 5.0	0.3 1.2 1.6	1.1 1.7 2.1	2.0 3.4 5.0	0.3 1.2 1.6	2.0 3.4 5.0	Vdc
Threshold Voltage Positive–Going	V_{T+}	5.0 10 15	2.2 4.6 6.8	3.6 7.1 10.8	2.2 4.6 6.8	2.9 5.9 8.8	3.6 7.1 10.8	2.2 4.6 6.8	3.6 7.1 10.8	Vdc
Negative–Going	V_{T-}	5.0 10 15	0.9 2.5 4.0	2.8 5.2 7.4	0.9 2.5 4.0	1.9 3.9 5.8	2.8 5.2 7.4	0.9 2.5 4.0	2.8 5.2 7.4	Vdc
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	Source I_{OH}	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
	Sink I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μ Adc
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μ Adc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0 10 15	$I_T = (1.8 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (3.6 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (5.4 \mu\text{A/kHz}) f + I_{DD}$							μ Adc

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.001$.

† $V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than $V_{T+ \text{ max}} - V_{T- \text{ min}}$).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise Time	t _{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time	t _{PLH} , t _{PHL}	5.0 10 15	— — —	125 50 40	250 100 80	ns

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

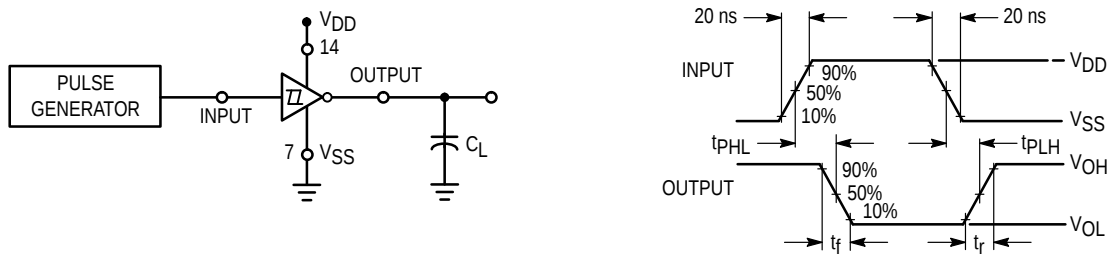


Figure 1. Switching Time Test Circuit and Waveforms

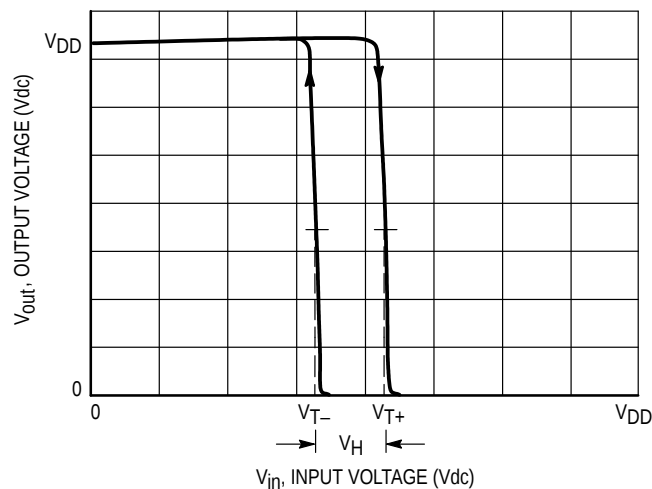


Figure 2. Typical Transfer Characteristics

APPLICATIONS

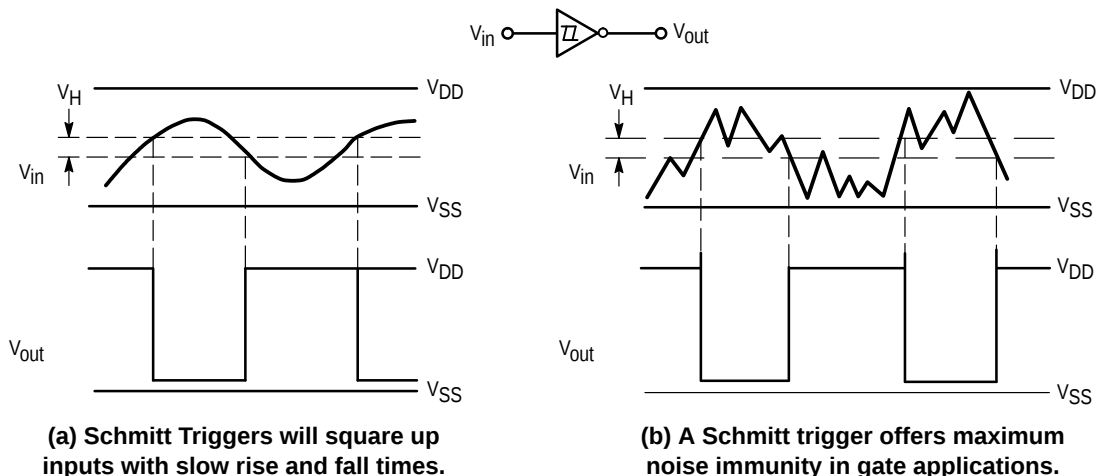
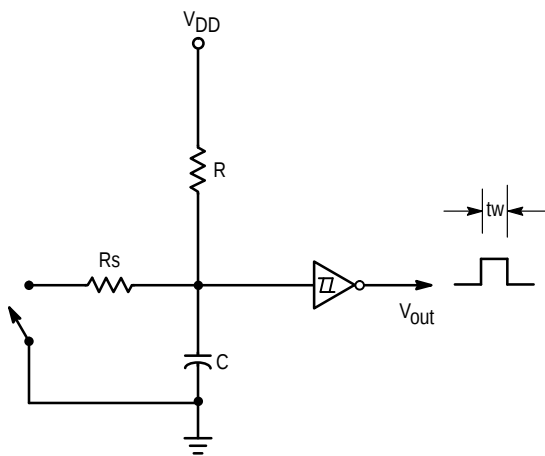
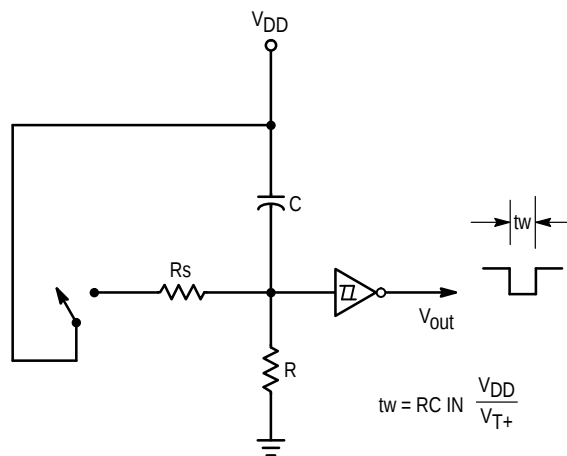


Figure 3.

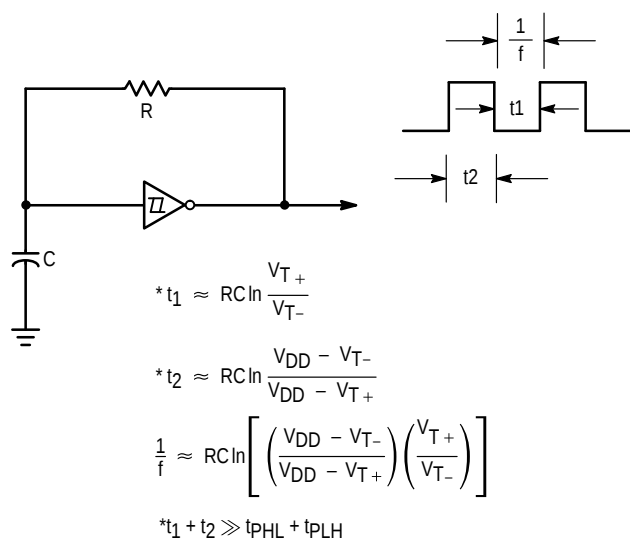


Useful as Pushbutton/Keyboard Debounce Circuit.

Figure 4. Monostable Multivibrator



$$tw = RC \ln \frac{V_{DD}}{V_{T+}}$$



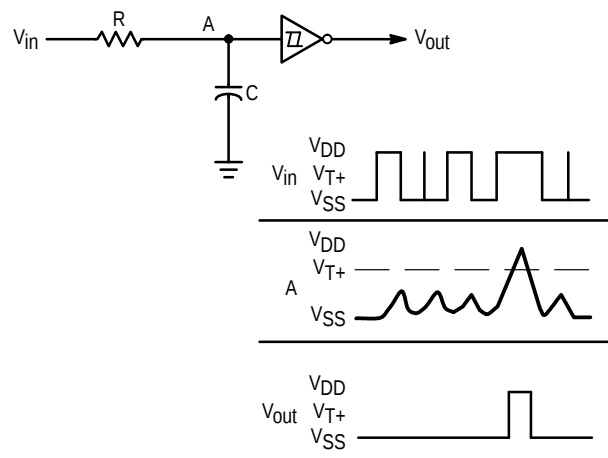
$$*t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$*t_2 \approx RC \ln \frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}$$

$$\frac{1}{f} \approx RC \ln \left[\left(\frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}} \right) \left(\frac{V_{T+}}{V_{T-}} \right) \right]$$

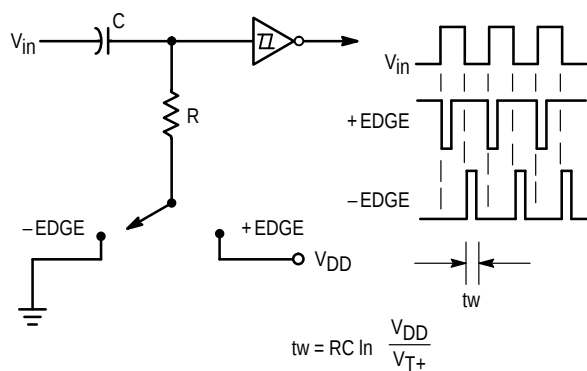
$$*t_1 + t_2 \gg t_{PHL} + t_{PLH}$$

Figure 5. Astable Multivibrator



Useful in discriminating against short pulse durations.

Figure 6. Integrator



$$tw = RC \ln \frac{V_{DD}}{V_{T+}}$$

Useful as an edge detector circuit.

Figure 7. Differentiator

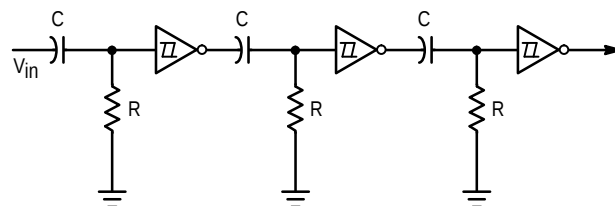
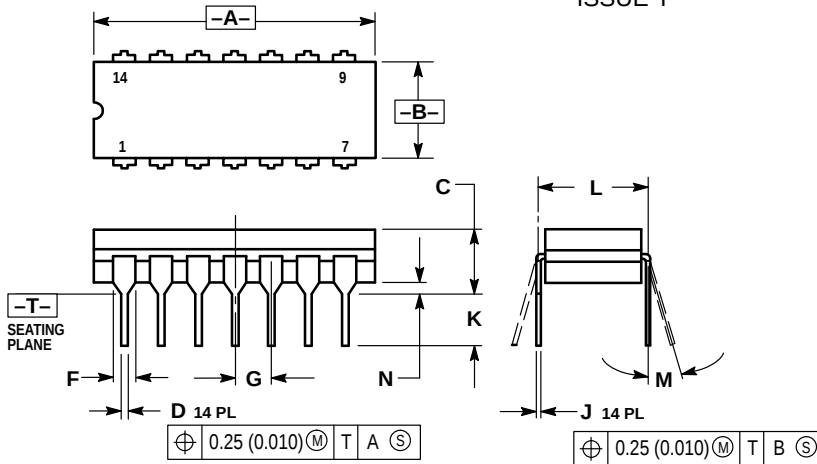


Figure 8. Positive Edge Time Delay Circuit

OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 632-08 ISSUE Y

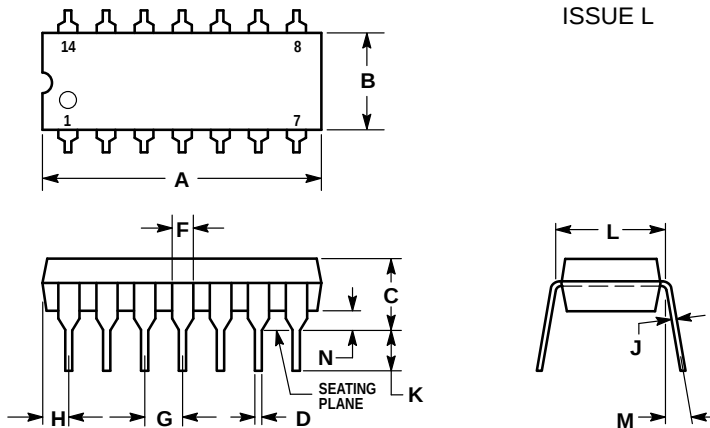


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 646-06 ISSUE L



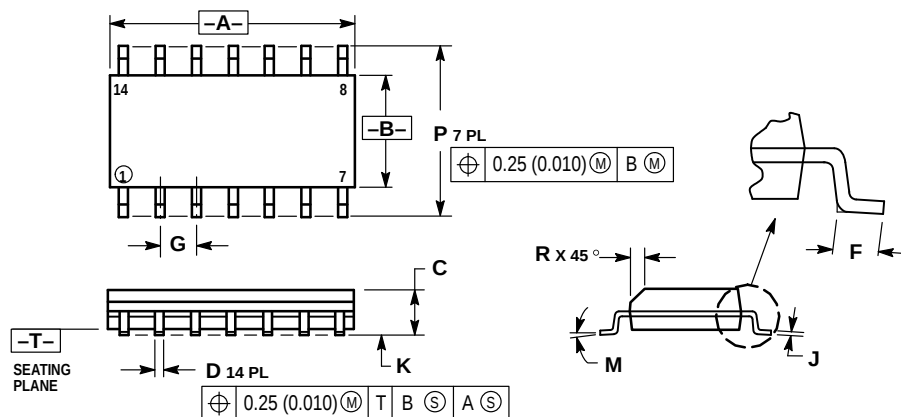
NOTES:

1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



MOTOROLA



MC14106B/D

