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MOTOROLA

Universal Cordless Telephone Subsystem IC with Scrambler

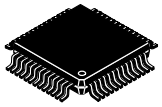
MC13110

UNIVERSAL CT–1 SUBSYSTEM INTEGRATED CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

The MC13110 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with New External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Frequency Inversion Scrambler/Descrambler
  - Can Be Enabled/Disabled Via MPU Interface
  - Programmable Carrier Modulation Frequency
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices
- AN1575: Refer to this Application Note for a List of the “Worldwide Cordless Telephone Frequencies” (List can also be found in Chapter 8 Addendum of DL128 Data Book)

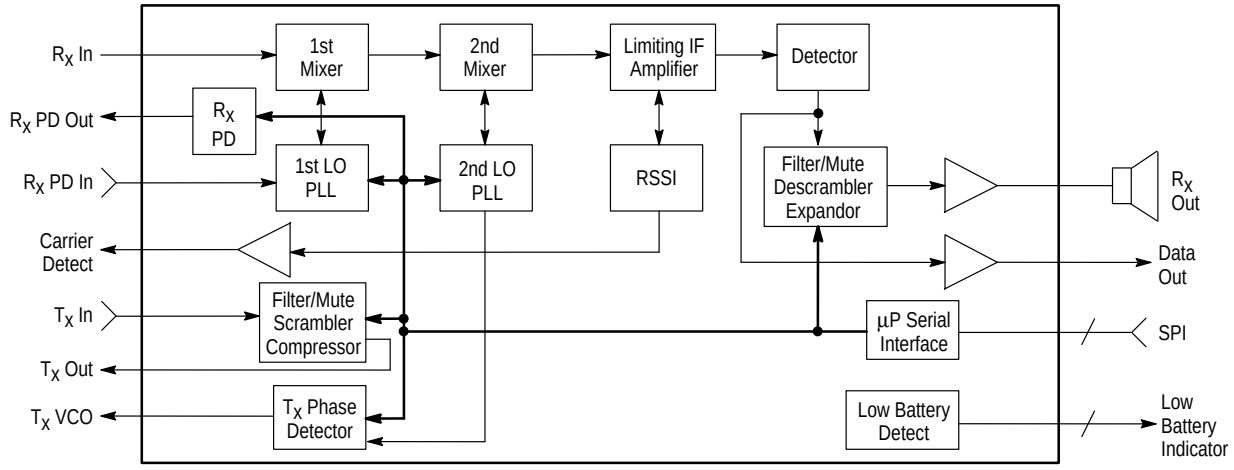


FB SUFFIX
PLASTIC QFP PACKAGE
CASE 848B

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC13110FB	T_A = – 40° to +85°C	QFP–52

Simplified Application



This device contains 8,262 active transistors.

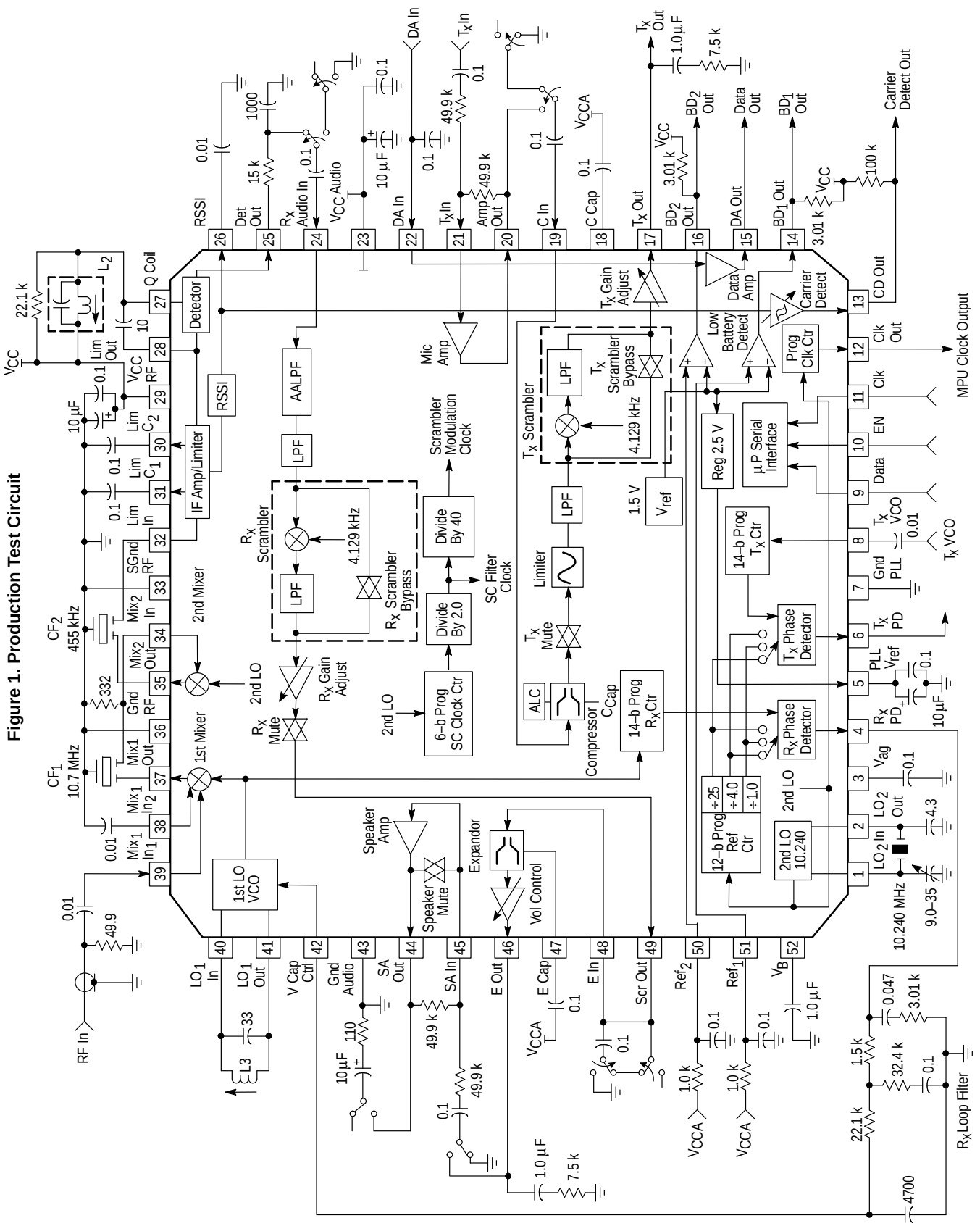


Figure 1. Production Test Circuit

NOTE: This schematic is only a representation of the actual production test circuit.

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +5.5	Vdc
Junction Temperature	T_J	–65 to +150	°C

NOTES: 1. Devices should not be operated at these limits. The "Recommended Operating Conditions" provide for actual device operation.

2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.6	5.0	Vdc
Operating Ambient Temperature	T_A	–40	–	85	°C
Input Voltage Low (Data, Clk, EN)	V_{IL}	–	–	0.3	V
Input Voltage High (Data, Clk, EN)	V_{IH}	2.5	–	–	V
Output Current (R_X PD, T_X PD) High Low	 I_{OH} I_{OL}	 – 0.7	 – –	 –0.7 –	mA

NOTE: All limits are not necessarily functional concurrently.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, T_A = 25°C, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Static Current					
Active Mode (2.7 V)	ACT I_{CC}	–	8.1	–	mA
Active Mode	ACT I_{CC}	–	8.6	12	mA
Receive Mode	R_X I_{CC}	–	4.3	5.3	mA
Standby Mode	STD I_{CC}	–	270	500	µA
Inactive Mode	INACT I_{CC}	–	35	80	µA

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
PLL VOLTAGE REGULATOR								
Regulated Output Level	I_L = 0 mA	–	PLL V_{ref}	V_O	2.4	2.5	2.6	V
Line Regulation	I_L = 0 mA, V_{CC} = 3.6 to 5.5 V	V_{CC} Audio	PLL V_{ref}	V_{Reg} Line	–	–0.6	20	mV
Load Regulation	V_{CC} = 3.6 V, I_L = 1.0 mA	V_{CC} Audio	PLL V_{ref}	V_{Reg} Load	–	–1.1	20	mV
PLL LOOP CHARACTERISTICS								
2nd LO Frequency (No Crystal)	–	LO_2 In	–	f_{2ext}	–	12	–	MHz
2nd LO Frequency (With Crystal)	–	–	LO_2 In LO_2 Out	f_{2ext}	–	12	–	MHz
T_X VCO (Input Frequency)	V_{in} = 200 mVpp	–	T_X VCO	f_{txmax}	–	80	–	MHz

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
PLL PHASE DETECTOR								
Output Voltage Low	I_{IL} = 0.7 mA	–	R_X PD T_X PD	V_{OL}	–	–	(PLL V_{ref}) *.2	V
Output Voltage High	I_{IH} = –0.7 mA	–	R_X PD T_X PD	V_{OL}	(PLL V_{ref}) *.8	–	–	V
3–State Leakage Current	V = 1.2 V	–	R_X PD T_X PD	I_{OZ}	–50	–	50	nA
Output Capacitance	–	–	R_X PD T_X PD	C_{out}	–	8.0	–	pF
Output Rise and Fall Time	C_{Load} = 50 pF	–	R_X PD T_X PD Clk Out	t_r, t_f	–	250	–	ns
MICROPROCESSOR SERIAL INTERFACE								
Input Current Low	V_{in} = 0.3 V Standby Mode	–	Data, Clk, EN	I_{IL}	–5.0	0.3	–	µA
Input Current High	V_{in} = 3.3 V Standby Mode	–	Data, Clk, EN	I_{IH}	–	1.5	5.0	µA
Hysteresis Voltage	–	–	Data, Clk, EN	V_{hys}	–	1.0	–	V
Maximum Clock Frequency	–	Data, EN, Clk	–	–	–	2.0	–	MHz
Input Capacitance	–	Data, Clk, EN	–	C_{in}	–	8.0	–	pF
EN to Clk Setup Time	–	–	EN, Clk	t_{suEC}	–	200	–	ns
Data to Clk Setup Time	–	–	Data, Clk	t_{suDC}	–	100	–	ns
Hold Time	–	–	Data, Clk	t_h	–	90	–	ns
Recovery Time	–	–	EN, Clk	t_{rec}	–	90	–	ns
Input Pulse Width	–	–	EN, Clk	t_w	–	100	–	ns
Input Rise and Fall Time	–	–	Data, Clk, EN	t_r, t_f	–	9.0	–	µs
MPU Interface Power–Up Delay	90% of PLL V_{ref} to Data, Clk, EN	–	–	t_{puMPU}	–	100	–	µs
FM RECEIVER (f_{RF} = 46.77 MHz [USA Ch 21], f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz)								
Sensitivity (Input for 12 dB SINAD)	50 Ω Termination	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	– –	2.8 –98	– –	µVrms dBm
	Single–Ended, Matched Input	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	– –	1.0 –107	– –	µVrms dBm
	Differential, Matched Input	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	– –	.56 –112	– –	µVrms dBm
1st Mixer Voltage Conversion Gain	V_{in} = 1.0 mVrms, with CF_1 Filter as Load	Mix_1 $In_{1/2}$	Mix_1 Out	MX_{gain1}	–	12	–	dB
2nd Mixer Voltage Conversion Gain	V_{in} = 3.0 mVrms, with CF_2 Filter as Load	Mix_2 In	Mix_2 Out	MX_{gain2}	–	20	–	dB
1st and 2nd Mixer Voltage Gain Total	V_{in} = 1.0 mVrms, with CF_1 and CF_2 Load	Mix_1 $In_{1/2}$	Mix_2 Out	MX_{gainT}	24	28	–	dB
1st Mixer Input Impedance	Single–Ended Input	–	Mix_1 $In_{1/2}$	R_{P1} C_{P1}	– –	875 2.7	– –	Ω pF
2nd Mixer Input Impedance	f_{in} = 10.7 MHz	–	Mix_2 In	Z_{in2}	–	3.0	–	kΩ

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
FM RECEIVER (f_{RF} = 46.77 MHz [USA Ch 21], f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz)								
1st Mixer Output Impedancet	–	–	Mix_1 Out	Z_{out1}	–	330	–	Ω
2nd Mixer Output Impedance	–	–	Mix_2 Out	Z_{out2}	–	1.5	–	kΩ
IF –3.0 dB Limiting Sensitivity	f_{in} = 455 kHz	Lim In	Det Out	IF Sens	–	71	100	μVrms
Total Harmonic Distortion	With R_C = 15 k/1.0 nF Filter at Det Out	Mix_1 In_1	Det Out	THD	–	1.3	2.0	%
Recovered Audio	V_{in} = 3.16 mVrms with R_C = 15 k/1000 pF Filter at Det Out	Mix_1 In_1	Det Out	AFO	80	105	150	mVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
Signal to Noise Ratio	V_{in} = 3.16 mVrms, R_C = 15 k/1000 pF	Mix_1 In_1	Det Out	SN	–	49	–	dB
AM Rejection Ratio	V_{in} = 3.16 mVrms, 30% AM, @ 1.0 kHz, R_C = 15 k/1000 pF	Mix_1 In_1	Det Out	AMR	30	47	–	dB
1st Mixer, 1.0 dB Voltage Compression (Input Pin Referred)	–	Mix_1 $In_{1/2}$	Mix_1 Out	V_O 1.0 dB Mix_1	–	15	–	mVrms
2nd Mixer, 1.0 dB Voltage Compression (Input Pin Referred)	50 Ω Input	Mix_2 In	Mix_2 Out	V_O 1.0 dB Mix_2	–	14	–	mVrms
1st Mixer 3rd Order Intercept (Input Pin Referred)	V_{in} = 3.98 mVrms	Mix_1 In_1	Mix_1 Out	TOI_{mix1}	–	56	–	mVrms
2nd Mixer 3rd Order Intercept (Input Pin Referred)	V_{in} = 3.98 mVrms, 50 Ω Input	Mix_2 In	Mix_2 Out	TOI_{mix2}	–	53	–	mVrms
Detector Output Impedance	–	–	Det Out	Z_O	–	870	–	Ω
RSSI/CARRIER DETECT (R_L = 100 kΩ)								
RSSI Output Current Dynamic Range	–	Mix_1 In	RSSI	RSSI	–	80	–	dB
Carrier Sense Threshold	CD Threshold Adjust = (10100)	Mix_1 In	CD Out	V_T	–	33	–	μVrms
Hysteresis	–	Mix1 In	CD Out	Hys	–	3.6	7.0	dB
Output High Voltage	V_{in} = 0 Vrms, CD = (10100)	Mix_1 In	CD Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage	V_{in} = –80 dBV, CD = (10100)	Mix_1 In	CD Out	V_{OL}	–	0.02	0.4	V

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI/CARRIER DETECT (R_L = 100 kΩ)								
Carrier Sense Threshold Adjustment Range	Programmable through MPU Interface	–	–	$V_{T\ low\ range}$	–20	–	–	dB
		–	–	$V_{T\ hi\ range}$	–	–	11	
Carrier Sense Threshold – Number of Steps	Programmable through MPU Interface	–	–	V_{Tn}	–	32	–	–
DATA AMP COMPARATOR								
Hysteresis	–	DA In	DA Out	Hys	30	40	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	2.7	V_{CC} – 0.7	–	V
Input Impedance	–	–	DA In	Z_I	–	11	–	kΩ
Output Impedance	–	–	DA Out	Z_O	–	100	–	kΩ
Output High Voltage	V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	DA In	DA Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage	V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	DA In	DA Out	V_{OL}	–	0.04	0.4	V
EXPANDOR/R_X MUTE (f_{in} = 1.0 kHz)								
Absolute Gain	V_{in} = –20 dBV	E In	E Out	G	–3.0	0	3.0	dB
Gain Tracking	V_{in} = –30 dBV V_{in} = –40 dBV	E In	E Out	G_t	–21 –42	–20 –40	–19 –38	dB
Total Harmonic Distortion	V_{in} = –20 dBV	E In	E Out	THD	–	0.5	1.0	%
Maximum Input Voltage	–	R_X Audio In	–	–	–	–11.5	–	dBV
Maximum Output Voltage	Increase input voltage until output voltage THD = 5.0%, then measure output voltage. R_L = 7.5 k/1.0 µF	E In	E Out	V_{Omax}	–	0	–	dBV
Input Impedance	–	R_X Audio In E In	–	Z_{in}	– –	600 7.5	– –	kΩ
Attack Time	E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	E In	E Out	t_a	–	3.0	–	ms
Release Time	E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	E In	E Out	t_r	–	13.5	–	ms
Compressor to Expandor Crosstalk	V_{in} = –10 dBV, $V_{(E\ In)}$ = AC Gnd	C In	E Out	C_T	–	–90	–70	dB
R_X Data Muting (Δ Gain)	V_{in} = –20 dBV, R_X Gain Adj = (01111)	R_X Audio In	E Out	M_e	–	–83	–60	dB
SPEAKER AMP/SP MUTE								
Maximum Output Swing	V_{in} = 0 dBV, R_L = 130 Ω	SA In	SA Out	V_{Omax}	0.8	0.9	–	Vpp
Speaker Amp Muting	V_{in} = –20 dBV	SA In	SA Out	M_{sp}	–	–90	–60	dB
COMPRESSOR/T_X MUTE (f_{in} = 1.0 kHz, Scrambler Bypass Mode, T_X Gain Adj = (01111), f_{in} = 1.0 kHz)								
Absolute Gain	V_{in} = –10 dBV	T_X In	T_X Out	G	–4.0	0	4.0	dB
Gain Tracking	V_{in} = –30 dBV V_{in} = –40 dBV	T_X In	T_X Out	G_t	–11 –17	–10 –20	–9.0 –13	dB
Total Harmonic Distortion	V_{in} = –10 dBV	T_X In	T_X Out	THD	–	0.6	1.1	%

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
COMPRESSOR/T_X MUTE (f_{in} = 1.0 kHz, Scrambler Bypass Mode, T_X Gain Adj = (01111), f_{in} = 1.0 kHz)								
Maximum Output Voltage	Increase input voltage until output voltage THD = 5.0%, then measure output voltage. R_L = 7.5 k/1.0 µF	C In	T_X Out	V_{Omax}	–	–5.0	–	dBV
Input Impedance	–	C In	T_X Out	Z_{in}	–	10	–	kΩ
Attack Time	C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	C In	T_X Out	t_a	–	3.0	–	ms
Release Time	C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	C In	T_X Out	t_r	–	13.5	–	ms
Expandor to Compressor Crosstalk	V_{in} = –20 dBV, Speaker Amp No Load, $V_{(C\ In)}$ = AC Gnd	E In	T_X Out	C_T	–	–60	–40	dB
T_X Muting	V_{in} – 10 dBV	T_X In	T_X Out	M_c	–	–90	–60	dB
ALC Output Level	V_{in} = –10 dBV V_{in} = –2.5 dBV Limiter and Mutes disabled	T_X In	T_X Out	ALC_{out}	–15 –13	–11 –10	–8.0 –6.0	dBV
Limiter Output Level	V_{in} = –2.5 dBV, ALC disabled	T_X In	T_X Out	V_{lim}	–10	–7.0	–	dBV
R_X AND T_X SCRAMBLER (2nd LO = 10.24 MHz, T_X Gain Adj = (01111), R_X Gain Adj = (01111), Volume Control = (0 dB Default Levels), SCF Clock Divider = 31. Total is divide by 62 for SCF clock frequency of 165.16 kHz)								
R_X High Frequency Corner (Note 1)	R_X Path, f = 479 Hz, V R_X Audio In = –20 dBV	R_X Audio In	Scr Out	R_X f_{ch}	–	3.65	–	kHz
T_X High Frequency Corner (Note 1)	T_X Path, f = 250 Hz, V T_X In = –10 dBV, Mic Amp = Unity Gain	T_X In	T_X Out	T_X f_{ch}	–	3.879	–	kHz
Absolute Gain	R_X: V_{in} = –20 dBV T_X: V_{in} = –10 dBV, Limiter disabled	R_X Audio In T_X In	E Out T_X Out	AV	–4.0 –4.0	0 0	4.0 4.0	dB
Pass Band Ripple	R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = low corner frequency to high corner frequency	C In	E Out	Ripple	–	2.0	–	dB
Scrambler Modulation Frequency	R_X: 100 mV (–20 dBV) T_X: 316 mV (–10 dBV)	R_X Audio In C In	E Out T_X Out	f_{mod}	4.119	4.129	4.139	kHz
Group Delay	R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = 1.0 kHz	C In	E Out	GD	–	1.0	–	ms
	f_{in} = low corner frequency to high corner frequency	C In	E Out	GD	–	4.0	–	
Carrier Breakthrough	R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In	C In	E Out	CBT	–	–60	–	dB
Baseband Breakthrough	R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = 1.0 kHz, f_{meas} = 3.192 kHz	C In	E Out	BBT	–	–50	–	dB

NOTE: 1. The filter specification is based on a 10.24 MHz 2nd LO, and a switched–capacitor (SC) filter counter divider ratio of 31. If other 2nd LO frequencies and/or SC filter counter divider ratios are used, the filter corner frequency will be proportional to the resulting SC filter clock frequency.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
MIC AMP (f_{in} = 1.0 kHz, External resistors set to gain of 1)								
Open Loop Gain	–	T_X In	Amp Out	AVOL	–	100,000	–	V/V
Gain Bandwidth	–	T_X In	Amp Out	GBW	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	T_X In	Amp Out	V_{Omax}	–	2.8	–	Vpp
LOW BATTERY DETECT								
Average Threshold Voltage Before Electronic Adjustment	V_{CC} = 3.6 V, $V_{ref_}$Adj = (0111). Take average of rising and falling threshold	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_i	1.36	1.5	1.64	V
Average Threshold Voltage After Electronic Adjustment	V_{CC} = 3.6 V, $V_{ref_}$Adj = (adjusted value). Take average of rising and falling threshold	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_f	1.475	1.5	1.525	V
Hysteresis	–	Ref_1 Ref_2	BD_1 Out BD_2 Out	Hys	–	4.0	–	mV
Input Current	V_{in} = 1.0 to 2.0 V	–	Ref_1 Ref_2	I_{in}	–50	–	50	nA
Output High Voltage	V_{in} = 2.0 V, R_L = 3.9 kΩ to V_{CC}	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage	V_{in} = 1.0 V, R_L = 3.9 kΩ to V_{CC}	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OL}	–	0.1	0.4	V

PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Description
1 2	LO_2 In LO2 Out	–	These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver. "LO_2 In" may also serve as an input for an externally generated reference signal which is typically ac–coupled.
3	V_{ag}	–	Internal reference voltage for switched capacitor filter section.
4	R_X PD	Output	Three state voltage output of the R_X Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_X PLL loop filter. It is important to minimize the line length and parasitic capacitance of this pin.
5	PLL V_{ref}	–	PLL voltage regulator output pin. An internal voltage regulator provides a stable power supply voltage for the R_X and T_X PLL's and can also be used as a regulated supply voltage for other IC's.
6	T_X PD	Output	Three state voltage output of the T_X Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external T_X PLL loop filter. It is important to minimize the line length and parasitic capacitance of this pin.
7	Gnd PLL	Gnd	Ground pin for PLL section of IC.
8	T_X VCO	Input	Transmit divide counter input which is driven by an ac–coupled external transmit loop VCO. The minimum signal level is 200 mVpp @ 60.0 MHz. This pin also functions as the test mode input for the counter tests.
9 10 11	Data EN Clk	Input	Microprocessor serial interface input pins for programming various counters and control functions.
12	Clk Out	Output	Microprocessor Clock Output which is derived from the 2nd LO crystal oscillator and a programmable divider. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes.
13	CD Out	I/O	Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to "wake–up" from Inactive Mode.
14	BD_1 Out	Output	Low battery detect output #1 (open collector with external pull–up resistor).
15	DA Out	Output	Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
16	BD_2 Out	Output	Low battery detect output #2 (open collector with external pull–up resistor).
17	T_X Out	Output	T_X path audio output.
18	C Cap	–	Compressor rectifier filter capacitor pin. Pull pin high through a capacitor.
19	C In	Input	Compressor input (ac–coupled).
20	Amp Out	Output	Microphone amplifier output.
21	T_X In	Input	T_X path input to microphone amplifier (Mic Amp) (ac–coupled).
22	DA In	Input	Data amplifier input (ac–coupled).
23	V_{CC} Audio	Supply	V_{CC} supply for audio section.
24	R_X Audio In	Input	R_X audio input (ac–coupled).
25	Det Out	Output	Audio output from FM detector.
26	RSSI	Output	Receive Signal Strength Indicator filter capacitor.
27 28	Q Coil Lim Out	–	A quad coil or ceramic discriminator connected to these pins as part of the FM demodulator circuit.
29	V_{CC} RF	Supply	V_{CC} supply for RF receiver section.
30 31	Lim C_2 Lim C_1	–	IF amplifier/limiter capacitor pins.
32	Lim In	Input	Signal input for IF amplifier/limiter.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Type	Description
33	SGND RF	Gnd	Ground pin for RF section of the IC.
34	Mix_2 In	Input	Second mixer input.
35	Mix_2 Out	Output	Second mixer output.
36	Gnd RF	Gnd	Ground pin for RF section of the IC.
37	Mix_1 Out	Output	First mixer output.
38	Mix_1 In_2	Input	Negative phase first mixer input.
39	Mix_1 In_1	Input	Positive phase first mixer input.
40 41	LO_1 In LO_1 Out	–	Tank Elements for 1st LO Multivibrator Oscillator are connected to these pins.
42	V_{cap} Ctrl	–	1st LO Varactor Control Pin.
43	Gnd Audio	Gnd	Ground for audio section of the IC.
44	SA Out	Output	Speaker amplifier output.
45	SA In	Input	Speaker amplifier input (ac–coupled).
46	E Out	Output	Expandor output.
47	E_{cap}	–	Expandor rectifier filter capacitor pin. Pull pin high through a capacitor.
48	E In	Input	Expandor Input.
49	Scr Out	Output	R_X Scrambler Output.
50	Ref_2	–	Reference voltage input for Low Battery Detect #2.
51	Ref_1	–	Reference voltage input for Low Battery Detect #1.
52	V_B	–	Internal half supply analog ground reference.

FM Receiver

The FM receiver can be used with either a quad coil or a ceramic resonator. The FM receiver and 1st LO have been designed to work for all country channels, including 25 channel U.S., without the need for any external switching circuitry (see Figure 29).

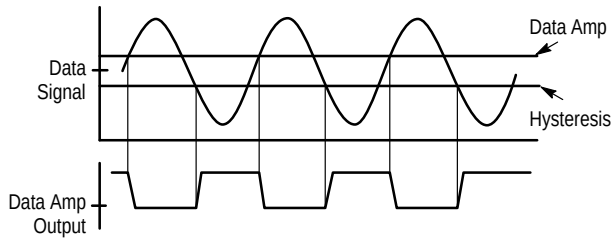
RSSI/Carrier Detect

Connect 0.01 μF to Gnd from “RSSI” output pin to form the carrier detect filter. “CD Out” is an open collector output which requires an external 100 kΩ pull–up resistor to V_{CC}. The carrier detect threshold is programmable through the MPU interface.

Data Amp Comparator

The data amp comparator is an inverting hysteresis comparator. Its open collector output has an internal 100 kΩ pull–up resistor. A band pass filter is connected between the “Det Out” pin and the “DA In” pin with component values as shown in Figure 1 (Test Circuit). The “DA In” input signal is ac–coupled.

Figure 2. Data Amp Operation



Expandor/ Compressor

In Appendix B, the EIA/CCITT recommendations for measurement of the attack and decay times are defined. The curves in Figures 3 and 4 show the typical expandor and compressor output versus input responses.

Figure 3. Expandor Typical Response

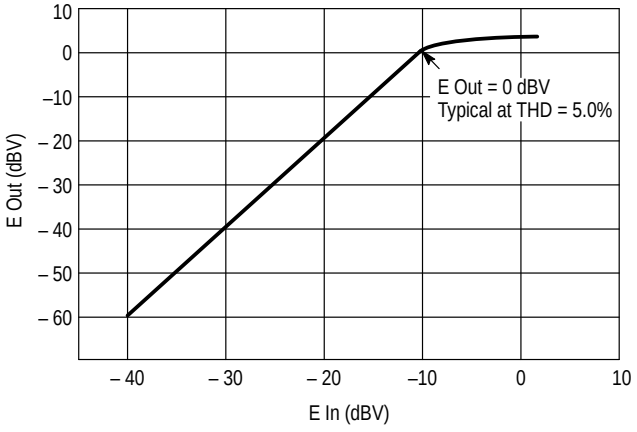
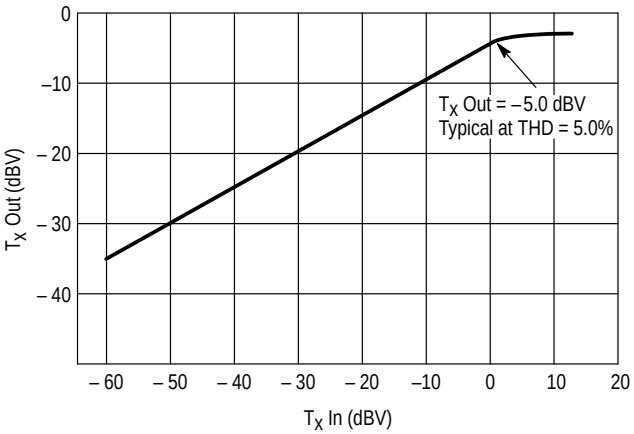


Figure 4. Compressor Typical Response



R_X Audio Path (LPF/R_X Gain Adjust/ R_X Mute/Expandor/Volume Control)

The R_X Audio signal path goes from “R_X Audio In” (Pin 24) to “E Out” (Pin 46). The “R_X Audio In” input signal is ac coupled. AC couple between “Scr Out” and “E In” (see Figure 3).

Speaker Amp/SP Mute

The Speaker Amp is an inverting rail–to–rail operational amplifier. The noninverting input is connected to the internal V_B reference. External resistors and capacitors are used to set the gain and frequency response. The “SA In” Input is ac coupled.

Mic Amp

The Mic Amp is an inverting rail–to–rail operational amplifier with noninverting input terminal connected to internal V_B reference. External resistors and capacitors are set to the gain and frequency response. The “T_X In” input is ac coupled.

T_X Audio Path (Compressor/ALC/T_X Mute/ Limiter/LPF/T_X Gain Adjust)

The T_X Audio signal path goes from “C In” (Pin 19) to “T_X Out” (Pin 17). The “C In” input signal is ac coupled. The ALC (Automatic Level Control) provides a “soft” limit to the output signal swing as the input voltage increases slowly (i.e., a sine wave is maintained). The Limiter circuit limits rapidly changing signal levels by clipping the signal peaks. The ALC and/or Limiter can be disabled through the MPU serial interface (see Figure 4).

T_X and R_X Scrambler

The T_X and R_X signal paths each contain a frequency inversion scrambler in the MC13110. Each scrambler contains a pre–mixer low pass switched capacitor filter (SCF), a double balanced mixer and a post–mixer low pass switched capacitor filter. The scrambler function can be defeated by setting the T_X or R_X Scrambler Bypass bits in the control register to “1” through the MPU interface. In this mode, the mixer and the post–mixer LPF are bypassed and

only the pre–mixer LPF remains in the signal path. The SCF corner frequencies are proportional to the SCF clock. The SCF Clock Divider is programmable through the MPU interface, (SCF Clock) = F(2nd LO)/(SCF Divider Value*2). The scrambler modulation frequency is (SCF Clock)/40. Four scrambler modulation frequencies may be selected (see Figures 28 and 29).

PLL Voltage Regulator

The "PLL V_{ref}" pin is the internal supply voltage for the R_X and T_X PLL's. It is regulated to a nominal 2.5 V. The "V_{CC} Audio" pin is the supply voltage for the internal voltage regulator. Two capacitors with 10 μF and 0.1 μF values must be connected to the "PLL V_{ref}" pin to filter and stabilize this regulated voltage. The "PLL V_{ref}" pin may be used to power other IC's as long as the total external load current does not exceed 1.0 mA. The tolerance of the regulated voltage is initially ±8.0%, but is improved to ±4.0% after the internal Bandgap voltage reference is adjusted electronically through the MPU serial interface. The voltage regulator is turned off in the Standby and Inactive modes to reduce current drain. In these modes, the "PLL V_{ref}" pin is internally connected to the "V_{CC} Audio" pin (i.e., the power supply voltage is maintained but is now unregulated).

Low Battery Detect

Two external precision resistor dividers are used to set independent thresholds for two battery detect hysteresis comparators. The voltages on "Ref_1" and "Ref_2" are compared to an internally generated 1.5 V reference voltage. The tolerance of the internal reference voltage is initially ±6.0%. The Low Battery Detect threshold tolerance can be improved by adjusting a trim–pot in the external resistor divider. Alternately, the tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming. The internal reference can be measured directly at the "V_B" pin. During final test of the telephone, the V_B internal reference voltage is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13110 IC is powered up. Low Battery Detect outputs are open collector.

Power Supply Voltage

This circuit is used in a cordless telephone handset and base unit. The handset is battery powered and can operate on three NiCad cells or on 5.0 V supply.

PLL Frequency Synthesizer General Description

Figure 5 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL). This dual PLL is fully programmable through the MCU serial interface and supports most country channel frequencies including USA (25 ch), Spain, Australia, Korea, New Zealand, U. K., Netherlands, France, and China.

The 2nd local oscillator and reference divider provide the reference frequency for the receive (R_X) and transmit (T_X) PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_X and T_X reference frequency values. Additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.25 kHz reference frequencies required for the U. K. The 14–bit T_X counter is programmed for the desired transmit channel frequency. The 14–bit R_X counter is programmed for the desired first local oscillator frequency. All counters power up in the proper default state for USA channel #21 (channel #6 for FCC 10 channel band) and for a 10.24 MHz reference frequency crystal. Internal fixed capacitors can be connected to the tank circuit of the 1st LO through microprocessor control to extend the sensitivity of the 1st LO for U.S. 25 channel operation.

PLL I/O Pin Specifications

The 2nd LO, R_X and T_X PLL's, and MPU serial interface are powered by the internal voltage regulator at the "PLL V_{ref}" pin. The "PLL V_{ref}" pin is the output of a voltage regulator which is powered from the "V_{CC} Audio" power supply pin and is regulated by an internal bandgap voltage reference. Therefore, the maximum input and output levels for most PLL I/O pins (LO_2 In, LO_2 Out, R_X PD, T_X PD, T_X VCO) is the regulated voltage at the "PLL V_{ref}" pin. The ESD protection diodes on these pins are also connected to "PLL V_{ref}". Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 6 shows a simplified schematic of the I/O pins.

Figure 5. Dual PLL Simplified Block Diagram

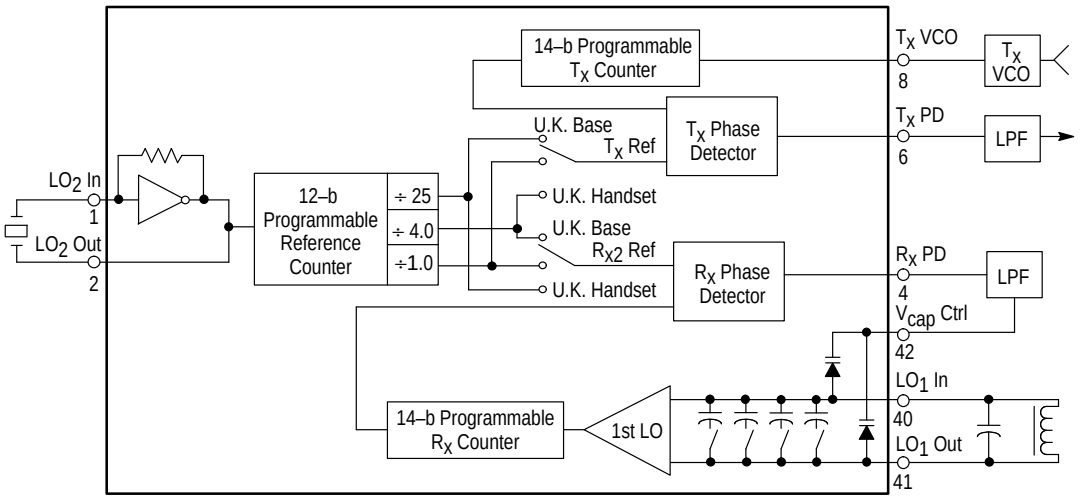
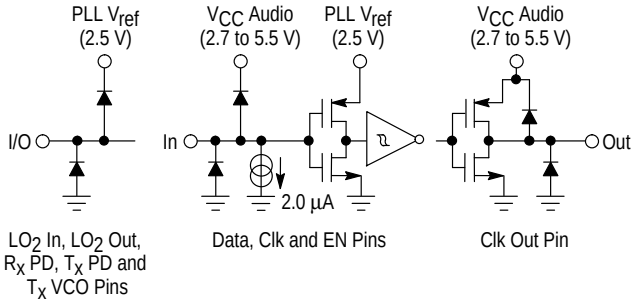


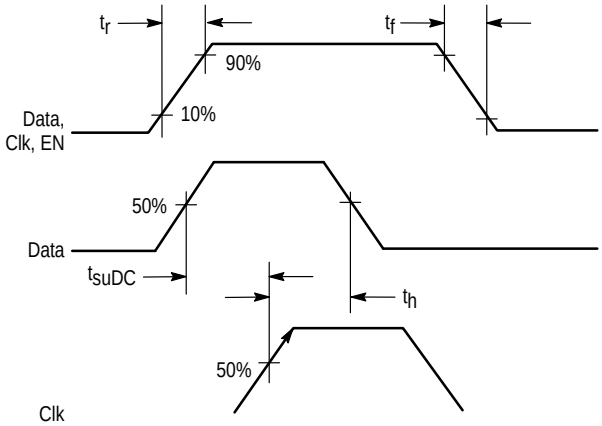
Figure 6. PLL I/O Pin Simplified Schematics



Microprocessor Serial Interface

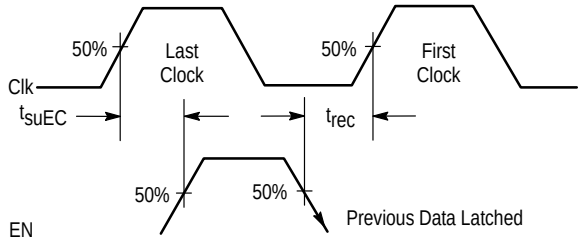
The “Data”, “Clk”, and “EN” pins provide an MPU serial interface for programming the reference counters, the transmit and receive channel divider counters, the switched capacitor filter clock counter, and various control functions. The “Data” and “Clk” pins are used to load data into the shift register. Figure 7 shows the timing required on the “Data” and “Clk” pins. Data is clocked into the shift register on positive clock transitions.

Figure 7. Data and Clock Timing Requirement



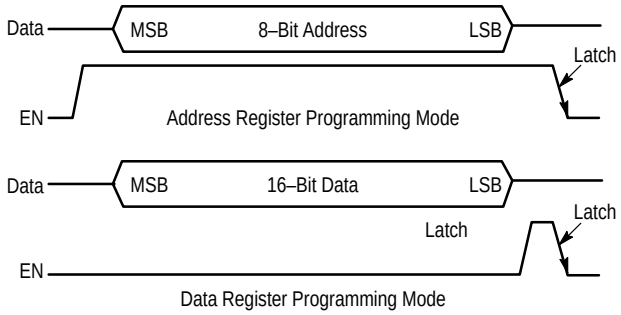
After data is loaded into the shift register, the data is latched into the appropriate latch register using the “EN” pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register specified by the address that was previously loaded. Figure 5 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 8. Enable Timing Requirement



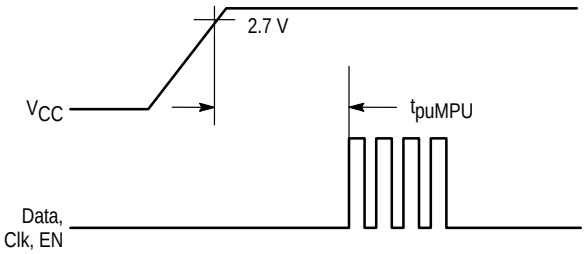
The state of the EN pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 9 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when “EN” is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the “EN” high state. The convention in these figures is that latch bits to the left are loaded into the shift register first.

Figure 9. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 µs after the power supply has reached its minimum level during power–up (see Figure 10). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_X, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 10. Microprocessor Serial Interface Power–Up Delay



Data Registers

Figure 11 shows shows the data latch registers and addresses which are used to select each of these registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. Bits preceeding the register must be “0’s” as shown in Figure 11.

Figure 11. Microprocessor Interface Data Latch Registers

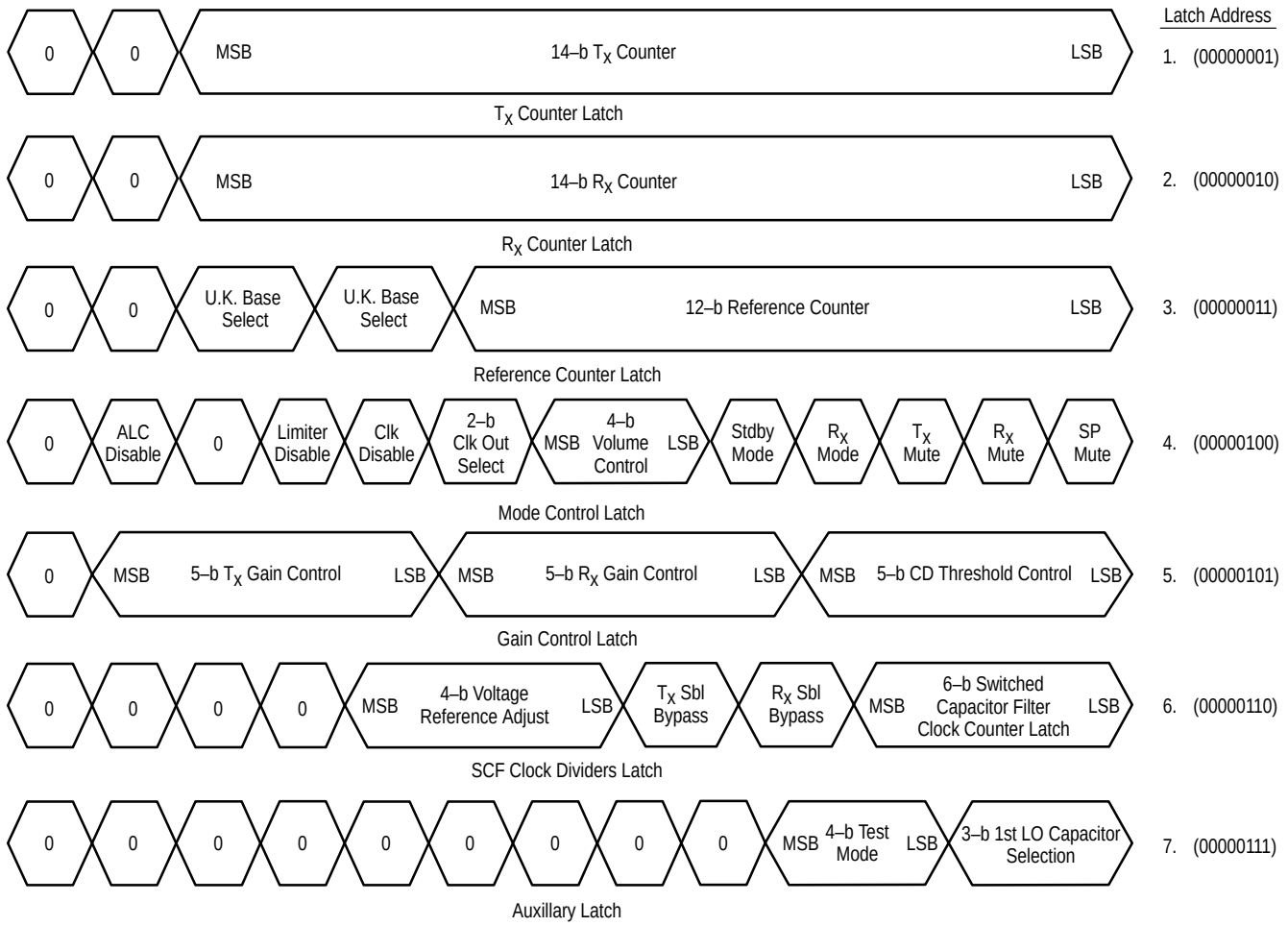


Figure 12. Reference Frequency and Reference Divider Values

Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency	SC Filter Clock Divider	SC Filter Clock Frequency	Scrambler Modulation Divider	Scrambler Modulation Frequency
10.24 MHz	2048	1.0	5.0 kHz	31	165.16 kHz	40	4.129 kHz
10.24 MHz	1024	4.0	2.5 kHz	31	165.16 kHz	40	4.129 kHz
11.15 MHz	2230	1.0	5.0 kHz	34	163.97 kHz	40	4.099 kHz
12.00 MHz	2400	1.0	5.0 kHz	36	166.67 kHz	40	4.167 kHz
11.15 MHz	1784	1.0	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	4.0	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	25	1.0 kHz	34	163.97 kHz	40	4.099 kHz

Reference Frequency Selection

The "LO_2 In" and "LO_2 Out" pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 12 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries. "LO_2 In" may also serve as an input for an externally generated reference signal which is ac–coupled. The switched capacitor filter 6–bit programmable counter must be programmed for the crystal frequency that is selected since this clock is derived from the crystal frequency and must be held constant regardless of the crystal that is selected. The actual switched capacitor clock divider ratio is twice the programmed divider ratio since there is a fixed divide by 2.0 after the programmable counter. The scrambler mixer modulation frequency is the switched capacitor clock divided by 40.

Reference Counter

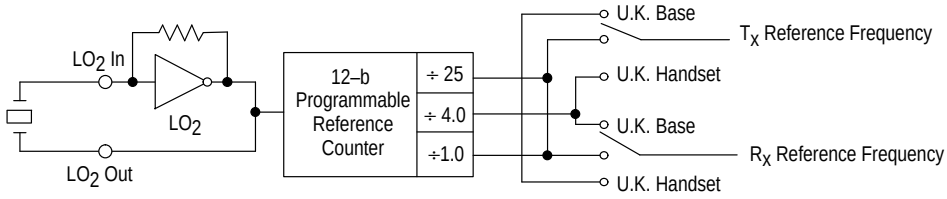
Figure 13 shows how the reference frequencies for the R_X and T_X loops are generated. All countries except the U.K.

require that the T_X and R_X reference frequencies be identical. In this case, set “U.K. Base Select” and “U.K. Handset Select” bits to “0”. Then the fixed divider is set to “1” and the T_X and R_X reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value. The U.K. is a special case which requires a different reference frequency value for T_X and R_X. For U.K. base operation, set “U.K. Base Select” to “1”. For U.K. handset operation, set “U.K. Handset Select” to “1”.The Netherlands is also a special case since a 2.5 kHz reference frequency is used for both the T_X and R_X reference and the total divider value required is 4096 which is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set “U.K. Base Select” to “1” and set “U.K. Handset Select” to “1”. This will give a fixed divide by 4 for both the T_X and R_X reference. Then set the reference divider to 1024 to get a total divider of 4096.

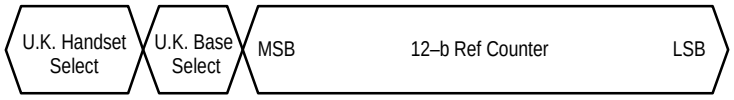
Mode Control Register

Power saving modes, mutes, disables, volume control, and microprocessor clock output frequency are all set by the Mode Control Register. Operation of the Mode Control Register is explained in Figures 14 through 21.

Figure 13. Reference Register Programming Mode



U.K. Handset Select	U.K. Base Select	T_X Divider Value	R_X Divider Value	Application
0	0	1.0	1.0	All but U.K. and Netherlands
0	1	25	4.0	U.K. Base Set
1	0	4.0	25	U.K. Hand Set
1	1	4.0	4.0	Netherlands Base and Hand Set



14–Bit Reference Counter Latch

Figure 14. Mode Control Register Bits

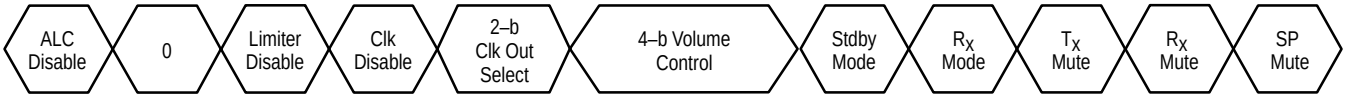


Figure 15. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
Limiter Disable	1 0	Limiter Disabled Normal Operation
Clock Disable	1 0	MPU Clock Output Disabled Normal Operation
T_X Mute	1 0	Transmit Channel Muted Normal Operation
R_X Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13110 is used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation; Active, R_X, Standby, Interrupt, and Inactive. In Active mode, all circuit blocks are powered. In R_X mode, all circuitry is powered down except for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In Inactive Mode, all circuitry is powered down except the MPU interface. Latch memory is maintained in all modes. Figure 16 shows the control register bit values for selection of each power saving mode and Figure 17 shows the circuit blocks which are powered in each of these operating modes.

Figure 16. Power Saving Mode Selection

Stdby Mode Bit	R_X Mode Bit	"CD Out/ Hardware Interrupt" Pin	Mode
0	0	X	Active
0	1	X	R_X
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Interrupt

Figure 17. Power Saving Modes

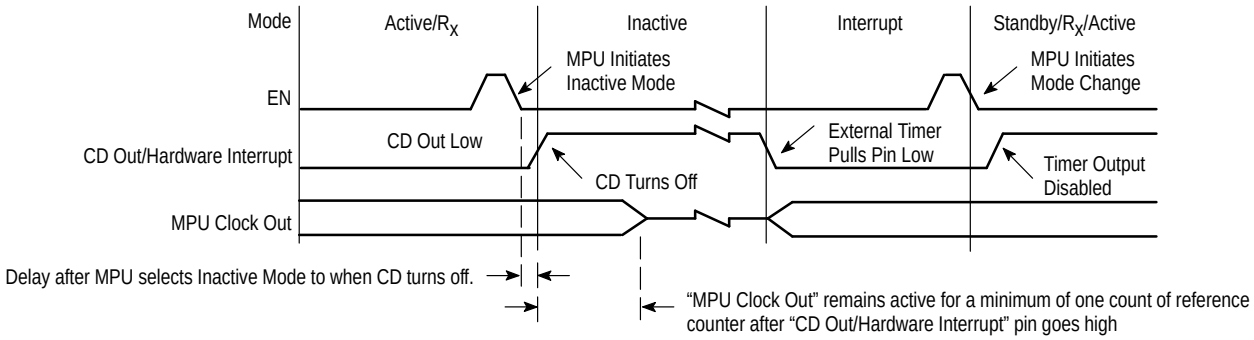
Circuit Blocks	Active	R_X	Standby	Inactive
"PLL V_{ref}" Regulated Voltage	X	X	X[1]	X[1]
MPU Interface	X	X	X	X
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver and 1st LO VCO	X	X		
R_X PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_X PLL	X			
R_X and T_X Audio Paths	X			

NOTE: In Standby and Inactive Modes, "PLL V_{ref}" remains powered but is not regulated. It will fluctuate with V_{CC}.

Inactive Mode Operation and Hardware Interrupt

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the combo IC into the Inactive mode, which turns off the MPU Clock Output (see Figure 18), and then disable the microprocessor. In order to give the MPU adequate time to power down, the MPU Clock output remains active for a minimum of one reference counter cycle (about 200 μs) after the command is given to switch into the "Inactive" mode. An external timing circuit should be used to initiate the turn–on sequence. The "CD Out" pin has a dual function. In the Active and R_X modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state due to the external pull–up resistor. In the Inactive mode, the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low" by the external timing circuit, the combo IC switches from the Inactive to the Interrupt mode thereby turning on the MPU Clock Output. The MPU can then resume control of the combo IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active or R_X modes.

Figure 18. Hardware Interrupt Operation



MPU "Clk Out" Divider Programming

This pin is a clock output which is derived from the crystal oscillator (2nd local oscillator). It can be used to drive a microprocessor and thereby reduce the number of crystals required. Figure 19 shows the relationship between the crystal frequency and the clock output for different divider values. Figure 20 shows the "Clk Out" register bit values.

Figure 19. Clock Output Values

Crystal Frequency	Clock Output Divider			
	2	3	4	5
10.24 MHz	5.120 MHz	3.413 MHz	2.560 MHz	2.048 MHz
11.15 MHz	5.575 MHz	3.717 MHz	2.788 MHz	2.230 MHz
12.00 MHz	6.000 MHz	4.000 MHz	3.000 MHz	2.400 MHz

MPU "Clk Out" Radiated Noise on Circuit Board

The clock line running between the MC13110 and the microprocessor has the potential to radiate noise which can cause problems in the system especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize radiated noise, a 1.0 kΩ resistor is included on–chip in series with the "Clk Out" output driver. A small capacitor can be connected to the "Clk Out" line on the PCB to form a single pole low pass filter. This filter will significantly reduce noise radiated from the "Clk Out" line.

Volume Control Programming

The volume control adjustable gain block can be programmed in 2.0 dB gain steps from –14 dB to +16 dB. The power–up default value is 0 dB. (See Figure 21.)

Figure 20. Clock Output Divider

Clk Out Bit #1	Clk Out Bit #0	Clk Out Divider Value
0	0	2
0	1	3
1	0	4
1	1	5

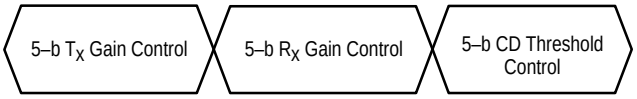
Figure 21. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the T_X Voltage Gain, R_X Voltage Gain, and Carrier Detect threshold. Operation of these latch bits are explained in Figures 22, 23 and 24.

Figure 22. Gain Control Latch Bits



T_X and R_X Gain Programming

The T_X and R_X audio signal paths each have a programmable gain block. If a T_X or R_X voltage gain other than the nominal power–up default is desired, it can be programmed through the MPU interface. Alternately, these programmable gain blocks can be used during final test of the telephone to electronically adjust for gain tolerances in the telephone system as shown in Figure 23. In this case, the T_X and R_X gain register values should be stored in ROM during final test so that they can be reloaded each time the combo IC is powered up.

Figure 23. T_X and R_X Gain Control

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Control #	Gain/Attenuation Amount
0	0	0	0	0	0	–15 dB
0	0	0	0	1	1	–14 dB
0	0	0	1	0	2	–13 dB
0	0	0	1	1	3	–12 dB
0	0	1	0	0	4	–11 dB
0	0	1	0	1	5	–10 dB
0	0	1	1	0	6	–9.0 dB
0	0	1	1	1	7	–8.0 dB
0	1	0	0	0	8	–7.0 dB
0	1	0	0	1	9	–6.0 dB
0	1	0	1	0	10	–5.0 dB
0	1	0	1	1	11	–4.0 dB
0	1	1	0	0	12	–3.0 dB
0	1	1	0	1	13	–2.0 dB
0	1	1	1	0	14	–1.0 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1.0 dB
1	0	0	0	1	17	2.0 dB
1	0	0	1	0	18	3.0 dB
1	0	0	1	1	19	4.0 dB
1	0	1	0	0	20	5.0 dB
1	0	1	0	1	21	6.0 dB
1	0	1	1	0	22	7.0 dB
1	0	1	1	1	23	8.0 dB
1	1	0	0	0	24	9.0 dB
1	1	0	0	1	25	10 dB
1	1	0	1	0	26	11 dB
1	1	0	1	1	27	12 dB
1	1	1	0	0	28	13 dB
1	1	1	0	1	29	14 dB
1	1	1	1	0	30	15 dB
1	1	1	1	1	31	16 dB

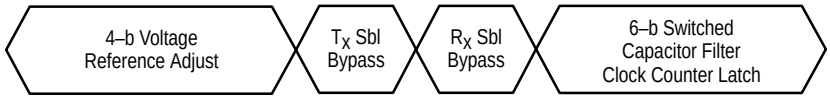
Carrier Detect Threshold Programming

The “CD Out” pin gives an indication to the microprocessor if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be programmed through the MPU interface as shown in Figure 24. Alternately, the carrier detect threshold can be electronically adjusted during final test of the telephone to reduce the tolerance of the carrier detect threshold. This is done by measuring the threshold and then by adjusting the threshold through the MPU interface. In this case, it is necessary to store the carrier detect register value in ROM so that the CD register can be reloaded each time the combo IC is powered up.

Figure 24. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	–20 dB
0	0	0	0	1	1	–19 dB
0	0	0	1	0	2	–18 dB
0	0	0	1	1	3	–17 dB
0	0	1	0	0	4	–16 dB
0	0	1	0	1	5	–15 dB
0	0	1	1	0	6	–14 dB
0	0	1	1	1	7	–13 dB
0	1	0	0	0	8	–12 dB
0	1	0	0	1	9	–11 dB
0	1	0	1	0	10	–10 dB
0	1	0	1	1	11	–9.0 dB
0	1	1	0	0	12	–8.0 dB
0	1	1	0	1	13	–7.0 dB
0	1	1	1	0	14	–6.0 dB
0	1	1	1	1	15	–5.0 dB
1	0	0	0	0	16	–4.0 dB
1	0	0	0	1	17	–3.0 dB
1	0	0	1	0	18	–2.0 dB
1	0	0	1	1	19	–1.0 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1.0 dB
1	0	1	1	0	22	2.0 dB
1	0	1	1	1	23	3.0 dB
1	1	0	0	0	24	4.0 dB
1	1	0	0	1	25	5.0 dB
1	1	0	1	0	26	6.0 dB
1	1	0	1	1	27	7.0 dB
1	1	1	0	0	28	8.0 dB
1	1	1	0	1	29	9.0 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Figure 25. Switched Capacitor Filter Clock Divider/Voltage Reference Adjust Latch Bits



SCF Clock Divider/Voltage Reference Adjust Register

This register controls the scrambler bypass mode, the divider value for the programmable switched capacitor filter clock divider, and the voltage reference adjust. Operation is explained in Figures 25 through 30.

Figure 26. Bypass Mode Bit Description

T_X Scrambler Bypass	1	T_X Scrambler Post–Mixer LPF and Mixer Bypassed
	0	Normal Operation with T_X Scrambler
R_X Scrambler Bypass	1	R_X Scrambler Post–Mixer LPF and Mixer Bypassed
	0	Normal Operation R_X Scrambler

Switched Capacitor Filter Clock Programming

A block diagram of the switched capacitor filter and scrambler modulation clock dividers is shown in Figure 27. There is a fixed divide by 2 after the programmable divider. The switched capacitor filter clock value is given by the following equation;

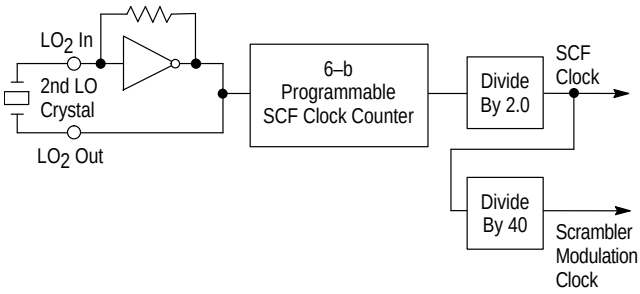
(SCF Clock) = F(2nd LO)/(SCF Divider Value * 2)

The scrambler modulation clock frequency (SMCF) is proportional to the SCF clock and is given by the following equation;

SMCF = (SCF Clock Frequency)/40

The SCF divider should be set to a value which gives a SCF Clock as close to 165.16 kHz as possible based on the 2nd LO frequency which is chosen (see Figure 12).

Figure 27. SCF Clock and Scrambler Carrier Circuit



Scrambler Modulation Frequency Programming

Four different scrambler modulation frequencies may be selected by programming the SCF Clock divider as shown in Figures 28 and 29. Note that all filter corner frequencies will change proportionately with the SCF Clock and Scrambler Modulation Frequency. The power–up default SCF Clock divider value is 31.

Figure 28. Scrambler Modulation Frequency Programming for a 10.240 MHz 2nd LO

SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)	R_X Upper (Scrambler Bypassed) Corner Frequency (kHz)	T_X Upper (Scrambler Bypassed) Corner Frequency (kHz)
29	58	176.55	4.414	267.2	3.902	4.147	3.955
30	60	170.67	4.267	258.3	3.772	4.008	3.823
31	62	165.16	4.129	250.0	3.650	3.879	3.700
32	64	160.00	4.000	242.2	3.536	3.758	3.584

NOTE: All filter corner frequencies have a tolerance of ±3%.

Figure 29. Scrambler Modulation Frequency Programming for a 11.15 MHz 2nd LO

SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)	R_X Upper (Scrambler Bypassed) Corner Frequency (kHz)	T_X Upper (Scrambler Bypassed) Corner Frequency (kHz)
32	64	174.22	4.355	263.7	3.850	4.092	3.903
33	66	168.94	4.223	255.7	3.733	3.968	3.785
34	68	163.97	4.099	248.2	3.624	3.851	3.673
35	70	159.29	3.982	241.1	3.520	3.741	3.568

NOTE: All filter corner frequencies have a tolerance of ±3%.

Voltage Reference Adjustment

The internal 1.5 V Bandgap voltage reference provides the voltage reference for the “BD1 Out” and “BD2 Out” low battery detect circuits, the “PLL V_{ref}” voltage regulator, the “V_B” reference, and all internal analog ground references. The initial tolerance of the Bandgap voltage reference is ±6%. The tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming.

During final test of the telephone, the battery detect threshold is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13110 is powered up (see Figure 30).

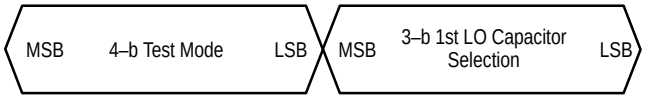
Figure 30. Bandgap Voltage Reference Adjustment

V_{ref}Adj. Bit #3	V_{ref}Adj. Bit #2	V_{ref}Adj. Bit #1	V_{ref}Adj. Bit #0	V_{ref}Adj. #	V_{ref} Adj. Amount
0	0	0	0	0	–9.0%
0	0	0	1	1	–7.8%
0	0	1	0	2	–6.6%
0	0	1	1	3	–5.4%
0	1	0	0	4	–4.2%
0	1	0	1	5	–3.0%
0	1	1	0	6	–1.8%
0	1	1	1	7	–0.6%
1	0	0	0	8	+0.6 %
1	0	0	1	9	+1.8 %
1	0	1	0	10	+3.0 %
1	0	1	1	11	+4.2 %
1	1	0	0	12	+5.4 %
1	1	0	1	13	+6.6 %
1	1	1	0	14	+7.8 %
1	1	1	1	15	+9.0 %

Auxiliary Register

The auxiliary register contains a 3–bit 1st LO Capacitor Selection latch and a 4–bit Test Mode latch. Operation of these latch bits are explained in Figures 31, 32 and 34.

Figure 31. Auxiliary Register Latch Bits



First Local Oscillator Programmable Selection (U.S. Applications)

There is a very large frequency difference between the minimum and maximum channel frequencies in the 25 Channel U.S. Standard.The sensitivity of the 1st LO may not be large enough to accommodate this large frequency variation. Fixed capacitors can be connected across the 1st LO tank circuit to change the 1st LO sensitivity. Internal switches and capacitors are provided to enable microprocessor control over internal fixed capacitor values. Figures 32 and 33 show the schematic representation of the 1st LO and the tank circuit. Figure 34 shows the latch control bit values for microprocessor control.

Figure 32. First Local Oscillator Schematic

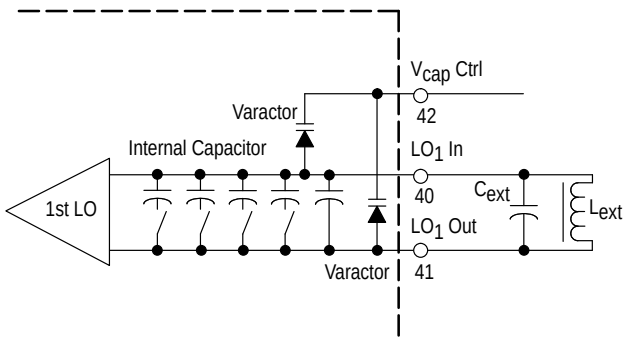


Figure 33. First Local Oscillator Simplified Schematic

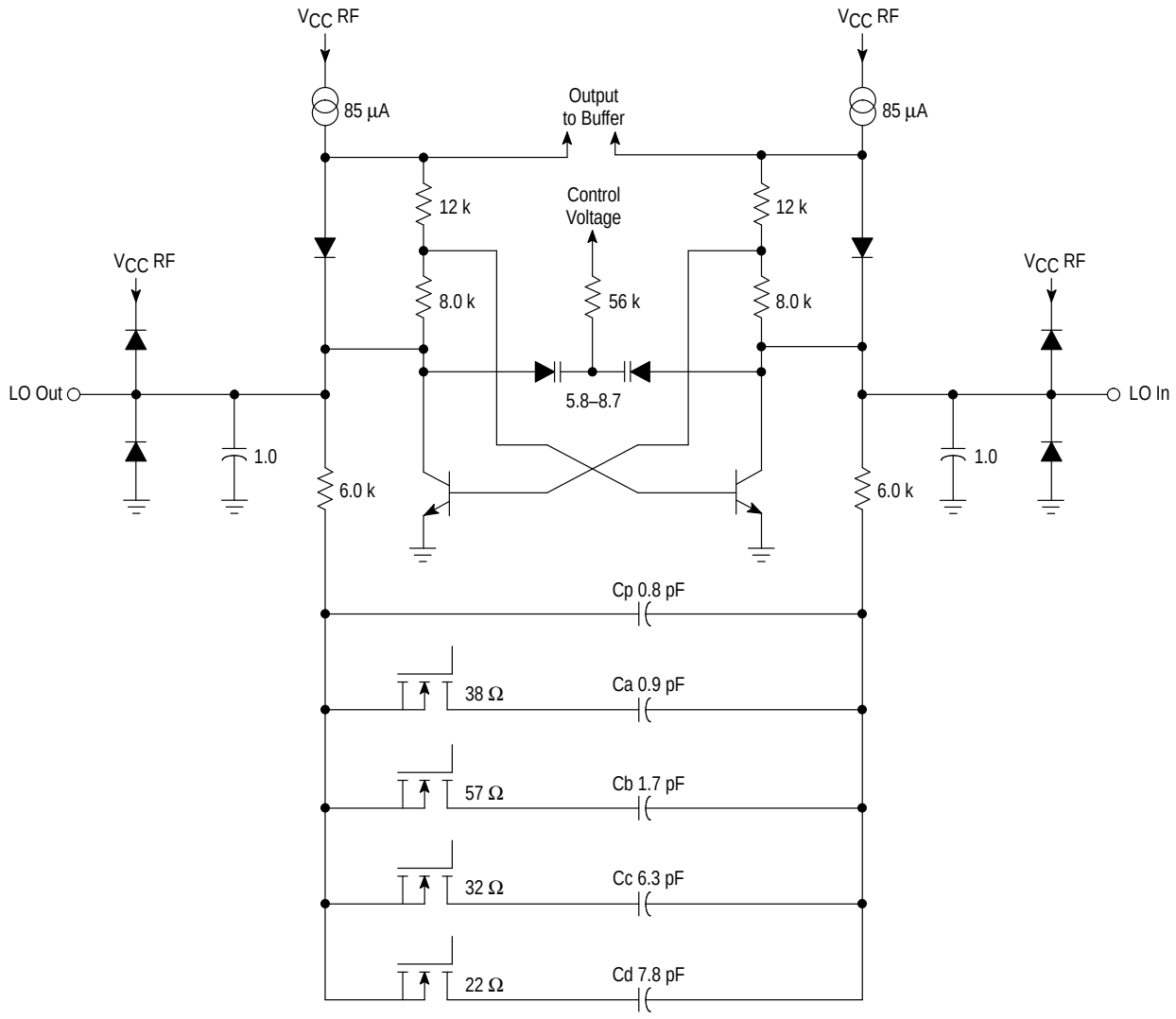


Figure 34. First Local Oscillator Programmable Capacitor Selection for U.S. 25 Channels

1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap Bit 0	1st LO Cap. Select	U.S. Base Chan-nels	U.S. Handset Channels	Internal Capacitor Value	Varactor Value over 0.3 to 2.5 V	Equivalent Internal Parallel Resistance at 40 MHz (kΩ)	Equivalent Internal Parallel Resistance at 51 MHz (kΩ)	External Capacitor Value	External Inductor Value
0	0	0	0	1–10	–	0.8 pF	5.8–8.7 pF	>1000	>1000	24 pF	0.47 µH
0	0	0	0	–	1–10	0.8 pF	5.8–8.7 pF	>1000	>1000	33 pF	0.47 µH
0	0	1	1	11–16	–	2.5 pF	5.8–8.7 pF	35	21	24 pF	0.47 µH
0	1	0	2	17–25	–	1.7 pF	5.8–8.7 pF	100	60	24 pF	0.47 µH
0	1	1	3	–	11–16	8.6 pF	5.8–8.7 pF	6.1	3.8	33 pF	0.47 µH
1	0	0	4	–	17–25	7.1 pF	5.8–8.7 pF	8.0	5.0	33 pF	0.47 µH

Figure 35. Digital Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T_X V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	0	Normal Operation	>200 mVpp	–
1	0	0	0	1	R_X Counter, upper 6	0 to 2.5 V	Input Frequency/64
2	0	0	1	0	R_X Counter, lower 8	0 to 2.5 V	See Note Below
3	0	0	1	1	R_X Prescaler	0 to 2.5 V	Input Frequency/4
4	0	1	0	0	T_X Counter, upper 6	0 to 2.5 V	Input Frequency/64
5	0	1	0	1	T_X Counter, lower 8	0 to 2.5 V	See Note Below
6	0	1	1	0	T_X Prescaler	>200 mVpp	Input Frequency/4
7	0	1	1	1	Reference Counter	0 to 2.5 V	Input Frequency/Reference Counter Value
8	1	0	0	0	Divide by 4, 25	0 to 2.5 V	Input Frequency/100
9	1	0	0	1	SC Counter	0 to 2.5 V	Input Frequency/SC Counter Value
10	1	0	1	0	Scrambler Modulation Counter	0 to 2.5 V	Input Frequency/40

NOTE: To determine the correct output, look at the lower 8–bits in the R_X or T_X register (Divisor (7;0). If the value of the divisor is > 16, then the output divisor value is Divisor (7;2) (the upper 6–bits of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) > = 2, then output divisor value is Divisor (3;2) (bits 2 and 3 of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) < 2, then output divisor value is (Divisor (3;2) + 60).

Figure 36. Analog Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Circuit Blocks Under Test	Input Pin	Output Pin
11	1	0	1	1	Compressor	C In	T_X In
12	1	1	0	0	T_X Scrambler	T_X In	T_X Out
13	1	1	0	1	ALC Gain = 10 Option	N/A	N/A
14	1	1	1	0	ALC Gain = 25 Option	N/A	N/A
15	1	1	1	1	Not Used	N/A	N/A

Test Modes

Digital and analog test modes can be selected through the 4–bit Test Mode Register. In digital test mode, the "T_X V_{CO}" input pin is multiplexed to the input of the counter under test and the output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. Make sure test mode bits are set to "0's" for normal operation. Digital test mode operation is described in Figure 35. During normal operation and when testing the T_X Prescaler, the "T_X VCO" input can be a minimum of 200 mVpp at 80 MHz and should be ac–coupled. For other test modes, input signals should be standard logic levels of 0 to 2.5 V and a maximum frequency of 16 MHz.

The analog test modes enable separate testing of the Compressor and T_X Scrambler blocks as shown in Figure 36. Also, ALC Gain options can be selected through analog test modes.

Power–Up Defaults for Control and Counter Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The device is initially placed in the Rx mode with all mutes active. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The switched capacitor filter clock counter is set properly for operation with a 10.24 MHz crystal. The scrambler bypass mode control are set for normal operation of scrambler. The T_X and R_X latch registers are set for USA Channel Frequency 21 (Channel 6 for previous FCC 10 Channel Band). Figure 37 shows the initial power–up states for all latch registers.

Figure 37. Latch Register Power–Up Defaults

		MSB								LSB							
Register	Count	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_X	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_X	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	X	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	0	1	1	1	1	0	1	1	1	1	1	0	1	0	0
SC	31	–	–	–	–	0	1	1	1	0	0	0	1	1	1	1	1
Aux	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

Evaluation PC Board

The PCB should be double sided with a full ground plane on one side; any leaded components are inserted on the ground plane side. This affords shielding and isolation from the circuit side of the PCB. The other side is the circuit side which has the interconnect traces and the surface mount components. In cases where cost allows, it may be benificial to use multi layer boards.

The placement of certain components specified in the application circuits is very critical. These components should be placed first and the other less critical components are fitted in last. In general, all RF paths should be kept as short as possible, ground pins should be grounded at the pins and V_{CC} pins should have adequate decoupling to ground at the pins. In mixed mode systems where digital and RF/Analog circuitry are present, the V_{EE} and V_{CC} busses are isolated ac –wise from each other.

Component Selection

The evaluation PC board is designed to accommodate specific components, while in some cases it is versatile enough to use components from various manufacturers and coil types. The application circuit schematics specify particular components that were used to achieve the results shown in the typical curves and tables, but alternate components should give similar results.

The MC13110 IC is capable of matching the sensitivity, IMD, adjacent channel rejection, and other performance criteria of a multi–chip analog cordless telephone system. For the most part, the same external components are used as in the multi–chip solution. In the following discussion, various parts of the system are analyzed for best peformance and cost tradeoffs. Specific recommendations are made where certain components or circuit designs offer superior performance. The system analyzed is the USA “CT–1” cordless phone.

Input Matching/Sensitivity

The sensitivity of the IC is typically 0.56 μVrms matched with no preamp. To achieve suitable system performance, a preamp and passive duplexer must be used. In production final test, each section of the IC is separately tested to guarantee its system performance in the specific application. The preamp and duplexer yields typically –114 dBm 12 dB SINAD sensitivity performance under full duplex operation.

The duplexer is important to achieve full duplex operation without significant “de–sensing” of the receiver by the transmitter. The combination of the duplexer and preamp circuit have to attenuate the transmitter power to the receiver by over 60 dB to be effective. They do this while improving the receiver system noise figure and without giving up too much IMD intermodulation performance.

The duplexer may be a single piece unit offered by Shimida and Sansui products (designed for 10 channel CT–1 cordless phone) or a two piece solution offered by Toko (designed for 25 channel operation). The duplexer frequency response at the receiver port has a notch at the transmitter frequency band of about 35 to 40 dB with a 2.0 to 3.0 dB insertion loss at the receiver frequency band.

The preamp circuit utilizes a tuned transformer at the output side of the amplifier; this transformer is designed to bandpass filter the receiver input frequency while rejecting the transmitter frequency. The tuned preamp also improves the noise performance by reducing the bandwidth of the pass band and reducing the second stage contribution of the 1st mixer. The preamp is biased at about 1.0 mA and 3.0 Vdc which yields suitable noise figure and gain.

Mixers

The 1st and 2nd mixers are similar in design. Both are double balanced to suppress the LO and the input frequencies to give only the sum and difference frequencies out. Typically the LO is suppressed about 40 to 60 dB. The 1st mixer may be driven either differentially or single ended. The gain of the 1st mixer has a 3.0 dB corner at 20 MHz and is used at a 10.7 MHz IF. It has an output impedance of 330 Ω and matches to a typical 10.7 MHz ceramic filter with a source and load impedance of 330 Ω. A series resistor may be used to raise the impedance for use with crystal filters which typically have an input impedance much greater than 330 Ω. The 2nd mixer input impedance is typically 3.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard 330 Ω 10.7 MHz ceramic filter. The second mixer output impedance is 1.5 kΩ making it suitable to match 455 kHz ceramic filters.

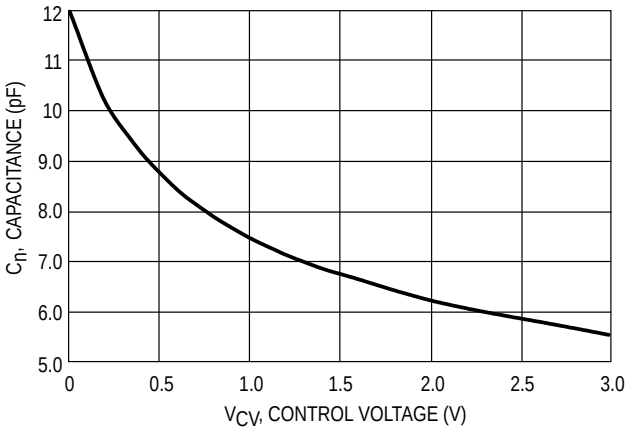
The following table is a list of typical input impedances over frequency for the 1st Mixer. R_P and C_P are represented in parallel form.

Frequency (MHz)	R_P (Ω)	C_P (pF)
20	977.7	2.44
25	944.3	2.60
30	948.8	2.65
35	928	2.55
40	900	2.51
45	873.4	2.65
50	859.3	2.72
55	821	2.72
60	795	2.74

First Local Oscillator

The 1st LO is a multi–vibrator oscillator that takes an external capacitance and inductance. It is voltage controlled to an internal varactor from an external loop filter and an on–board phase–lock loop (PLL). The schematic in Figure 33 shows all the basic parasitic elements of the internal circuitry. The 1st LO internal component values have a tolerance of 15%. A typical dc bias level on the LO Input and LO Output is 0.47 Vdc. The curve in Figure 38 is the varactor control voltage range as it relates to capacitance. It represents the expected capacitance for a given control voltage of the MC13110.

Figure 38. First Local Oscillator Varacter versus Control Voltage



Second Local Oscillator

The 2nd LO is a CMOS oscillator similar to that used in the MC145162. The 2nd LO is also used as the PLL reference oscillator. It is designed to utilize an external parallel resonant crystal.

PLL Design

The 1st LO level is important, as well as the choice of the crystal for the PLL clock reference and 2nd LO. A fundamental, parallel resonant crystal specified with 7.0 to 12 pF load calibration capacitance is recommended. With load calibration capacitance too high, the crystal locks up very slowly. If the LO power is less than –10 dBm, a pull–down resistor at the 1st LO emitter (Pin 41) will increase its drive level. The LO level is primarily a function of the Colpitts capacitive voltage divider formed by the capacitors between the base to emitter and the emitter to ground.

The VCO gain factor expressed in MHz/V is indeed critical to the phase noise performance. If this curve is too steep or too sensitive to changes in control voltage, it may degrade the phase noise performance. The external VCO circuit design needs to consider the typical swing of the control voltage and the corresponding linearity of the transfer function, $\Delta f_{osc}/\Delta V_{control}$. In general, the higher the Q of the VCO circuit inductor, the better phase noise performance.

Adjacent channel rejection and isolation between the 1st and 2nd mixers may be adversely affected due to layout problems and difficulty in getting close to the package pins with the grounds and decoupling capacitors on the RF V_{CC}. These system parameters must be evaluated for sensitivity to layout and external component placement.

Intermodulation and adjacent channel performance problems may also result from spurs around the 1st LO which may be caused by harmonics from the switched capacitor clock driver and too low 1st LO drive level. The clock driver operates at a frequency which is f(2nd LO)/(2 * (SCF Divider)). The harmonics are n * (f(2nd LO)), where n can be any positive integer. The current spikes of the SCF on the supply lines cause the disturbance of the 1st LO. This may be verified by observing the spurs on a spectrum analyzer while changing the clock divider value. The spur frequencies will change when the divider value is changed. The spurious sideband problem may be avoided by changing the clock divider value via software for each channel where it is a problem. Certain channels are worse than others.

The PLL alignment procedure for the application circuit is detailed in Appendix C. Refer to the MC145162 data sheet for PLL design example.

Limiting IF Amplifiers

The limiting IF amplifier typically has about 110 dB of gain; the frequency response starts rolling off at 1.0 MHz. Decoupling capacitors should be placed close to the decoupling Pins 31 and 32 to ensure low noise and stable operation. The IF input impedance is 1.5 kΩ for a suitable match to 455 kHz ceramic filters.

RSSI/Carrier Detect

The Received Signal Strength Indicator (RSSI) indicates the strength of the IF level and the output is proportional to the logarithm of the IF input signal magnitude. The RSSI dynamic range is typically 80 dB. Connect 0.01 µF to GND from “RSSI” output pin to form the carrier detect filter. A resistor needed to convert the RSSI current to voltage is included in the internal circuit. An internal temperature compensated reference current also improves the RSSI accuracy over temperature.

“CD Out” is an open collector output; thus, an external 100 kΩ pull–up resistor to V_{CC} is recommended. The carrier detect threshold is programmable through the MPU interface.

Quadrature Detector

The quadrature detector is coupled to the IF with an external capacitor between Pins 27 and 28; thus, the recovered signal level output is increased for a given bandwidth by increasing the capacitor. The external quadrature component may be either a LCR resonant circuit, which may be adjustable, or a ceramic resonator which is usually fixed tuned.

The bandwidth performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit’s bandwidth:

$$(1)\quad R_T = Q\,X_L$$

where R_T is the equivalent shunt resistance across the LC Tank. X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

Specific 455 kHz quadrature LC components are manufactured by Toko in various 5 mm, 7 mm and 10 mm shielded cans in surface mount or leaded packages. Recommended components such as, the 7 mm Toko, is used in the application circuit. When minaturization is a key constraint, a surface mount inductor and capacitor may be chosen to form a resonant LC tank with the PCB and parasitic device capacitance. The 455 kHz IF center frequency is calculated by

$$(2)\quad f_c = [2\pi\,(LC_p)^{1/2}] - 1$$

where L is the parallel tank inductor. C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a detector at 455 kHz and a specific loaded Q. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 455 kHz and an IF bandpass of 20 kHz, the IF bandpass Q is approximately 23; the loaded Q of the quadrature tank is chosen at 15.

Example:

Let the total external C = 180 pF. Note: the capacitance may be split between a 150 pF chip capacitor and a 5.0 to 25 pF variable capacitor; this allows for tuning to compensate for component tolerance. Since the external capacitance is much greater than the internal device and PCB parasitic capacitance, the parasitic capacitance may be neglected.

Rewrite equation (2) and solve for L:

$L = (0.159)^2/(C\ fc^2)$
$L = 678\ \mu H$; Thus, a standard value is chosen:
$L = 680\ \mu H$ (surface mount inductor)

The value of the total damping resistor to obtain the required loaded Q of 15 can be calculated from equation (1):

$R_T = Q(2\pi fL)$
$R_T = 15\ (2\pi)(0.455)(680) = 29.5\ k\Omega$

The internal resistance, R_{int} at the quadrature tank Pin 27 is approximately 100 kΩ and is considered in determining the external resistance, R_{ext} which is calculated from

$R_{ext} = ((R_T)(R_{int}))/(R_{int} - R_T)$
$R_{ext} = 41.8\ k\Omega$; Thus, choose the standard value:
$R_{ext} = 39\ k\Omega$

A ceramic discriminator is recommended for the quadrature circuit in applications where fixed tuning is desired. The ceramic discriminator and a 22 k resistor are placed from Pin 27 to V_{CC}. A 10 pF capacitor is placed from Pin 28 to 27 to properly drive the discriminator.

MuRata Erie has designed a resonator that is compatible with the IC. For US applications the part number is CDBM455C48. For Europe the part number is CDBM450C48. Contact Motorola Analog Marketing for performance data using muRata's parts.

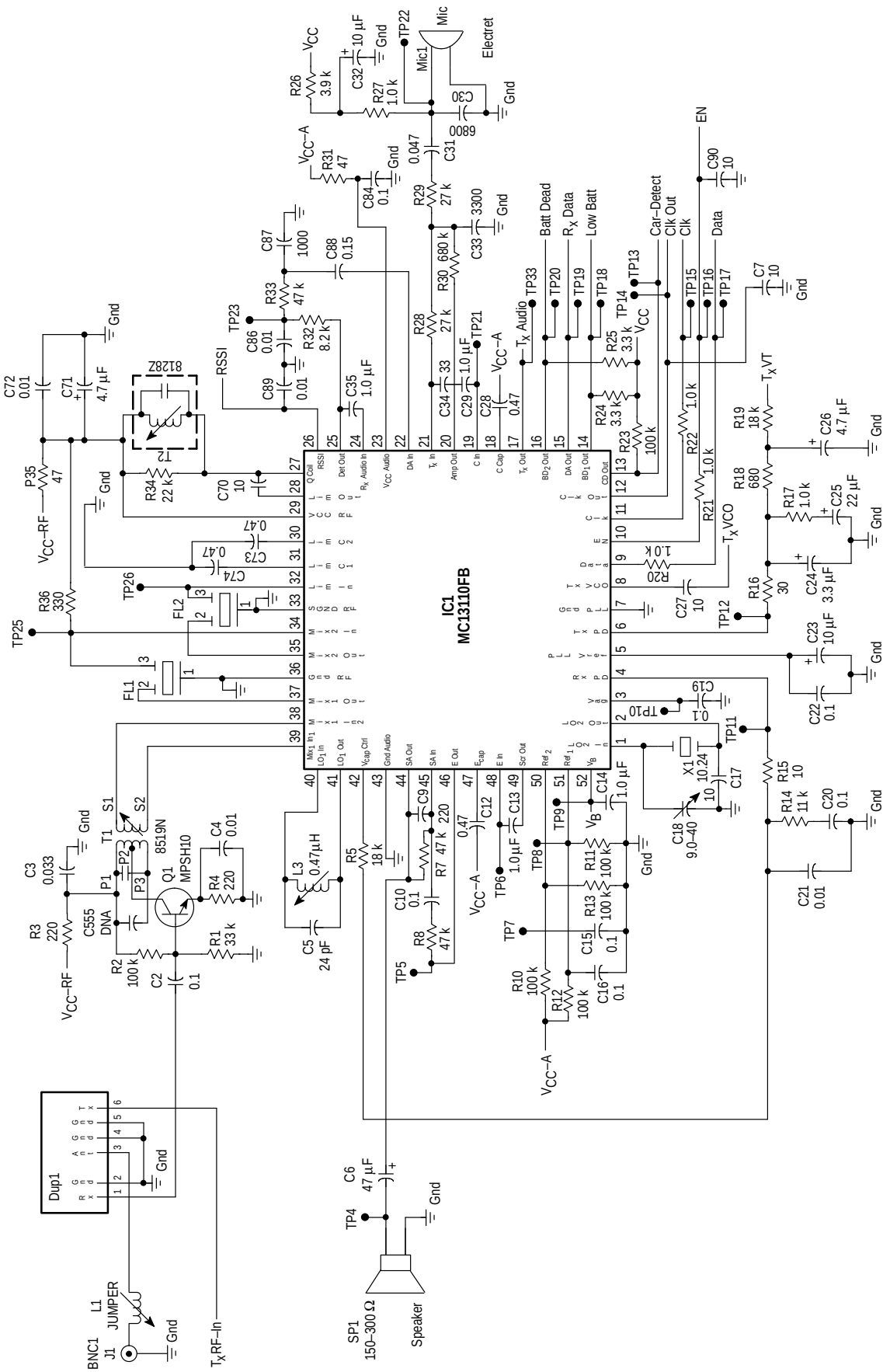
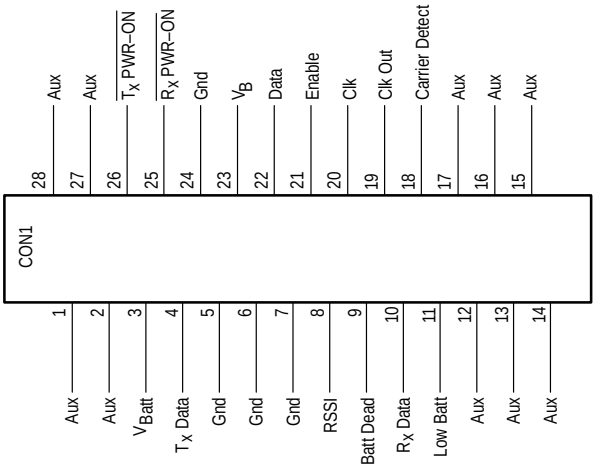
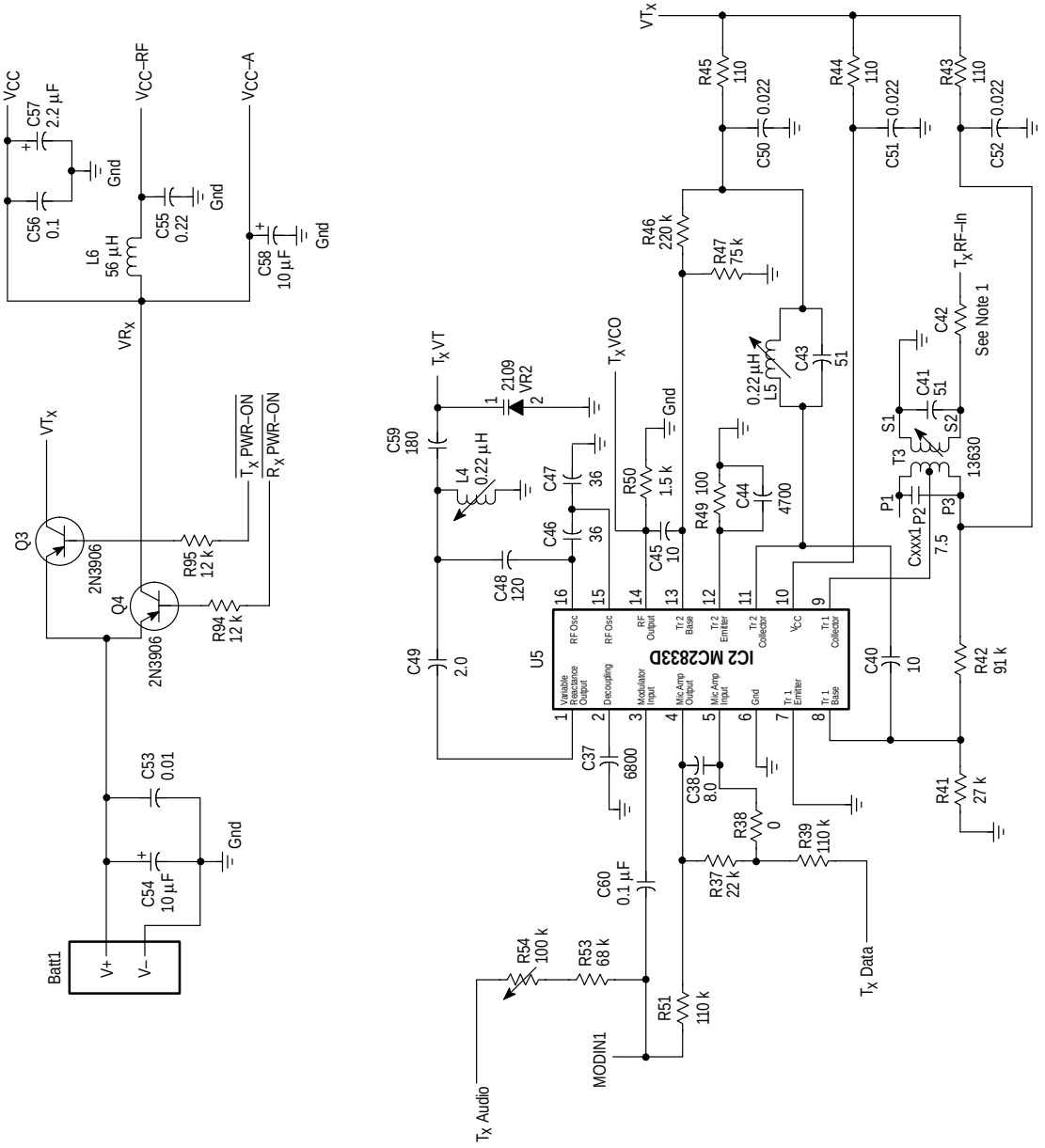


Figure 39a. Baseset RF Applications Circuit





NOTE 1: C42 = X42 = 51 Ω

Figure 39a. Baseset RF Applications Circuit (continued)

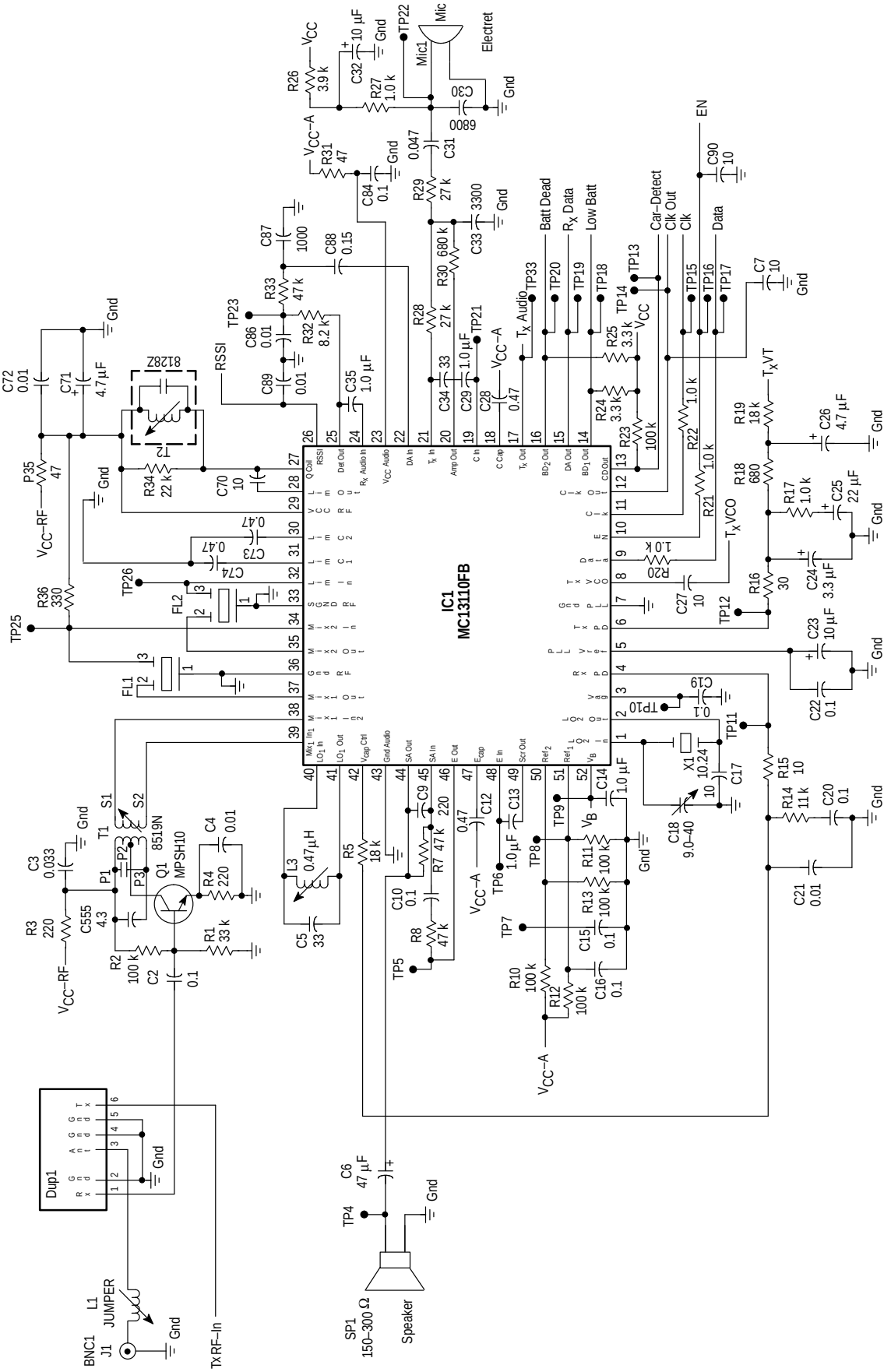


Figure 39b. Handset RF Applications Circuit

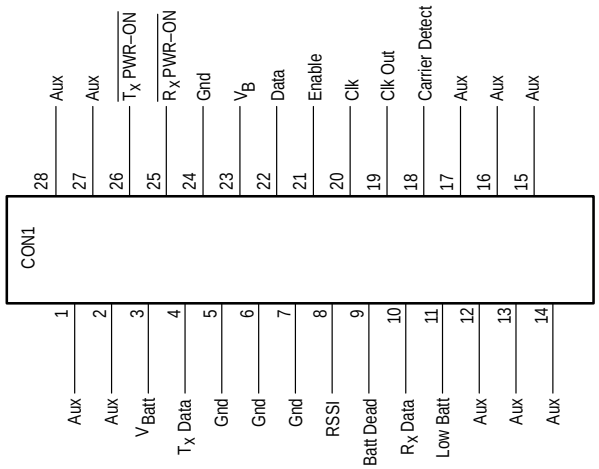
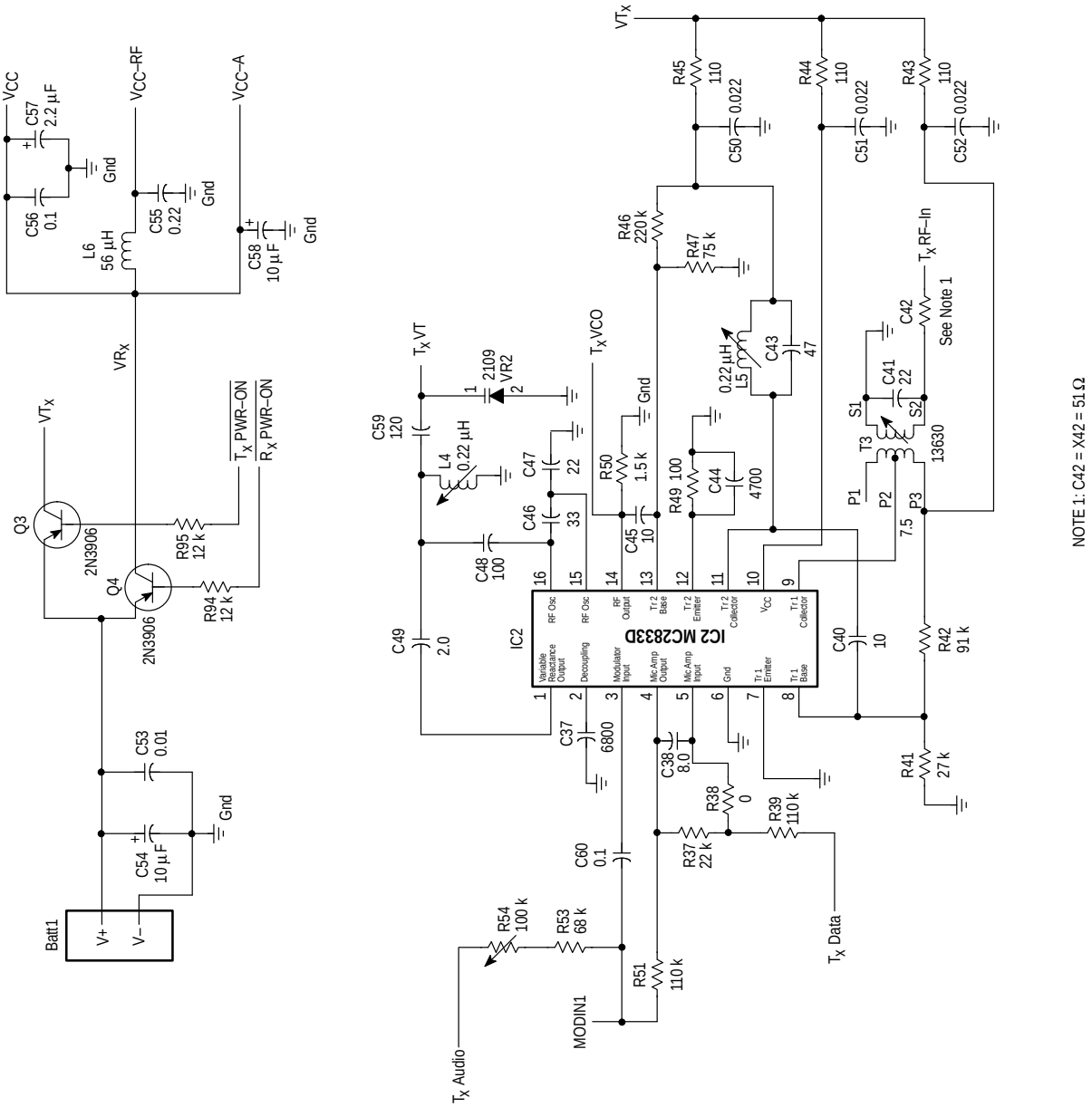


Figure 39b. Handset RF Applications Circuit (continued)



NOTE 1: C42 = X42 = 51 Ω

APPENDIX B – MC13110 APPLICATION BOARD BILL OF MATERIAL (USA)

Reference	Description	Value	Package	Part Number	Vendor
X1	10.24 Crystal (Load Cap <12 pF)	–	HC49US	AAL10M240000FLE10A	Standard Crystal
VR2	Diode	–	Sot23	MMBV2109LT1	Motorola
DUP1	Duplexer (25 Channel)	Baseset	Hybrid	DPX1035 75B–153B	Sumida
DUP1	Duplexer (25 Channel)	Handset	Hybrid	DPX1035 75B–154B	Sumida
FL1	10.7 MHz Filter (Red Dot)	–	–	SFE10.7MS2–A	muRata
FL2	455 kHz Filter	–	–	CFU455E2	muRata
IC1	Universal Cordless Telephone IC	–	QFP	MC13110FB	Motorola
IC2	FM Transmitter IC	–	SO–16	MC2833D	Motorola
L3	Inductor	0.47 μH	Can	292SNS–T1370Z	Toko
L4/L5	Inductor	0.22 μH	Can	292SNS–T1368Z	Toko
T1/T3	Transformer	–	Can	600GCS–8519N	Toko
T2	Quadrature Coil	–	Can	7MCS–8128Z	Toko
Q1	Transistor	–	TO–92	MPSH10	Motorola
Q3	Transistor	–	TO–92	2N3906	Motorola
Q4	Transistor	–	TO–92	2N3906	Motorola

NOTE: Components for the Handset and Baseset are the same, except where noted on the Bill of Material and Schematic.

APPENDIX C – MEASUREMENT OF COMPANDOR ATTACK/DECAY TIME

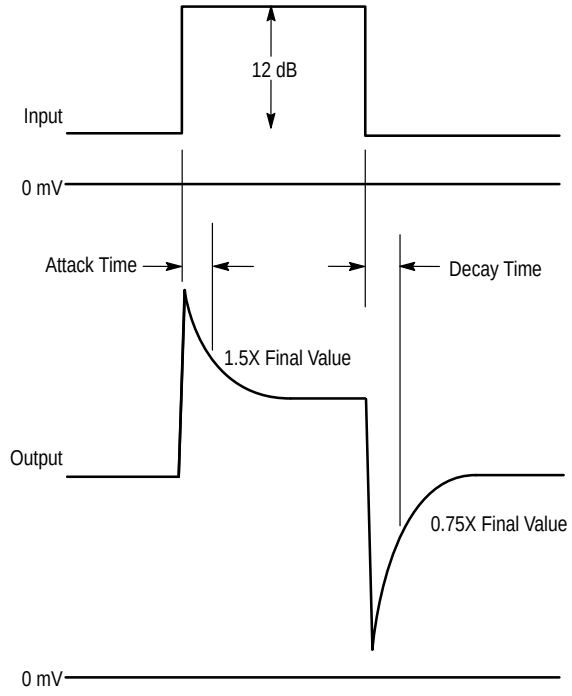
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

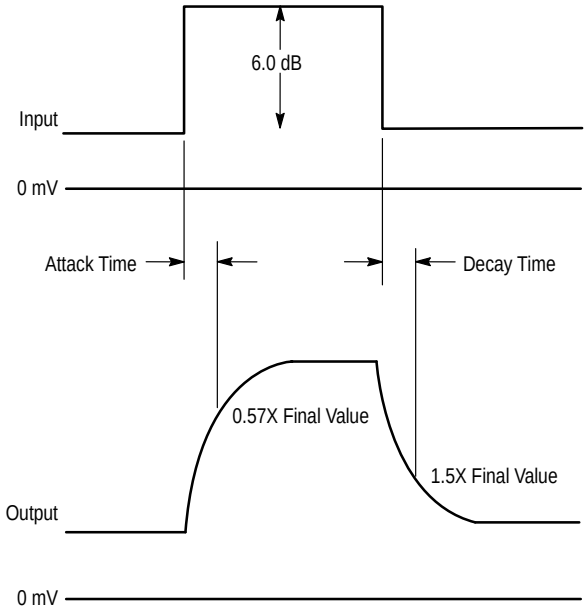


Expandor Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

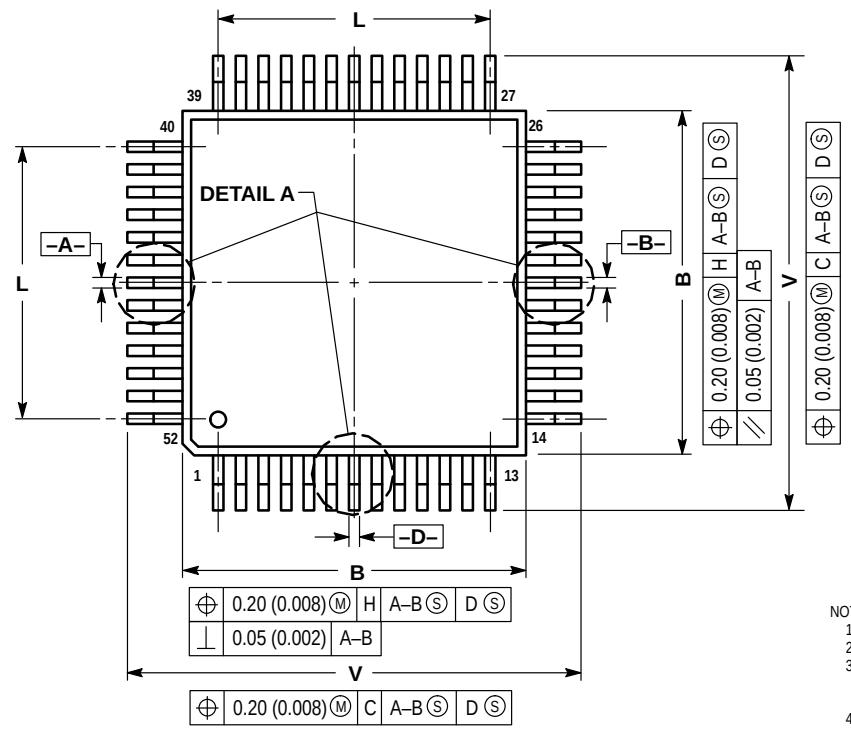
Expandor Decay

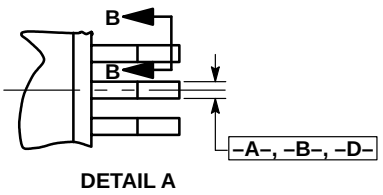
For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



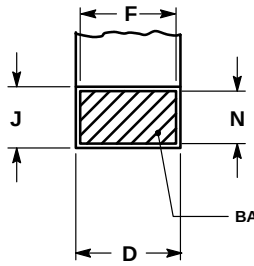
OUTLINE DIMENSIONS

FB SUFFIX
PLASTIC QFP PACKAGE
CASE 848B–04
ISSUE C



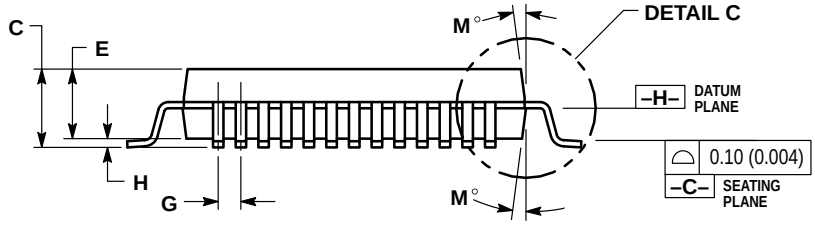


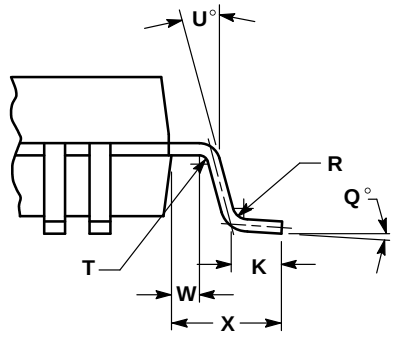
DETAIL A



0.02 (0.008) M C A–B S D S

SECTION B–B





DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

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JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

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