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MOTOROLA

MC13017

Product Preview

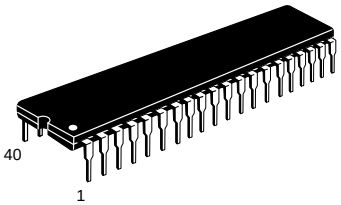
NTSC/PAL Chroma 10 Color TV and Timebase Processor

The MC13017 consists of all the necessary circuits for TV NTSC/PAL decoding and timebase processing. It forms a kit set with the MC44301 VIF and the TDA3190 Sound IF and Power for a low cost, high performance CTV system.

- On–Chip Sync Separator
- Dual Loop Horizontal Timebase
- Direct Locked Vertical Counter
- X–Ray Protection
- Noise Blanking on Sync Separator
- NTSC/PAL Color Decoding
- Direct Interface with SECAM TDA3030B
- 4.43/3.579 MHz Crystal Reference
- Three DC High Impedance Control Outputs for Contrast, Brightness, and Saturation
- 12 V Supply
- Vertical Ramp Buffer Output
- Sandcastle Output
- Hue Control

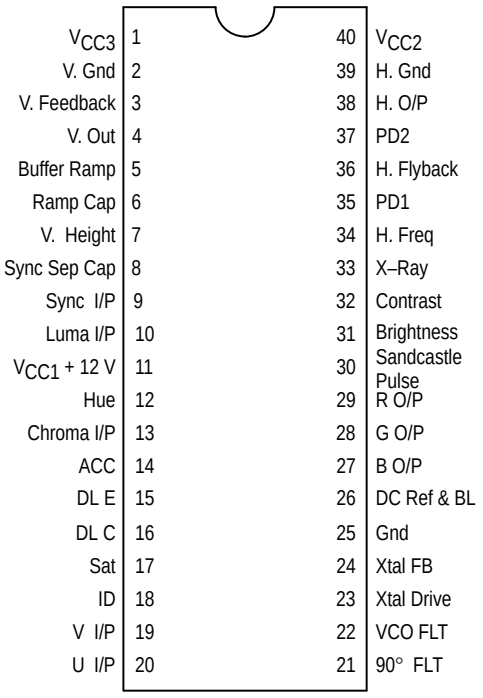
NTSC/PAL CHROMA 10 COLOR TV and TIMEBASE PROCESSOR

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1}, V_{CC3} V_{CC2}	15 10	V
Operating Temperature Range	T_A	0 to +70	5C
Storage Temperature Range	T_{stg}	– 55 to +125	°C
Horizontal Output Voltage Vertical Output Voltage	V_{OH} V_{OV}	8.0 4.0	V

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13017P	T_A = 0° to +70°C	Plastic DIP

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PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	V_{CC3}	+12 V supply for V_{CC2} power regulator.
2	Vert Gnd	Vertical output analog ground.
3	Vert Feedback	The Ramp on Pin 6 is internally inverted, level shifted and subtracted from the input to Pin 3. The result appears as an output on an open collector at Pin 4.
4	Vert Out	Vertical ramp output to external vertical power drive.
5	Buffer Ramp	The vertical buffer ramp output of Pin 6.
6	Ramp Cap	The external cap is charged by a current controlled through vertical height control Pin 7 to produce a vertical ramp. The discharge of the cap is controlled internally by the vertical counter.
7	Vert Height	Current input for vertical height control.
8, 9	Sync Sep Cap, Sync I/P	Sync separator input is a NPN transistor stage with the signal presented at its base with a peak level of about 4.0 V. The emitter is brought out to Pin 8 through a 200 Ω resistor so that a capacitor with a series resistor may be connected. The circuit behaves as a peak detector with a slicing level controlled by the choice of charge and discharge resistors. An additional time constant is connected through a diode to prevent the slice level from riding up on the field sync.
11	V_{CC1}	+12 V supply for chroma.
12	Hue	This is Hue control for NTSC system. It should be connected to V_{CC1} at PAL system. When voltage at Pin 12 is smaller than 8.0 V, NTSC mode is selected.
15	DL E	Delay line drive open emitter terminal.
16	DL C	Delay line drive open collector terminal.
18	ID Filter	An external filter cap is connected at this pin for ID circuit.
19, 20	V, U	V, U inputs after delay line to detectors.
21	90° Filter	90° phase shifter filter.
22	VCO Filter	Color reference VCO filter.
23 24	Xtal 2 Xtal 1	A 4.43 MHz (PAL), or 3.579 MHz (NTSC) crystal is connected to the internal VCO for color subcarrier reference frequency.
30	Sandcastle Pulse Output	The Sandcastle Pulse Output is delivered through 200 Ω from an emitter–follower with 10 kΩ pull–down. The blanking duration is determined by the applied flyback pulse. The burst gate determined by the second half of the flyback levels are: Blanking (4.0 V), Burst Gate (11 V).
35	PD1	Horizontal phase detector current output. The PLL 1 is locked to the sync input with 2H oscillator.
36	Horiz Flyback	Horizontal flyback, a positive input pulse exceeded threshold of 1.0 V is required, input impedance is between 600 and 2.0 kΩ so that a minimum of 0.5 mA current is needed to exceed the threshold voltage. The recommended peak current is 2.0 mA.
37	PD2	Second horizontal phase detector current output. The function of PLL 2 is to adjust the horizontal drive in order to maintain the flyback in phase with the oscillator.
38	Horiz Out	This is a saturated NPN transistor with a 2.0 kΩ internal load to regulate supply V_{CC2}.
39	Horiz Gnd	Horizontal analog output grounding should be connected nearby the external horizontal output stage.
40	V_{CC2}	Regulated supply to horizontal timebase section. A diode is in series with 270 Ω from V_{CC3} + 12 V to block the high voltage startup supply of 10 mA for horizontal oscillator.

OUTLINE DIMENSIONS

P SUFFIX
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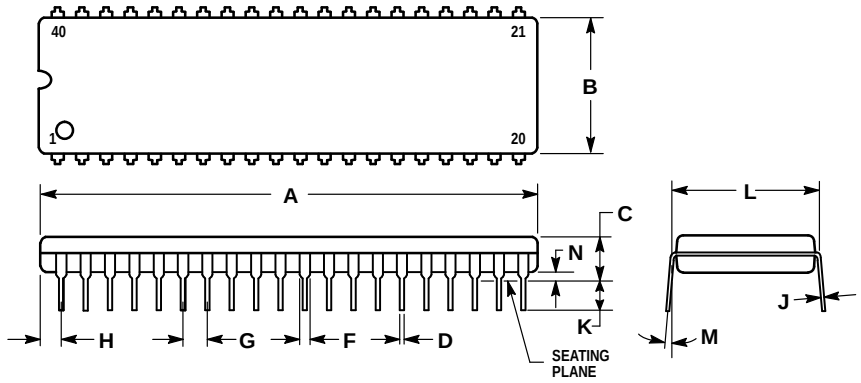
CASE 711–03
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15°	0 °	15°
N	0.51	1.02	0.020	0.040

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