Product Preview

Low Voltage Dual RF/IF PLL Frequency Synthesizer

MC12306

2.0GHz/500MHz LOW VOLTAGE DUAL PLL FREQUENCY SYNTHESIZER

The MC12306 is a 2.0GHz (RF)/500MHz (IF) monolithic serial input dual phase locked loop (PLL) synthesizer. The device contains a complete RF prescaler/PLL synthesizer and an IF prescaler/PLL synthesizer. It is designed to provide the high frequency RF local oscillator control and IF oscillator control for dual conversion receivers or transceivers. The two synthesizers share a common serial programming port as well as the reference oscillator input. Each side contains separate reference counters for independent programming of the comparison frequency. The device is intended for RF personal communication applications where small size and low power are critical.

Motorola's advanced Bipolar MOSAIC V technology is utilized for low power operation at a minimum supply voltage of 2.7V. The device is designed for operation over a 2.7 to 5.5V supply range for input frequencies up to 2.0GHz/500 MHz with a typical current drain of 10.5mA. The low power consumption makes the MC12306 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or GPS receivers. Dual modulus prescalers are integrated to provide either a 32/33 or 64/65 divide ratio for the RF synthesizer and a 8/9 or 16/17 divide ratio for the IF synthesizer.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

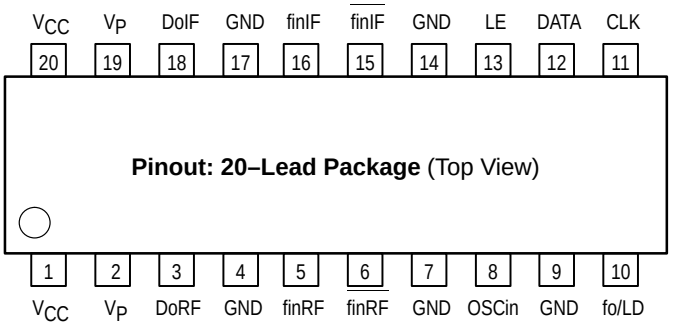
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02

- Low Power Supply Current of 10mA Typical for I_{CC} and 0.5mA Typical for I_P
- Supply Voltage of 2.7 to 5.5V
- Dual Modulus Prescaler With Selectable Divide Ratios of 32/33 or 64/65 for the RF Synthesizer and 8/9 or 16/17 for the IF Synthesizer
- On–Chip Reference Frequency Buffer
- Two Programmable Reference Dividers Consisting of a Binary 14–Bit Reference Counter (R = 8 to 16383)
- Two Programmable Dividers Consisting of a Binary 6–Bit (4 Bit for IF) Swallow Counter and an 11–Bit Counter
- Integrated Digital Phase/Frequency Detectors
- Balanced Charge Pump Outputs Which Can Be Disabled Individually Under Software Control
- Multi–function Test Pin for Observing RF or IF Lock Detect Output or Any One of Four Comparison Signals
- Test Pin Can Be Disabled Under Software Control to Reduce Current Drain
- Operating Temperature Range of –40°C to +85°C
- Space Efficient Plastic Surface Mount TSSOP Package

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage, Pins 1 and 20	–0.5 to +6.0	VDC
V_P	Power Supply Voltage, Pins 2 and 19	V_{CC} to +6.0	VDC
Tstg	Storage Temperature Range	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.



CASE 948E
ACTUAL SIZE

PIN NAMES

Name	I/O	Function
OSCin	I	Reference oscillator input. An external oscillator source must be ac coupled in to this pin
V_P	–	Power supply for charge pumps. V_P should be greater than or equal to V_{CC}. Separate pins (Pin 2 for RF/Pin 19 for IF) supply the charge pump circuitry
V_{CC}	–	Power supply voltage input. Bypass capacitors should be placed close to this pin and connected directly to the ground plane. Separate pins (Pin 1 for RF/Pin 20 for IF) supply the internal circuitry. Both V_{CC} voltages must be equal
Do RF	O	Internal charge pump output for RF synthesizer, can be disabled under SW control
Do IF	O	Internal charge pump output for IF synthesizer, can be disabled under SW control
GND	–	Ground
fo/LD	O	Multi–function digital output. This output is selectable as fr–RF, fr–IF, fv–RF, fv–IF, Lock–RF or Lock–IF under software control
fin RF	I	Prescaler input for the RF synthesizer. The high–frequency VCO output signal is ac–coupled into this pin
$\overline{\text{fin RF}}$	I	Complementary prescaler input for the RF synthesizer. This pin is ac–bypassed to ground
fin IF	I	Prescaler input for the IF synthesizer. The low frequency VCO output signal is ac–coupled into this pin
$\overline{\text{fin IF}}$	I	Complementary prescaler input for the IF synthesizer. This pin is ac–bypassed to ground
CLK	I	Clock input. Rising edge of clock shifts data into the shift registers
DATA	I	Binary serial input data
LE	I	Load Enable input. When LE pulses high, data stored in the shift registers is transferred into the appropriate latch (depending on the status of the control bits). In addition, while LE is high, the CLK input is disabled

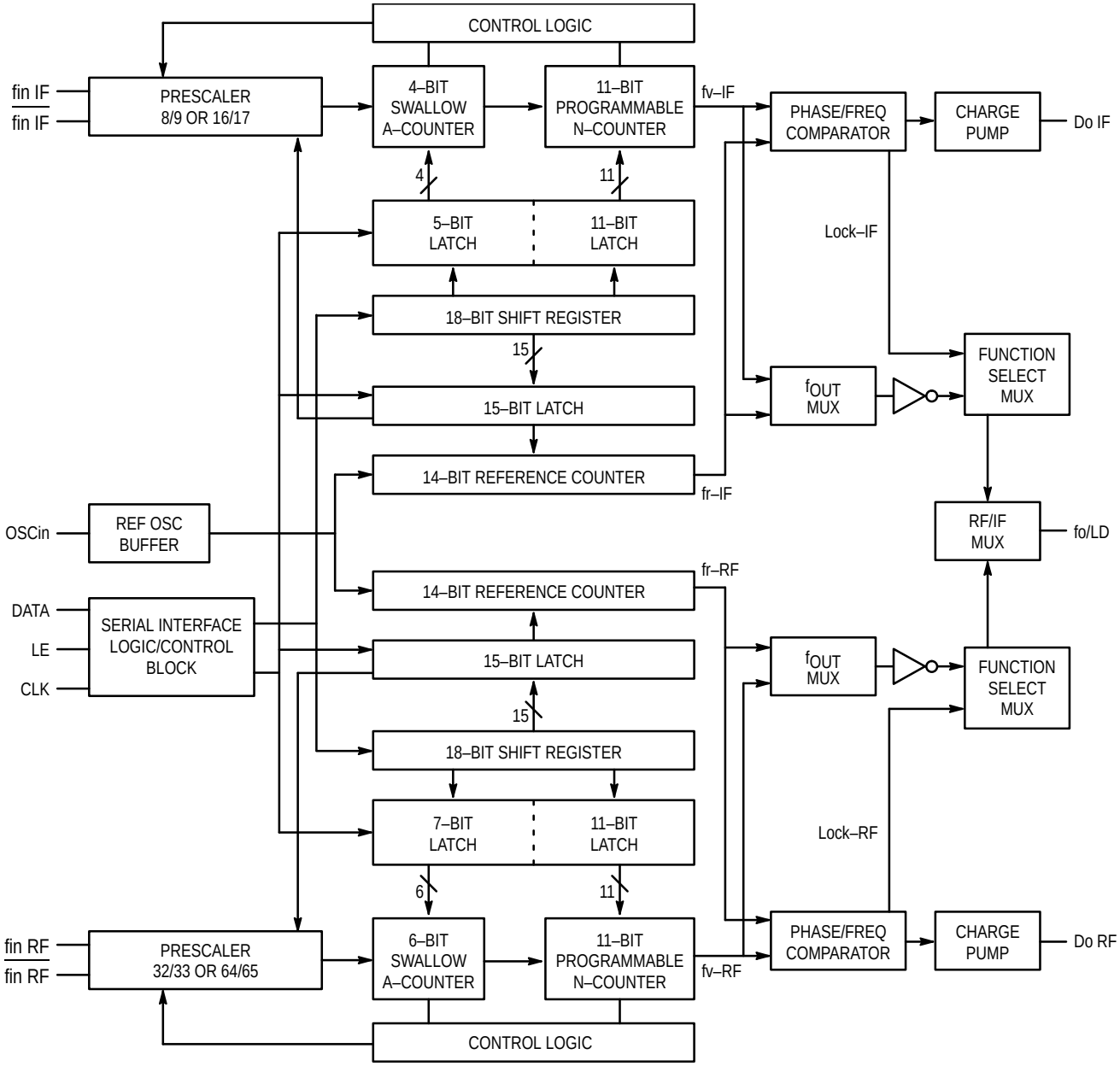


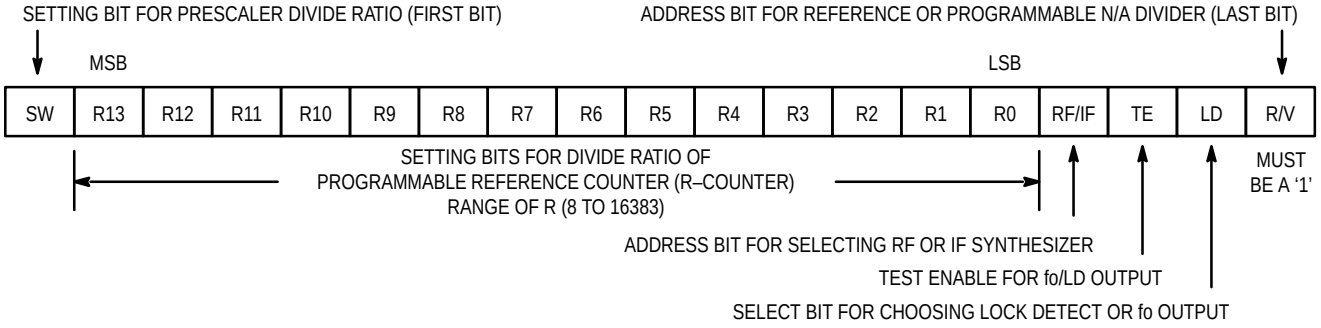
Figure 1. MC12306 Functional Block Diagram

SERIAL PROGRAMMING INTERFACE

A simple 3–line uni–directional serial interface is used to program the synthesizer. The interface consists of DATA , CLK (clock), and LE (load enable) inputs. While the LE input is LOW, a rising edge of the clock shifts one bit of serial data into the internal shift registers. The most significant bit (MSB) is shifted in first (SW). The last bit is a control bit which steers the data stream to either the Reference Divider (19 bits) or Programmable N/A Divider (22 bits) Latch. When the LE input pulses HIGH, the contents shifted in will be latched into the device. Only the last 19 bits (or 22–bits) serially clocked into the device are retained. Additional leading bits are ignored. This is useful in those cases where the programmer prefers to deal with bit streams which are multiples of a byte in length.

PROGRAMMABLE REFERENCE DIVIDER

A 19–bit serial data format is used to access the programmable reference counter and prescaler select bit. There are 3 separate fields in this data format which are illustrated below. The first field is 1–bit wide (SW) and selects one of the two modulus prescalers. A HIGH selects the lower modulus prescaler pair while LOW selects the higher modulus prescaler pair. The next field is 14–bits wide and contains the value of the reference counter divide ratio. The final field is 4–bits wide and is used for addressing and control. The first bit in this field is RF/IF, which selects whether the data is going to be latched into the RF section (1=RF) or the IF section (0=IF). The next bit, Test Enable (TE) controls the multi–function fo/LD output (1=Active). When this bit is disabled (0=TE), the output circuitry is shut off to conserve power. The next bit, Lock Detect (LD) controls whether the lock detector signal (1=Lock) or the fout (0=fout) is routed to the fo/LD output. The final bit is a control bit R/V which must be set high (1=R/V) to address the data stream to the Reference Divider.



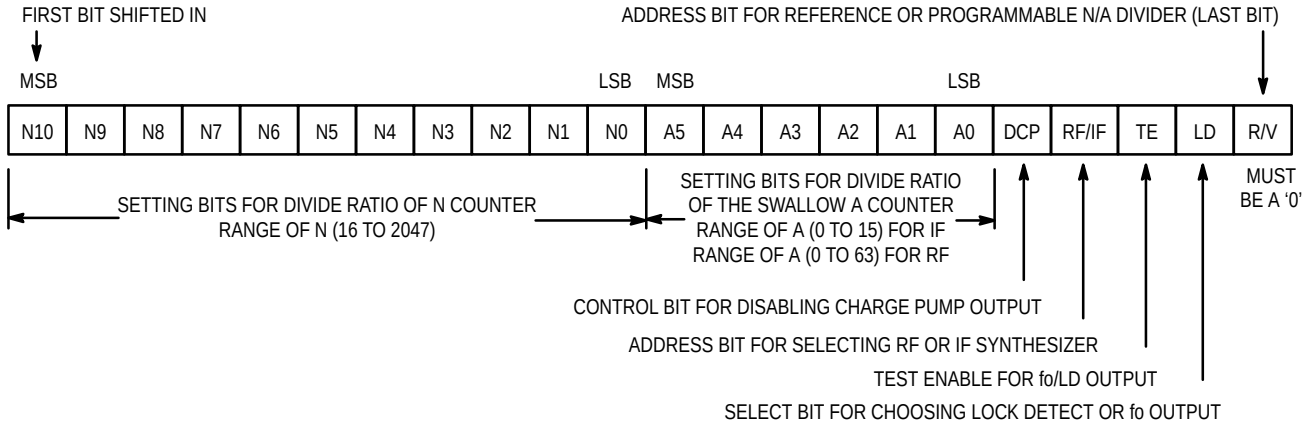
DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER

Divide Ratio R	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1	R 0
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

PRESCALER SELECT BIT			SYNTHESIZER SELECT BIT		TEST ENABLE BIT		LD SELECT BIT	
Synthesizer	**Prescaler Divide Ratio**	**SW**	**Synthesizer**	**RF/IF**	**Status of fo/LD**	**TE**	**Signal From fo/LD**	**LD**
RF RF	64/65 32/33	0 1	IF	0	Powered Down	0	f_{OUT}	0
IF IF	16/17 8/9	0 1	RF	1	Active	1	Lock Detect	1

PROGRAMMABLE N/A DIVIDER

A 22–bit serial data format is used to access the N Divider, A Divider, and some test control functions. There are 4 separate fields in this data format which are illustrated below. The first field is 11–bits wide and is used to program the N–counter. The next field is 6–bits wide and is used to program the A–counter. The next field (DCP) is 1–bit wide and it is used to enable and disable the charge pump output. If the field is set (1=DCP), the addressed charge pump is placed in a high–impedance state. In normal operation, the charge pump is enabled (0=DCP). The final field is 4–bits wide and is used for addressing and control. The first bit in this field is RF/IF, which selects whether the data is going to be latched into the RF section (1=RF) or the IF section (0=IF). The next bit, Test Enable (TE) controls the multi–function fo/LD output (1=Active). When this bit is disabled (0=TE), the output circuitry is shut off to conserve power. The next bit Lock Detect (LD) controls whether the lock detector signal (1=Lock) or the fout (0=fout) is routed to the fo/LD output. The final bit is a control bit R/V which must be set low (0=R/V) to address the data stream to the Programmable N/A Divider.



NOTE: When programming the A–counter for the IF loop, A4 and A5 should be set to '0'.

DIVIDE RATIO OF PROGRAMMABLE N–COUNTER **DIVIDE RATIO OF SWALLOW A–COUNTER**

Divide Ratio N	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1	N 0	Divide Ratio A	A 5	A 4	A 3	A 2	A 1	A 0
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1	63	1	1	1	1	1	1

SYNTHESIZER SELECT BIT		TEST ENABLE BIT		LD SELECT BIT		CHARGE PUMP CONTROL BIT	
Synthesizer	**RF/IF**	**Status of fo/LD**	**TE**	**Signal from fo/LD**	**LD**	**Do Output Status**	**DCP**
IF	0	Powered Down	0	f_{OUT}	0	Normal Operation	0
RF	1	Active	1	Lock Detect	1	Disabled	1

PROGRAMMING ORDER

There is no specific order by which the data words must be programmed for normal operation. In most applications, the RF and IF Programmable Reference Divider words are programmed first and the Programmable N/A Divider words are programmed last. The Programmable N/A Divider words are then changed as the synthesizer is tuned to different channels. It is important to note that the status of the TE and LD fields of the last word programmed determines the state of the fo/LD output.

PROGRAMMING THE STATE OF THE fo/LD OUTPUT

The multi–function test pin output can be used to observe any one of six internal signals: fr–RF, fr–IF, fv–RF, fv–IF, Lock–RF, and Lock–IF. In addition this output pin can be disabled to reduce current consumption of the part and minimize switching noise. All these functions are under software control. To fully configure the synthesizer, four data words must be programmed into the device to load all the latches. As previously stated, programming order is not important for normal operation. This is not the case though when the user would like to observe a test point. Under this condition, the last word loaded determines what test point will be observed. The table below illustrates which register needs to be programmed last and the state of the control bits to access each test point.

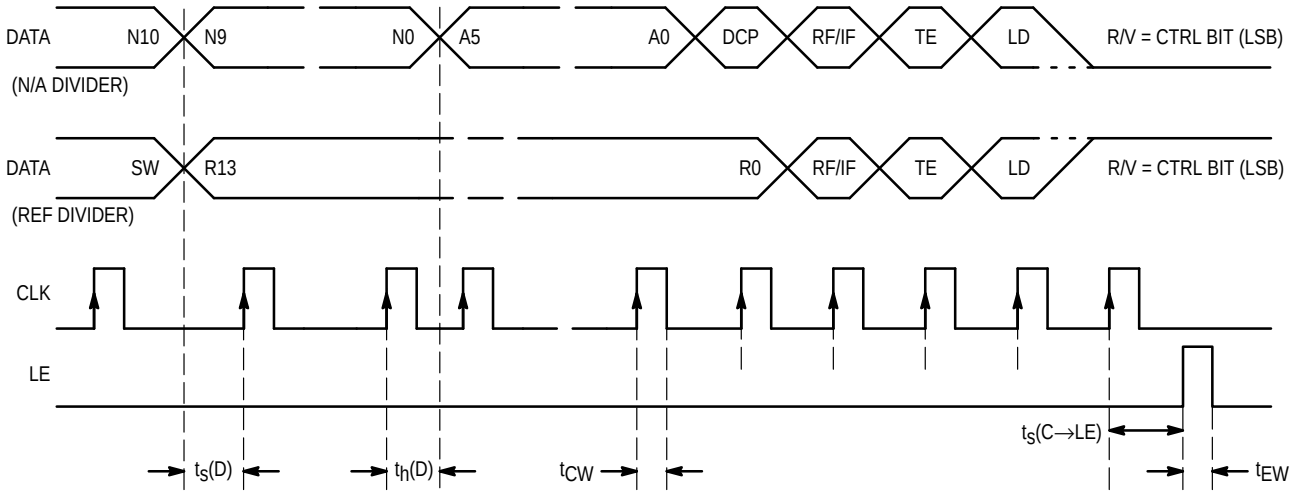
fo/LD Output	Register	R/V	RF/IF	TE	LD
fr IF	Reference Divider	1	0	1	0
fv IF	N/A Divider	0	0	1	0
Lock IF	Either	X	0	1	1
fr RF	Reference Divider	1	1	1	0
fv RF	N/A Divider	0	1	1	0
Lock RF	Either	X	1	1	1
Disabled	Either	X	X	0	X

X = Don't Care

DIVIDE RATIO SETTING

fvco = [(P•N)+A]•fosc ÷ R with A ≤ N (for continuous frequency steps P•N+A ≥ P(P–1))

- fvco: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11–bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 4–bit or 6–bit swallow counter (0 to 63, A≤N, for RF synthesizer; 0 to 15, A≤N, for IF synthesizer)
- fosc: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14–bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (32 or 64 for RF synthesizer; 8 or 16 for IF synthesizer)



NOTE:Data shifted into register on rising edge of CLK.

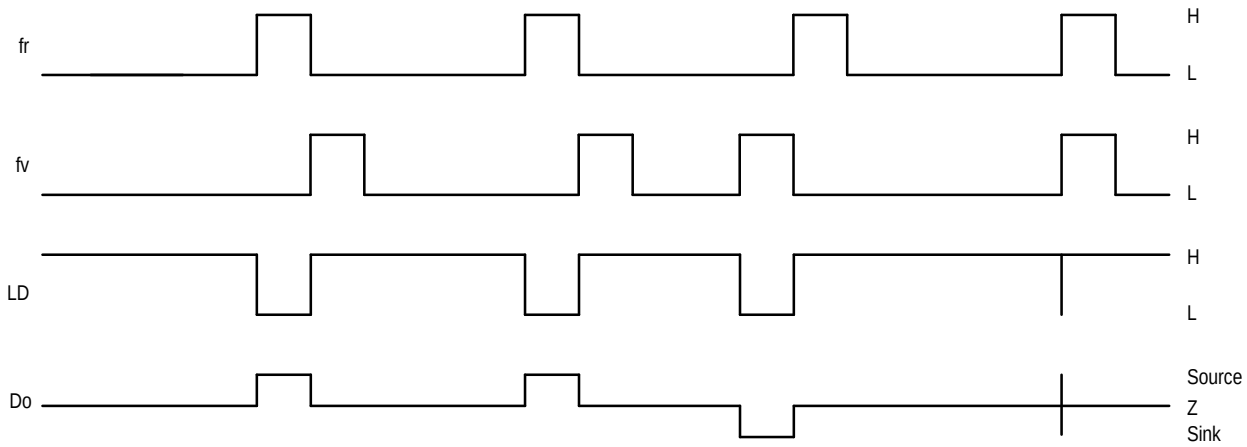
$t_S(D)$ = Setup Time DATA to CLK	$t_S(D) \geq 10ns$
$t_h(D)$ = Hold Time DATA to CLK	$t_h(D) \geq 20ns$
t_{CW} = CLK Pulse Width	$t_{CW} \geq 30ns$
t_{EW} = LE Pulse Width	$t_{EW} \geq 20ns$
$t_S(C \rightarrow LE)$ = Setup Time CLK to LE	$t_S(C \rightarrow LE) \geq 30ns$

Figure 2. Serial Data Input Timing

PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12306 is a high speed digital phase/frequency detector circuit. The circuit determines the “lead” or “lag” phase relationship and time difference between the leading edges of the VCO (fv) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

The operation of the phase comparator is shown in NO TAG.



NOTES: Do is a current output.
Phase difference detection range: -2π to $+2\pi$
The spike is output in order to diminish dead band.

$$\text{Internal Charge Pump Gain} \approx \frac{|I_{source}| + |I_{sink}|}{4\pi} = \frac{4mA}{4\pi}$$

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms

fr lags fv in phase OR fv>fr in frequency

When the phase of fr lags that of fv or the frequency of fv is greater than fr, the Do output will sink current. The pulse width will be determined by the time difference between the two rising edges.

fr leads fv in phase OR fv<fr in frequency

When the phase of fr leads that of fv or the frequency of fv is less than fr, the Do output will source current. The pulse width will be determined by the time difference between the two rising edges.

fr = fv in phase and frequency

When the phase and frequency of fr and fv are equal, the charge pump will be in a quiet state, except for current spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

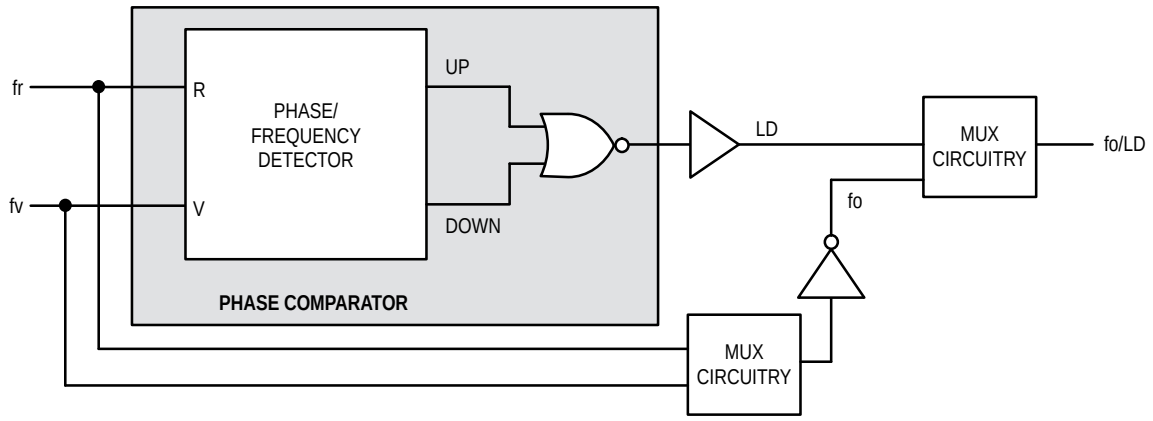


Figure 4. Detailed Phase/Frequency Comparator Block Diagram

LOCK DETECT

When the lock detector signal (Lock–IF or Lock–RF) is selected to be routed to the fo/LD output pin, the lock detector circuit provides a LOW pulse when fr and fv are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See NO TAG. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See NO TAG.

fo

When selected, the output frequency pin (fo/LD) provides a LOW going pulse at the fr or fv rate. The pulse width is determined by the frequency in the respective counter. This output is for test purposes only and may not swing all the way down to ground. The scope probe capacitive load should be less than 5pF.

OSCILLATOR INPUT

The device incorporates an on–chip reference buffer so that an external reference oscillator signal can be ac–coupled to the OSCin pin through a coupling capacitor. The magnitude of the ac–coupled signal must be between 500 and 2200 mV peak–to–peak.

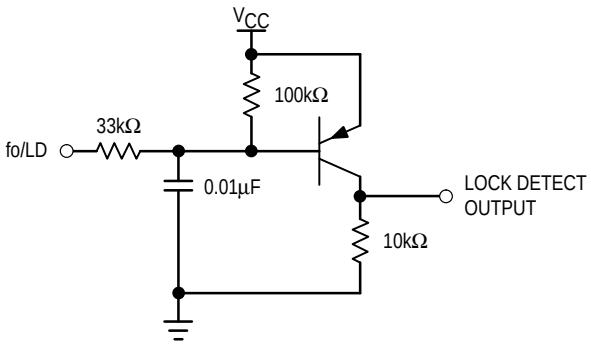


Figure 5. Typical Lock Detect Circuit

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5V; V_P = V_{CC} to 6.0V; T_A = –40 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I_{CC}	Supply Current for V_{CC}		10.0		mA	Note 1
			11.0		mA	Note 2
I_P	Supply Current for V_P		0.5		mA	Note 3
			0.7		mA	Note 4
F_{IN}–RF	Operating Frequency f_{IN}max f_{IN}min	2000		 500	MHz	Note 5
F_{IN}–IF	Operating Frequency f_{IN}max f_{IN}min	500		 40	MHz	Note 5
F_{OSC}	Operating Frequency (OSCin)	TBD	12	40	MHz	Note 5
V_{IN}	Input Sensitivity f_{IN}–RF (100–500MHz) f_{IN}–IF (40–100MHz) f_{IN}–IF	200 200 600		1000 1000 2000	$mV_{P–P}$	
V_{OSC}	OSCin	500		2200	$mV_{P–P}$	
V_{IH}	Input HIGH Voltage CLK, DATA, LE	$0.7V_{CC}$			V	
V_{IL}	Input LOW Voltage CLK, DATA, LE			$0.3V_{CC}$	V	
I_{IH}	Input HIGH Current (DATA, CLK and LE)		0.1	2.0	µA	V_{CC} = 5.5V
I_{IL}	Input LOW Current (DATA, CLK and LE)	–2.0	–0.1		µA	V_{CC} = 5.5V
I_{OSC}	Input Current (OSCin)		TBD		µA	
I_{Source}	Charge Pump Output Current		–2.0		mA	V_{Do} = V_P/2; V_P = 2.7V
I_{Sink}	Do		+2.0			V_{CC} = 2.7V; Note 6
$I_{Hi–Z}$	Output Disabled	–15		+15	nA	0.5V < V_{Do} < V_P – 0.5V
V_{OH}	Output HIGH Voltage (fo/LD)	4.4			V	V_{CC} = 5.0V
		2.4			V	V_{CC} = 3.0V
V_{OL}	Output LOW Voltage (fo/LD)			0.4	V	V_{CC} = 5.0V
				0.4	V	V_{CC} = 3.0V
I_{OH}	Output HIGH Current (fo/LD)			–1.0	mA	
I_{OL}	Output LOW Current (fo/LD)	1.0			mA	

1. V_{CC} = 3.3V, all outputs open.
2. V_{CC} = 5.5V, all outputs open.
3. V_P = 3.3V, all outputs open.
4. V_P = 6.0V, all outputs open.
5. AC coupling, F_{IN} measured with a 1000pF capacitor.
6. Source current flows out of the pin and sink current flows into the pin, typical charge pump sink and source curves are found in NO TAG.

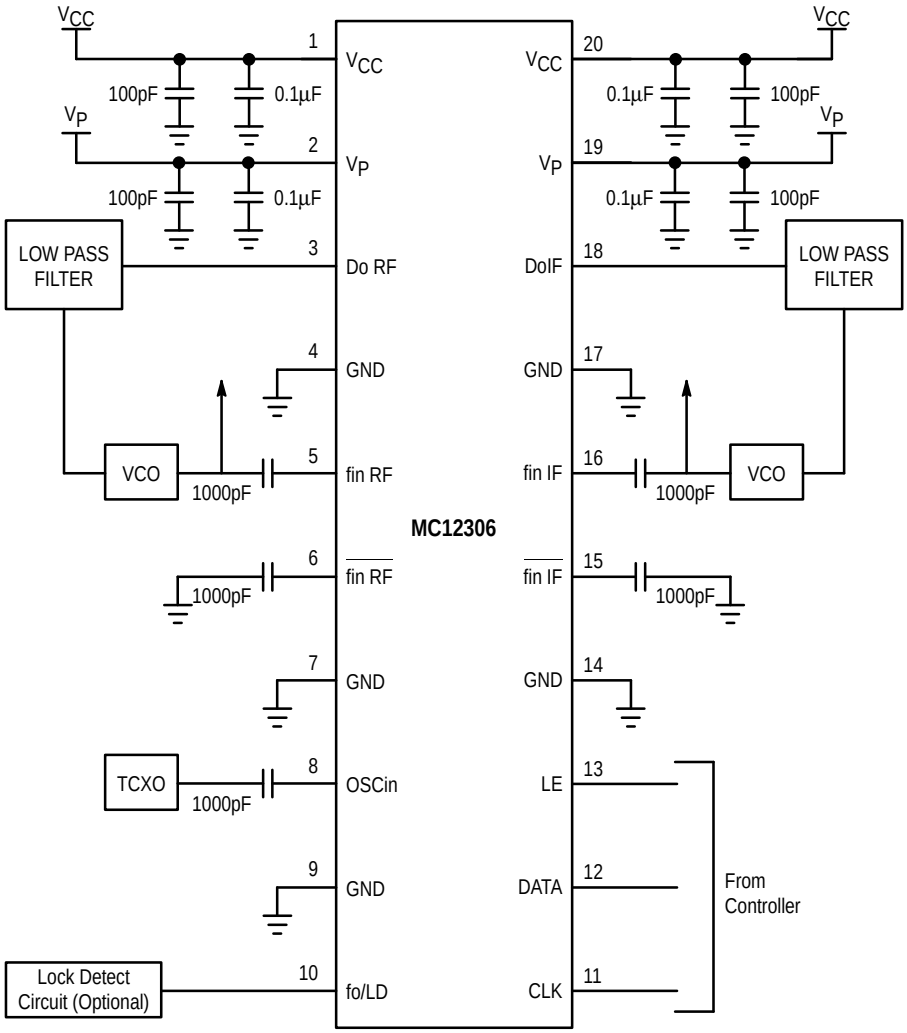


Figure 6. Typical Applications Example

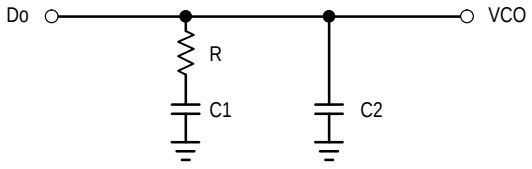


Figure 7. Typical Loop Filter

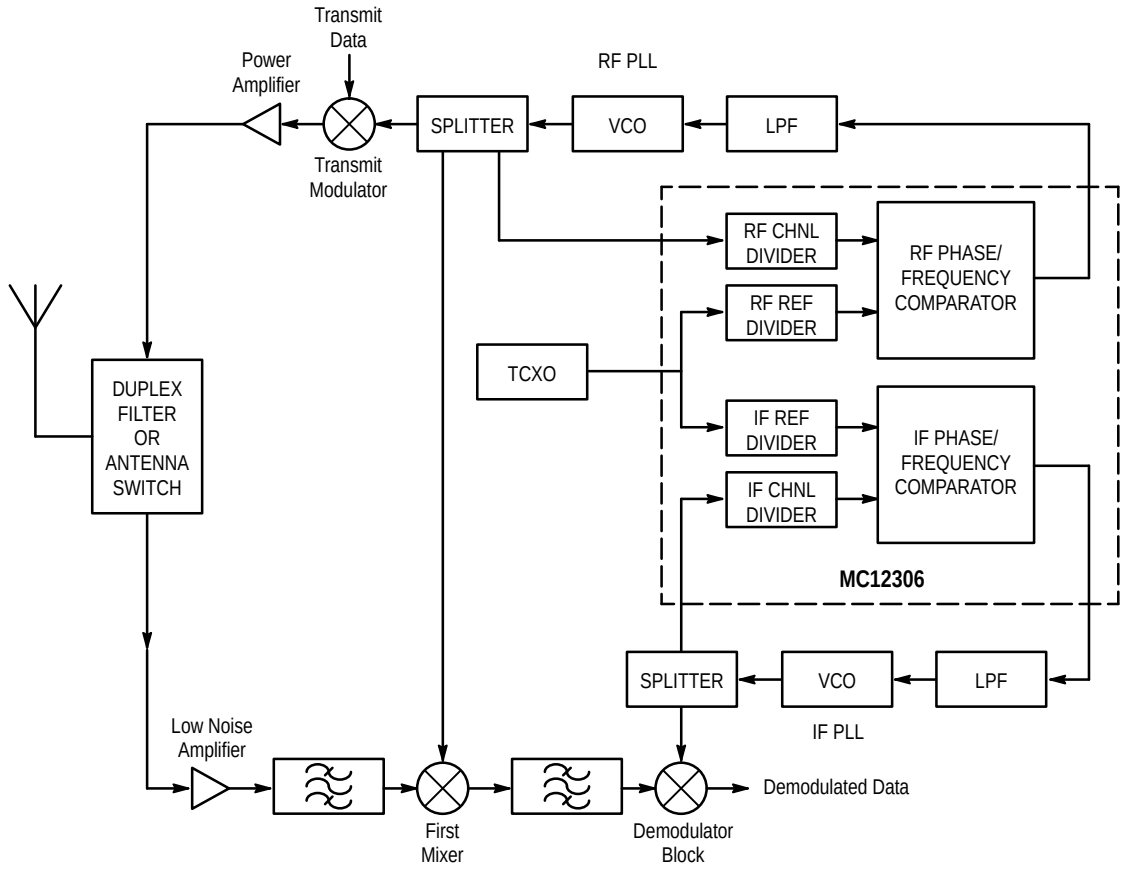


Figure 8. Typical Sub–System Block Diagram

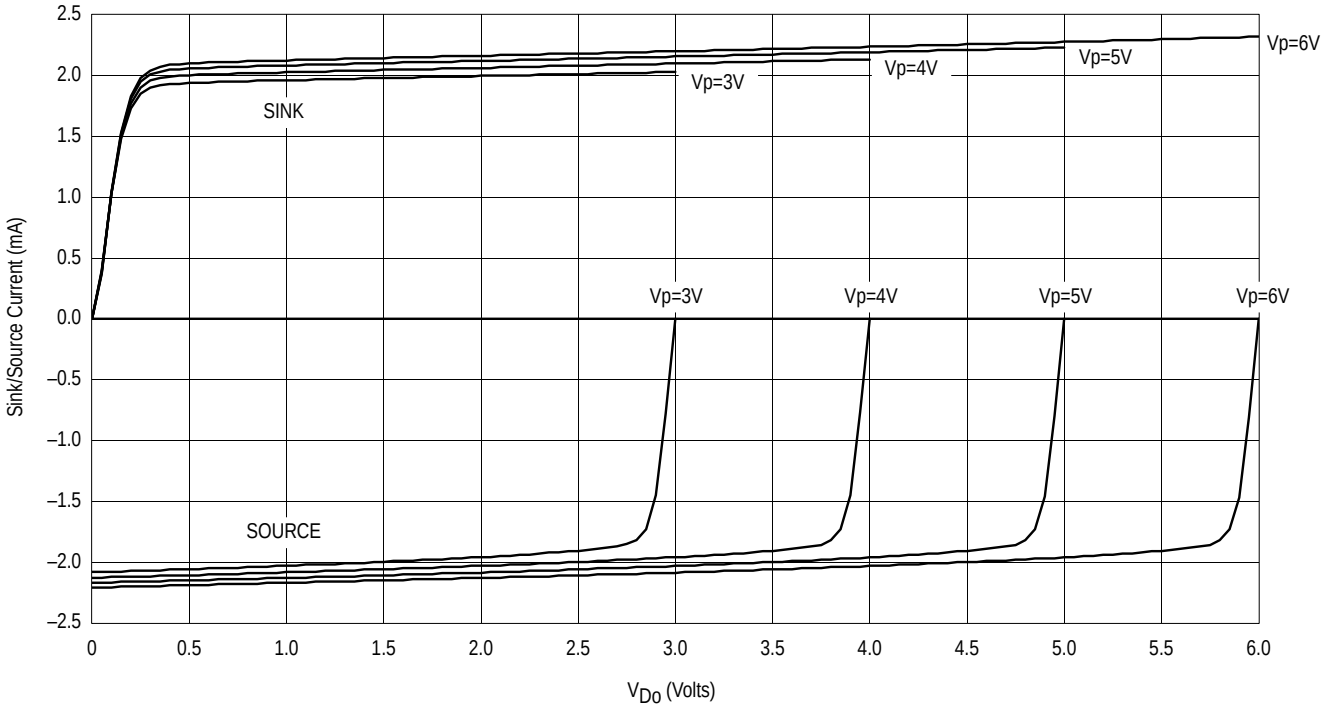
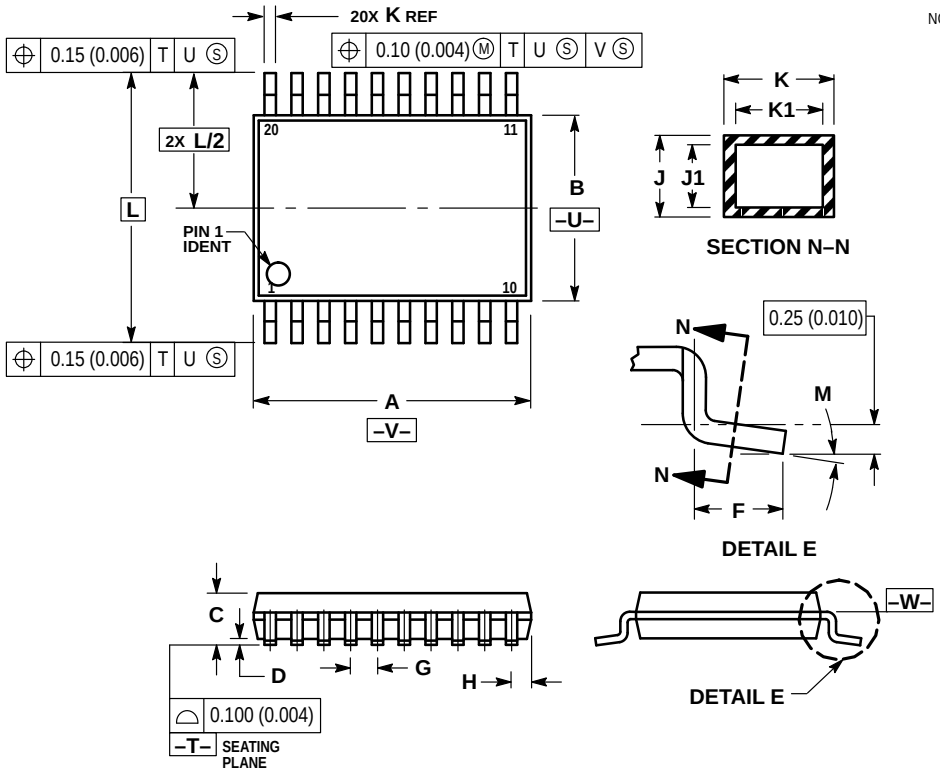


Figure 9. Typical MC12306 Charge Pump Sink and Source Current versus V_{Do}
(V_{CC} = 2.7V, T_A = 25°C)

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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