Product Preview

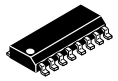
125-1000MHz Frequency Synthesizer

MC12181

125–1000MHz FREQUENCY SYNTHESIZER

The MC12181 is a monolithic bipolar synthesizer integrating a high performance prescaler, programmable divider, phase/frequency detector, charge pump, and reference oscillator/buffer functions. The device is capable of synthesizing a signal which is 25 to 40 times the input reference signal. The device has a 4–bit parallel interface to set the proper total multiplication which can range from 25 to 40. When combined with an external passive loop filter and VCO, the MC12181 serves as a complete PLL subsystem.

- 2.7 to 5.5V Operation
- Low power supply current of 4.5mA typical
- On chip reference oscillator/buffer supporting wide frequency operating range from 5 to 25MHz
- 4–bit parallel interface for programming divider (P = 25 .... 40)
- Wide 125 – 1000MHz frequency of operation
- Digital phase/frequency detector with linear transfer function
- Balanced Charge Pump Output
- Space efficient 16 lead SOIC package
- Operating Temperature Range of –40°C to 85°C
- > 1000 Volt ESD Protection (I/O to Ground, I/O to V_{CC})



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05

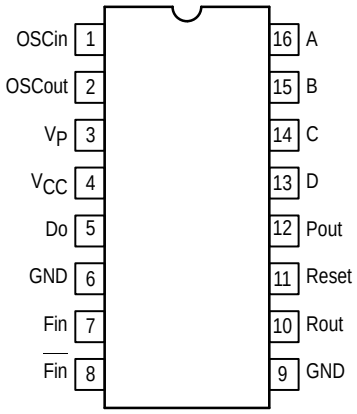
The device is suitable for application where a fixed local oscillator (LO) needs to be synthesized or where a limited number of LO frequencies need to be generated. The device also has auxiliary open emitter outputs (Pout and Rout) for observing the inputs to the phase detector for verification purposes. In normal use the pins should be left open. The Reset input is normally LOW. When this input is placed in the HIGH state the programmable divider and reference prescaler is reset and the charge pump output (Do) is placed in the OFF state.

The 4–bit programming interface maps into divider states ranging from 25 to 40. A is the LSB and D is the MSB. The data inputs (A,B,C, and D) are CMOS compatible and have pull–up resistors. The inputs can be tied directly to Vcc or Ground for programming or can be interfaced to an external data latch/register. Table 1 below has a mapping of the programming states.

Table 1. Programming States

D	C	B	A	Divider
L	L	L	L	25
L	L	L	H	26
L	L	H	L	27
L	L	H	H	28
L	H	L	L	29
L	H	L	H	30
L	H	H	L	31
L	H	H	H	32
H	L	L	L	33
H	L	L	H	34
H	L	H	L	35
H	L	H	H	36
H	H	L	L	37
H	H	L	H	38
H	H	H	L	39
H	H	H	H	40

Pinout: 16–Lead SOIC (Top View)



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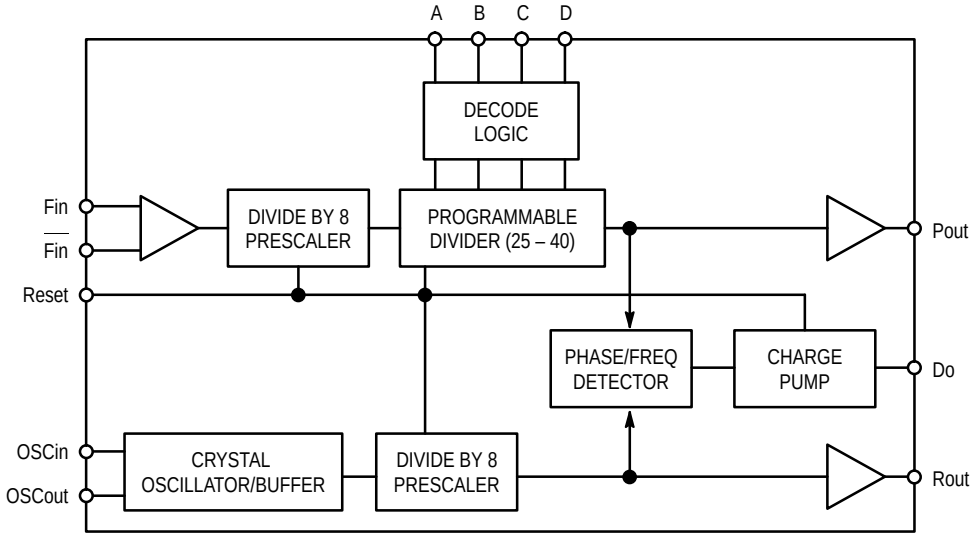

Figure 1. MC12181 Programmable Synthesizer

PIN NAMES

Pin	Pin No.	Function
OSCin	1	An external parallel resonant, fundamental crystal is connected between OSCin and OSCout to form an internal reference crystal oscillator. External capacitors C1 and C2 are required to set the proper crystal load capacitance and oscillator frequency (Figure 2). For an external reference oscillator, a signal is AC–coupled into the OSCin pin. In either mode a 50kΩ resistor must be connected between OSCin and OSCout.
OSCout	2	Oscillator output, for use with an external crystal as shown in Figure 2.
V_P	3	Positive power supply for charge pump. V_P MUST be greater than or equal to V_{CC}. Bypassing should be placed as close as possible to this pin and be connected directly to the ground plane.
V_{CC}	4	Positive power supply. Bypassing should be placed as close as possible to this pin and be connected directly to the ground plane.
Do	5	Single ended phase/frequency detector output. Three–state current sink/source output for use as a loop error signal when combined with an external low pass filter. The phase/frequency detector is characterized by a linear transfer function.
GND	6	Ground. This pin should be directly tied to the ground plane.
Fin	7	Prescaler input – The VCO signal is ac–coupled into the Fin Pin.
$\overline{\text{Fin}}$	8	Complementary prescaler input – This pin should be capacitively coupled to ground.
GND	9	Ground. This pin should be directly tied to the ground plane.
Rout	10	Open emitter test point used to verify proper operation of the reference divider chain. In normal operation this pin should be left OPEN.
Reset	11	Test pin used to clear the programmable divider and prescaler (Reset = H). When the Reset is in the HIGH state, the charge pump output is disabled. The Reset input has an internal pulldown. In normal operation it can be left open or tied to ground.
Pout	12	Open emitter test point used to verify proper operation of the programmable divider chain. In normal operation this pin should be left OPEN.
D C B A	13 14 15 16	Digital control inputs for setting the value of the programmable divider. A is the LSB and D is the MSB. In normal operation these pins can be tied to V_{CC} and/or ground to program a fixed divide or they can be driven by a CMOS logic level when used in a programmable mode. There is an internal pull–up resistor to V_{CC} on each input.

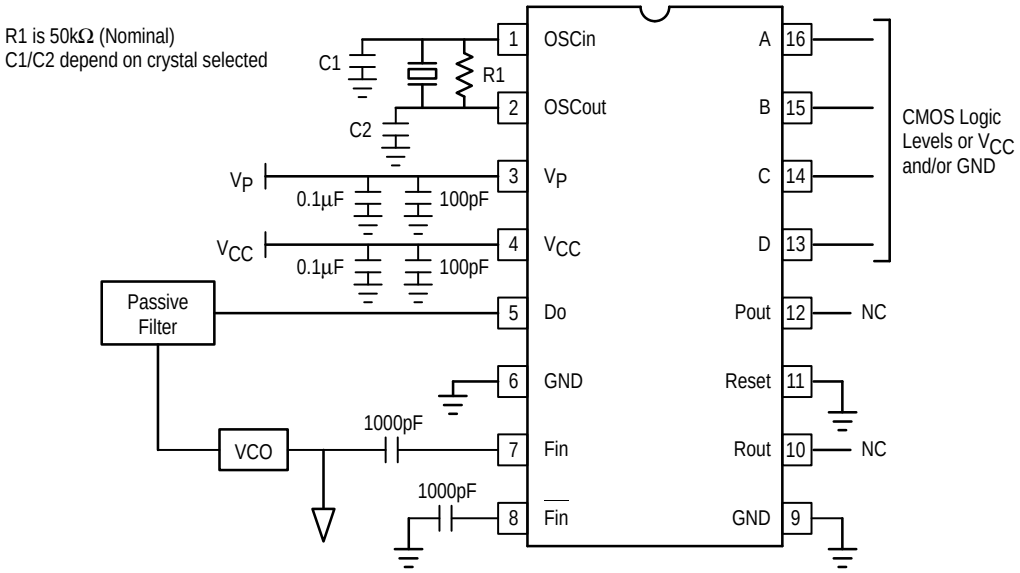

Figure 2. Typical Applications Example

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Range	2.7	5.5	VDC
V_{CC}max	Maximum Supply Range		6.0	VDC
$V_P$max	Maximum Charge Pump Voltage		V_{CC} to +6.0	VDC
T_A	Temperature Ambient	–40	85	°C
T_{STG}	Storage Temperature	–65	150	°C
V_{in}max	Maximum Input Signal (Any Pin)		V_{CC}+0.5V	VDC

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5V; V_P = V_{CC} to 5.5V; T_A = –40 to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{CC}	Supply Current for V_{CC}		4		mA	Note 1
I_P	Supply Current for V_P		0.5		mA	Note 1
OSCin	Input Frequency Range	5		25	MHz	Note 2
Fin	RF Input Frequency Range	125		1000	MHz	Note 3
Vin	Fin Input Sensitivity	100		1000	mV_{P-P}	Note 4
V_{OSC}	OSCin Input Sensitivity	500		2200	mV_{P-P}	Note 4
I_{OH}	Output Source Current (Do)	–2.8	–2.2	–1.6	mA	Note 5, V_{CC}=V_P=5.5, VDo=2.75V
I_{OL}	Output Sink Current (Do)	1.6	2.2	2.8	mA	Note 5, V_{CC}=V_P=5.5, VDo=2.75V
I_{OZ}	Output Leakage Current (Do)		0.5	15	nA	V_{CC}=V_P=5.5, VDo=2.75V
VDo	Charge Pump Operating Volt	0.5		V_P–0.5	V	
V_{IH}	Input HIGH Voltage (Reset, A, B, C, D)	0.7 V_{CC}			V	
V_{IL}	Input LOW Voltage (Reset, A, B, C, D)			0.3 V_{CC}	V	
I_{IH}	Input HIGH Current (Reset, A, B, C, D)			TBD	µA	
I_{IL}	Input LOW Current (Reset, A, B, C, D)	TBD			µA	
Vout	Output Amplitude (Pout, Rout)	800			mV	Note 6

1. V_{CC} and V_P = 5.5V; Fin = 1.0GHz; OSCin = 25MHz; Do open.
2. Assumes C_1 and C_2 (Figure 2) limited to ≤30pF each including stray capacitance in crystal mode, AC coupled input for external reference mode.
3. AC coupling, Fin measured with a 1000pF capacitor.
4. Signal AC coupling in input.
5. Min and Max values are targeted at <±30% of nominal.
6. Minimum resistor value of 20kΩ to ground.

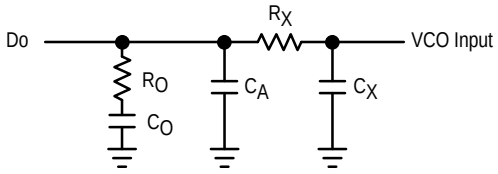

Figure 3. Typical Loop Filter Topology

OUTLINE DIMENSIONS

D SUFFIX
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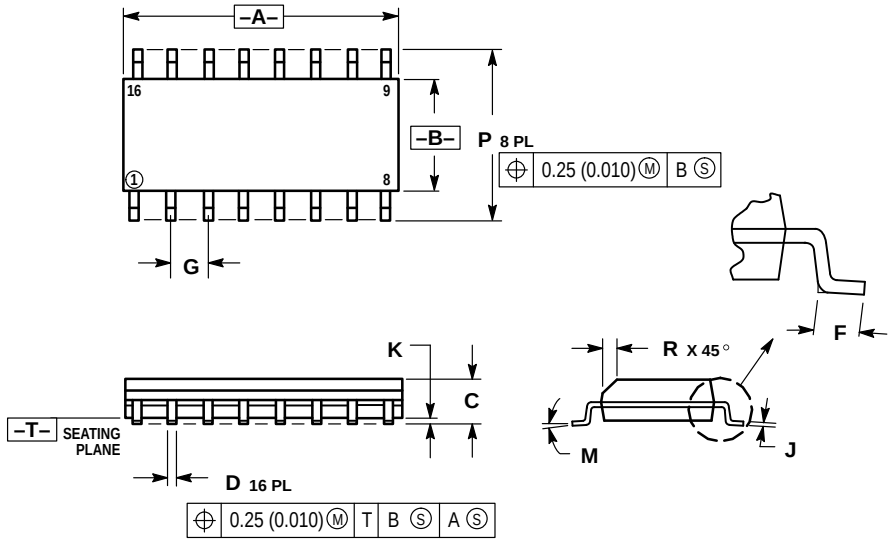
CASE 751B-05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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