Advance Information

PLL Frequency Synthesizer

MC12179

MECL PLL COMPONENTS

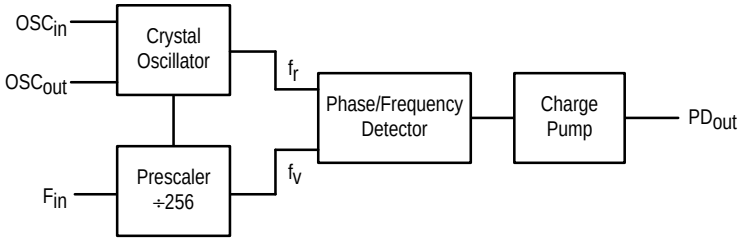
PLL Frequency Synthesizer

The MC12179 is a monolithic Bipolar synthesizer integrating the high frequency prescaler, phase/frequency detector, charge pump, and reference oscillator/buffer functions. When combined with an external loop filter and VCO, the MC12179 serves as a wide bandwidth PLL. Motorola's advanced Bipolar MOSAIC™ V technology is utilized for low power operation at a 5V supply voltage. The device is designed for operation up to 2.8GHz for wide bandwidth applications such as CATV down converters and satellite receiver tuners.

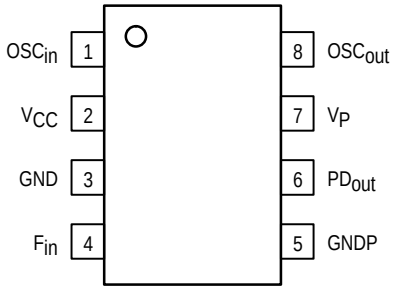
- 2.8GHz Maximum Operating Frequency
- Low Power Supply Current of 3.5mA Typical, Including I_{CC} and I_P Currents
- Supply Voltage of 5.0V Typical
- Integrated Divide by 256 Prescaler
- On-Chip Reference Oscillator/Buffer
- Digital Phase/Frequency Detector with Linear Transfer Function
- Balanced Charge Pump Output
- Space Efficient 8-Lead SOIC
- Operating Temperature Range of –40°C to +85°C
- Synthesizer With Phase Inverted Charge Pump Output Available – Please Consult a Motorola Representative

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

BLOCK DIAGRAM



Pinout: 8-Lead SOIC (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage, Pin 2	–0.5 to +6.0	VDC
V_P	Power Supply Voltage, Pin 7	V_{CC} to +6.0	VDC
T_{stg}	Storage Temperature Range	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MOSAIC V is a trademark of Motorola, Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5V; V_P = V_{CC} to 5.5V; T_A = –40 to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{CC}	Supply Current for V_{CC}		3.1		mA	Note 1
I_P	Supply Current for V_P		0.4		mA	Note 1
F_{IN}	Operating Frequency f_{IN}max f_{IN}min	2800		 500	MHz	Note 2
F_{OSC}	Operating Frequency Crystal Mode External Oscillator OSC_{in}			11 11	MHz	Note 3 Note 4
V_{IN}	Input Sensitivity F_{in}	100		1000	mV_{P-P}	Note 2
V_{OSC}	Input Sensitivity External Oscillator OSC_{in}	500		2200	mV_{P-P}	Note 4
I_{OSC}	Input Current		130 –310		µA	OSCin = V_{CC} OSCin = V_{CC}–2.2V
V_{IH}	Input HIGH Voltage (OSC_{in})	V_{CC} – 0.85		V_{CC}	V	
V_{IL}	Input LOW Voltage (OSC_{in})	V_{CC} – 2.20		V_{CC} – 1.35	V	
V_{OH}	Output HIGH Voltage (PD_{out})	V_P – 0.5			V	I_{OH} = –2.0mA
V_{OL}	Output LOW Voltage (PD_{out})			0.5	V	I_{OL} = 2mA
I_{OH}	Output Source Current (PD_{out})	–1.5	–2.0	–2.5	mA	V_P = 5.0V, V_{PDout} = V_P/2
I_{OL}	Output Sink Current (PD_{out})	1.5	2.0	2.5	mA	V_P = 5.0V, V_{PDout} = V_P/2
I_{OZ}	Output Leakage Current (PD_{out})			TBD	nA	

1. V_{CC} or V_P = 5.0V; F_{IN} = 2.56GHz; F_{OSC} = 10MHz crystal; PD_{out} open.
2. AC coupling, F_{IN} measured with a 1000pF capacitor.
3. Assumes C_1 and C_2 (Figure 1) limited to ≤30pF each including stray and parasitic capacitances for a maximum 11MHz crystal.
4. AC coupling to OSC_{in}.

PIN NAMES

Pin	I/O	Function	Pin No.
OSCin	I	Oscillator Input — An external parallel-resonant, fundamental crystal is connected between OSC_{in} and OSC_{out} to form an internal reference oscillator (crystal mode). External capacitors C1 and C2, as shown in Figure 1, are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen (up to a maximum of 30pF each including parasitic and stray capacitances). For an external reference oscillator, an external signal is AC-coupled to the OSC_{in} pin with a 1000pF coupling capacitor, with no connection to OSC_{out}. The AC-coupled signal must be at least 500mV_{P-P} and less than 2200mV_{P-P}. DC-coupling can be applied directly to the OSC_{in} pin for large amplitude signals limited to the V_{IL} and V_{IH} levels as specified in the Electrical Characteristics table, with no connection to OSC_{out}.	1
V_{CC}	—	Positive Power Supply.	2
GND	—	Ground.	3
F_{in}	I	Prescaler Input — This input is typically the loop VCO signal AC coupled into the F_{in} pin.	4
GNDP	—	Ground — For charge pump circuitry.	5
PD_{out}	O	Single ended phase/frequency detector output (charge pump output). Three-state current sink/source output for use as a loop error signal when combined with an external low pass filter. The phase/frequency detector is characterized by a linear transfer function.	6
V_P	—	Positive power supply for charge pump.	7
OSCout	O	Oscillator output, for use with an external cystal as shown in Figure 1.	8

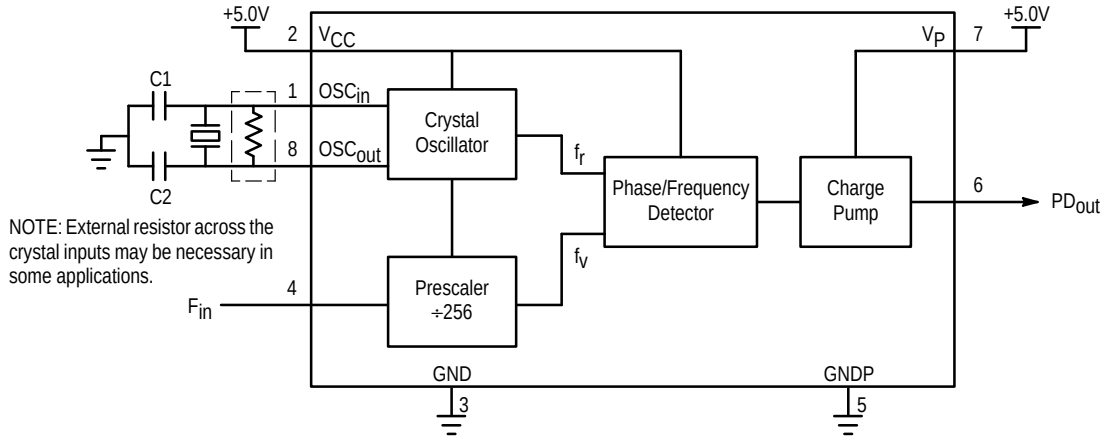


Figure 1. MC12179 Expanded Block Diagram

PHASE CHARACTERISTICS

The phase comparator in the MC12179 is a high speed digital phase/frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fv) signal and the reference (fr) input. The detector can cover a range of $\pm 2\pi$ radian of fv/fr phase difference. The operation of the charge pump output is shown in Figure 2.

fv leads fr in phase OR fv > fr in frequency

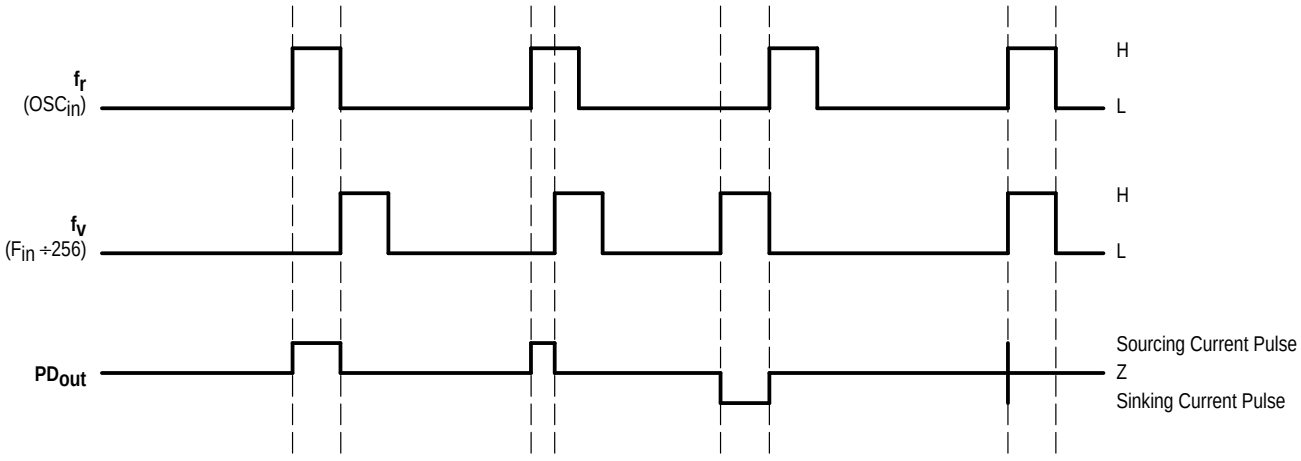
When the phase of fv leads that of fr or the frequency of fv is greater than fr, the PDout output will pulse LOW from a high impedance (HIGH-Z) state (current sinking pulse). The signal on PDout indicates to the VCO to decrease in frequency to bring the loop into lock.

fv lags fr in phase OR fv < fr in frequency

When the phase of fv lags that of fr or the frequency of fv is less than fr, the PDout output will pulse HIGH from a HIGH-Z state (current sourcing pulse). The signal on PDout indicates to the VCO to increase in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fv and fr are equal, the output PDout remains in the HIGH–Z state, except for the narrow source and sink self–canceling current pulses to eliminate the deadband. This situation indicates that the loop is in lock. The phase/frequency detector will cause either a wider sink or source current pulse to occur as necessary to maintain the loop in its locked state.



H = High voltage level; L = Low voltage level; Z = High impedance
NOTES: Phase difference detection range: ~–2π to 2π
Synthesizer with PDout charge pump output phase inversion available, please consult a Motorola representative.

Figure 2. Phase/Frequency Detector and Charge Pump Waveforms

OUTLINE DIMENSIONS

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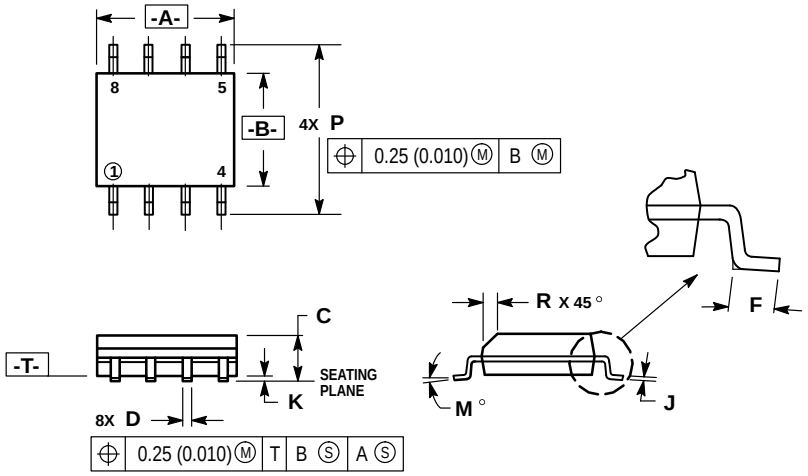
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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