# 2.0GHz Dual Modulus Prescaler

The MC12034A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 2.0GHz in programmable frequency steps.

The MC12034B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

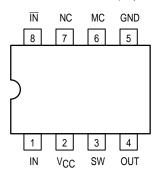
The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5V
- MC12034A for Positive Edge Triggered Synthesizers
- MC12034B for Negative Edge Triggered Synthesizers
- 12mA Maximum,  $-40^{\circ}$ C to  $+85^{\circ}$ C, V<sub>CC</sub> = 5.5Vdc
- · Modulus Control Input is Compatible with Standard CMOS and TTL
- Low-Power 8.5mA Typical

Design Criteria	Value	Unit
Internal Gate Count *	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	рJ

\*Equivalent to a two-input NAND gate.

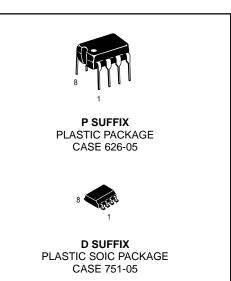
#### Pinout: 8-Lead Plastic (Top View)



## MC12034A MC12034B

### **MECL PLL COMPONENTS**

## ÷32/33, ÷64/65 DUAL MODULUS PRESCALER



### FUNCTION TABLE

SW	МС	Divide Ratio		
Н	Н	32		
Н	L	33		
L	Н	64		
L	L	65		

Note: SW: H = V<sub>CC</sub>, L = OPEN

MC: H = 2.0V to  $V_{CC}$ , L = GND to 0.8V

### MAXIMUM RATINGS

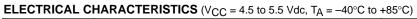
Symbol	Characteristic	Range	Unit
VCC	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
Т <sub>А</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	Vdc

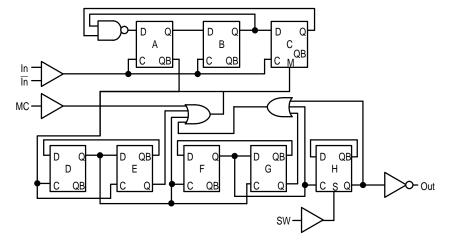
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

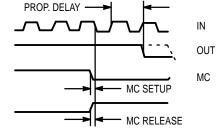


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Symbol	Characteristic	Min	Тур	Max	Unit
ft	Toggle Frequency (Sine Wave)	0.5	2.4	2.0	GHz
ICC	Supply Current Output Unloaded (Pin 2)	—	8.5	12	mA
VIH1	Modulus Control Input High (MC)	2.0		—	V
V <sub>IL1</sub>	Modulus Control Input Low (MC)	—		0.8	V
VIH2	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5V$	VCC	V <sub>CC</sub> + 0.5V	Vdc
V <sub>IL2</sub>	Divide Ratio Control Input Low (SW)	OPEN	OPEN	OPEN	—
V <sub>out</sub>	Output Voltage Swing (C <sub>L</sub> = 12 pF, R <sub>L</sub> = 1.1 k $\Omega$ )	1.0	1.6	—	V <sub>p-p</sub>
<sup>t</sup> SET	Modulus Setup Time MC to Out	—	8.0	10.0	ns
V <sub>in</sub>	Input Voltage Sensitivity 500–2000 MHz	100	_	1500	mVpp
IO	Output Current (C <sub>L</sub> = 12 pF, R <sub>L</sub> = 1.1 k $\Omega$ )	—	_	3.5	mA







Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

LOGIC DIAGRAM (MC12034A)



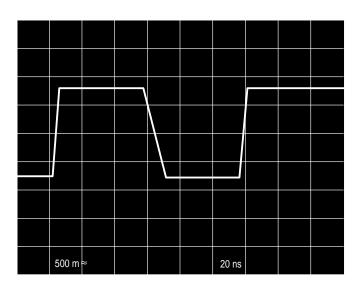


Figure 2. Typical Output Waveform

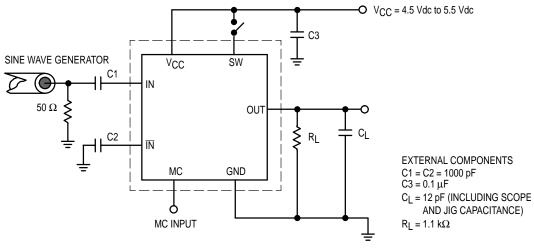
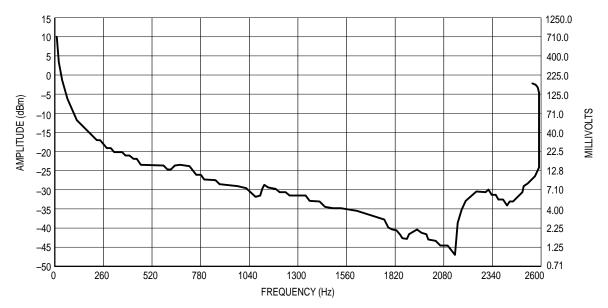
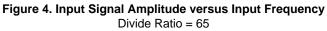


Figure 3. AC Test Circuit





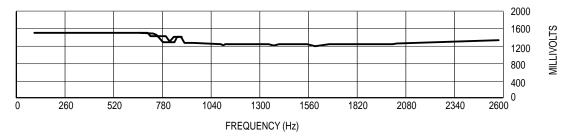
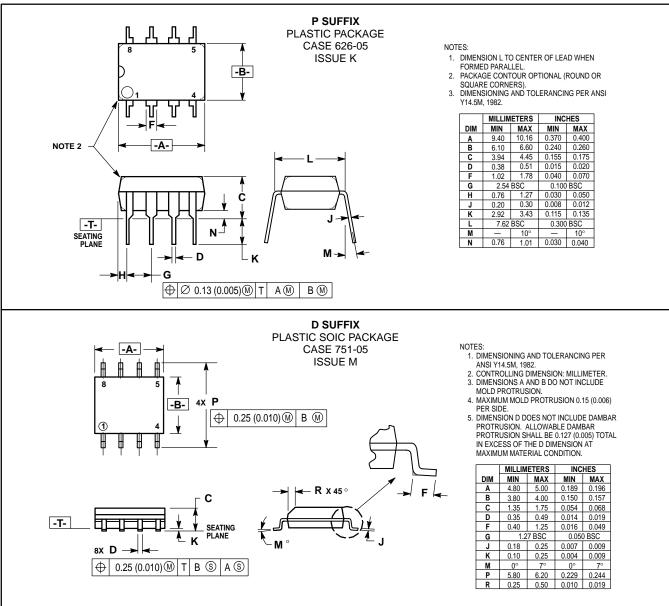


Figure 5. Output Amplitude versus Input Frequency

### **OUTLINE DIMENSIONS**



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